First Edition - 2008

Electronics Engineering

Premier12

U. A. Bakshi
A. P. Godse

Technical Publications Pune®

VISIT…

LANZAROTE
Caliente.COM

Table of Contents :

Chapter - 1 Semiconductor Diodes and Applications (1 - 1) to (1 - 170)

Chapter - 2 Zener Diode and Applications (2 - 1) to (2 - 26)

Chapter - 3 Bipolar Junction Transistor (3 - 1) to (3 - 92)

Chapter - 4 Transistor Amplifier (4 - 1) to (4 - 52)

Chapter - 5 Field Effect Transistor (5 - 1) to (5 - 70)

Chapter - 6 Operational Amplifiers (6 - 1) to (6 - 58)

Chapter - 7 Switching Theory and Logic Design (7 - 1) to (7 - 152)

Chapter - 8 Electronic Instruments (8 - 1) to (8 - 32)

Features of Book

- **More detailed and modular representation of chapters.**
- **Use of clear, plain and lucid language making the understanding very easy.**
- **Excellent theory well supported with the practical examples and illustrations.**
- **Approach of the book resembles classroom teaching.**

Best of Technical Publications
As per Revised Syllabus of UPTECH University - 2008 Course
Semester - I / II (Common to All Branches)

Electrical Engineering	**Bakshi**
Computer Concepts and Programming in C	**Godse**
Electronics Engineering	**Godse, Bakshi**

Electronics Engineering

Atul P. Godse
M. S. Software Systems (BITS Pilani)
B.E. Industrial Electronics
Formerly Lecturer in Department of Electronics Engg.
Vishwakarma Institute of Technology
Pune

Uday A. Bakshi
M. E.(Electrical)
Formerly Lecturer in Department of Electronics Engg.
Vishwakarma Institute of Technology
Pune

Visit us at : **www.vtubooks.com**

Technical Publications Pune

Electronics Engineering

ISBN 9788184315035

All rights reserved with Technical Publications. No part of this book should be reproduced in any form, Electronic, Mechanical, Photocopy or any information storage and retrieval system without prior permission in writing, from Technical Publications, Pune.

Published by :

Technical Publications Pune®
#1, Amit Residency, 412, Shaniwar Peth, Pune - 411 030, India.

Printer :

Alert DTPrinters
Sr.no. 10/3, Sinhagad Road,
Pune - 411 041

Preface

The importance of **Electronics Engineering** is well known in various engineering fields. Overwhelming response to our books on various subjects inspired us to write this book. The book is structured to cover the key aspects of the subject **Electronics Engineering.**

The book uses plain, lucid language to explain fundamentals of this subject. The book provides logical method of explaining various complicated concepts and stepwise methods to explain the important topics. Each chapter is well supported with necessary illustrations, practical examples and solved problems. All the chapters in the book are arranged in a proper sequence that permits each topic to build upon earlier studies. All care has been taken to make students comfortable in understanding the basic concepts of the subject.

The book not only covers the entire scope of the subject but explains the philosophy of the subject. This makes the understanding of this subject more clear and makes it more interesting. The book will be very useful not only to the students but also to the subject teachers. The students have to omit nothing and possibly have to cover nothing more.

We wish to express our profound thanks to all those who helped in making this book a reality. Much needed moral support and encouragement is provided on numerous occasions by our families. We wish to thank the **Publisher** and the entire team of **Technical Publications** who have taken immense pain to get this book in time with quality printing.

Any suggestion for the improvement of the book will be acknowledged and well appreciated.

Authors
A. P. Godse
U. A. Bakshi

Dedicated to Gururaj, Neha and Ruturaj

Table of Contents

Chapter - 1 Semiconductor Diodes and Applications (1 - 1) to (1 - 170)

1.1 Introduction .... 1 - 1

1.2 The Structure of Matter .... 1 - 1

  1.2.1 Structure of an Atom .... 1 - 2

1.3 Group - IV Materials (Semiconductor Materials) .... 1 - 3

  1.3.1 Structure of Semiconductor Materials .... 1 - 4

    1.3.1.1 Properties of Intrinsic materials .... 1 - 5

1.4 Ionization .... 1 - 5

1.5 The Energy-Band Theory .... 1 - 5

  1.5.1 The eV, Unit of Energy .... 1 - 7

1.6 Classification of Materials Based on Energy Band Theory .... 1 - 7

  1.6.1 Conductors .... 1 - 7

  1.6.2 Insulators .... 1 - 8

  1.6.3 Semiconductors .... 1 - 8

1.7 Intrinsic Semiconductors .... 1 - 9

  1.7.1 Crystal Structure of Intrinsic Semiconductor .... 1 - 9

  1.7.2 Charge Carriers in Intrinsic Semiconductors .... 1 - 10

  1.7.3 Conduction by Electrons and Holes .... 1 - 11

  1.7.4 Conduction in Intrinsic Semiconductors .... 1 - 12

1.8 Extrinsic Semiconductors .... 1 - 13

  1.8.1 Types of Impurities .... 1 - 13

1.9 n-Type Semiconductor .... 1 - 14

  1.9.1 Conduction in n-Type Semiconductor .... 1 - 14

1.10 p-Type Semiconductor .... 1 - 15

  1.10.1 Conduction in p-Type Semiconductor .... 1 - 16

1.11 P-N Junction .... 1 - 16

  1.11.1 Unbiased P-N Junction .... 1 - 16

  1.11.2 Formation of Depletion Region .... 1 - 17

1.11.3 Barrier Potential . . . . . 1 - 18
1.12 Unbiased P-N Junction . . . . . 1 - 19
1.12.1 Formation of Depletion Region . . . . . 1 - 19
1.12.2 Barrier Potential . . . . . 1 - 20
1.13 The p-n Junction Diode . . . . . 1 - 21
1.13.1 Biasing of p-n Junction Diode . . . . . 1 - 22
1.13.2 Types of Diodes . . . . . 1 - 22
1.14 Forward Biasing of p-n Junction Diode . . . . . 1 - 23
1.14.1 Operation of Forward Biased Diode . . . . . 1 - 23
1.14.2 Effect on the Depletion Region . . . . . 1 - 24
1.14.3 Effect of the Barrier Potential . . . . . 1 - 24
1.15 Reverse Biasing of p-n Junction Diode . . . . . 1 - 25
1.15.1 Operation of Reverse Biased Diode . . . . . 1 - 25
1.15.2 Breakdown in Reverse Biased . . . . . 1 - 27
1.16 The Volt-Ampere (V-I) Characteristics of a Diode . . . . . 1 - 28
1.16.1 Forward Characteristics of p-n Junction Diode . . . . . 1 - 28
1.16.2 Reverse Characteristics of p-n Junction Diode . . . . . 1 - 31
1.16.3 Complete V-I Characteristics of a Diode . . . . . 1 - 32
1.16.4 V-I Characteristics of Typical Ge and Si Diodes . . . . . 1 - 33
1.17 Equation of V-I Characteristics of Diode . . . . . 1 - 35
1.17.1 Nature of V-I Characteristics from Equation of Diode . . . . . 1 - 36
1.18 Effect of Temperature on Diode . . . . . 1 - 37
1.19 Junction Capacitances . . . . . 1 - 39
1.19.1 Transition Capacitance (C_T or C_{pn}) . . . . . 1 - 39
1.19.2 Diffusion Capacitance (C_D) . . . . . 1 - 40
1.20 A.C. Equivalent Circuits . . . . . 1 - 41
1.21 Diode Ratings . . . . . 1 - 42
1.21.1 Datasheet Specifications of 1N4001 - 1N4007 . . . . . 1 - 43
1.22 Mathematical Expression for the Dynamic Resistance . . . . . 1 - 45
1.23 What is Rectifier ? . . . . . 1 - 47
1.24 The Important Characteristics of a Rectifier Circuit . . . . . 1 - 47
1.25 Half Wave Rectifier . . . . . 1 - 48
1.25.1 Operation of the Circuit . . . . . 1 - 49
1.25.2 Average D.C. Load Current (I_{DC}) . . . . . 1 - 50

1.25.3 Average D.C. Load Voltage (E_{DC}) . . . . . 1 - 51
1.25.4 R.M.S. Value of Load Current (I_{RMS}) . . . . . 1 - 51
1.25.5 R.M.S. Value of the Load Voltage . . . . . 1 - 52
1.25.6 D.C. Power Output (P_{DC}) . . . . . 1 - 52
1.25.7 A.C. Power Input (P_{AC}) . . . . . 1 - 52
1.25.8 Rectifier Efficiency (η) . . . . . 1 - 53
1.25.9 Ripple Factor (γ) . . . . . 1 - 53
1.25.10 Load Current . . . . . 1 - 55
1.25.11 Peak Inverse Voltage (PIV) . . . . . 1 - 55
1.25.12 Transformer Utilization Factor (T.U.F.) . . . . . 1 - 56
1.25.13 Voltage Regulation . . . . . 1 - 57
1.25.13.1 Regulation Characteristics . . . . . 1 - 57
1.25.14 Disadvantages of Half Wave Rectifier Circuit . . . . . 1 - 58
1.25.15 Effect of Barrier Potential . . . . . 1 - 58
1.26 Full Wave Rectifier . . . . . 1 - 62
1.26.1 Operation of the Circuit . . . . . 1 - 62
1.26.2 Maximum Load Current . . . . . 1 - 64
1.26.3 Average D.C. Load Current (I_{DC}) . . . . . 1 - 65
1.26.4 Average D.C. Load Voltage (E_{DC}) . . . . . 1 - 66
1.26.5 RMS Load Current (I_{RMS}) . . . . . 1 - 66
1.26.6 R.M.S. Value of the Load Voltage . . . . . 1 - 67
1.26.7 D.C. Power Output (P_{DC}) . . . . . 1 - 67
1.26.8 A.C. Power Input (P_{AC}) . . . . . 1 - 67
1.26.9 Rectifier Efficiency (η) . . . . . 1 - 68
1.26.10 Ripple Factor (γ) . . . . . 1 - 68
1.26.11 Load Current (i_L) . . . . . 1 - 68
1.26.12 Peak Inverse Voltage (PIV) . . . . . 1 - 69
1.26.13 Transformer Utilization Factor (T.U.F.) . . . . . 1 - 70
1.26.14 Voltage Regulation . . . . . 1 - 71
1.26.15 Advantages of Full Wave Rectifier . . . . . 1 - 72
1.26.16 Disadvantages of Full Wave Rectifier . . . . . 1 - 72
1.26.17 Comparison of Half Wave and Full Wave Rectifiers . . . . . 1 - 72
1.27 Bridge Rectifier . . . . . 1 - 77
1.27.1 Operation of the Circuit . . . . . 1 - 77
1.27.2 Expressions for Various Parameters . . . . . 1 - 78
1.27.3 PIV Rating of Diodes . . . . . 1 - 80

1.27.4 What Happens if Input and Output Terminals are Reversed? . . . . 1 - 80
1.27.5 Advantages of Bridge Rectifier Circuit . . . . 1 - 81
1.27.6 Disadvantages of Bridge Rectifier . . . . 1 - 81
1.27.7 Applications . . . . 1 - 82

1.28 Comparison of Rectifier Circuits .... 1 - 84

1.29 Filter Circuits... 1 - 85

1.30 Capacitor Input Filter .... 1 - 86
1.30.1 Operation of the Filter with Half Wave Rectifier . . . . 1 - 86
1.30.2 Operation with Full Wave Rectifier . . . . 1 - 88
1.30.3 Approximate Analysis of Capacitor Input Filter. . . . . 1 - 90
1.30.4 Why Capacitor Filter is not Suitable for Variable Loads? . . . . 1 - 92
1.30.5 How to Decrease Ripple Factor ?. . . . . 1 - 92
1.30.6 D.C. Output Voltage with Capacitor Filter. . . . . 1 - 92
1.30.7 Expression for Ripple Voltage . . . . 1 - 93
1.30.8 Surge Current in a Capacitor Input Filter . . . . 1 - 93
1.30.8.1 Limiting the Surge Current. . . . . 1 - 95
1.30.9 Advantages . . . . 1 - 96
1.30.10 Disadvantages . . . . 1 - 96

1.31 Circuit Models of a Diode .... 1 - 98
1.31.1 Practical Diode Model . . . . 1 - 98
1.31.2 Ideal Diode Model . . . . 1 - 99
1.31.3 Piecewise Linear Model of Diode . . . . 1 - 99
1.31.4 Analysis of Diode Circuits . . . . 1 - 101

1.32 Clipper Circuits or Limiters .... 1 - 102
1.32.1 Steps to Analyse Clipper Circuits . . . . 1 - 102

1.33 Series Clippers .... 1 - 102
1.33.1 Series Negative Clipper Circuit. . . . . 1 - 103
1.33.2 Series Positive Clipper Circuit . . . . 1 - 106
1.33.3 Clipping Above Reference Voltage V_R . . . . 1 - 108
1.33.4 Clipping Below Reference Voltage V_R . . . . 1 - 110
1.33.5 Additional D.C. Supply in Series with Diode. . . . . 1 - 112

1.34 Parallel Clippers .... 1 - 115
1.34.1 Basic Parallel Clipper with Positive Clipping . . . . 1 - 116
1.34.2 Effect of Cut-in Voltage of Diode . . . . 1 - 118
1.34.3 Basic Parallel Clipper with Negative Limiting . . . . 1 - 120

1.35 Parallel Clipper Circuits with Reference Voltage V_R .... 1 - 123
1.35.1 Operation .... 1 - 124
1.35.2 Transfer Characteristics .... 1 - 125
1.35.3 Effect of Cut-in Voltage of Diode .... 1 - 126
1.35.4 Parallel Negative Clipper with Reference Voltage V_R .... 1 - 128
1.36 Two Way Parallel Clipper Circuit .... 1 - 131
1.36.1 Operation .... 1 - 132
1.36.2 Transfer Characteristics .... 1 - 133
1.37 Clamper Circuits .... 1 - 134
1.37.1 Negative Clamper .... 1 - 134
1.37.2 Positive Clamper .... 1 - 137
1.37.3 Steps to Analyze Clamping Network .... 1 - 139
1.37.4 Addition of Battery in Clamper .... 1 - 140
1.37.5 Clamper Application .... 1 - 141
1.38 Voltage Multipliers .... 1 - 142
1.38.1 Half Wave Voltage Doubler .... 1 - 142
1.38.2 Full Wave Voltage Doubler .... 1 - 144
1.38.3 Voltage Tripler .... 1 - 146
1.38.4 Voltage Quadrupler .... 1 - 149
1.38.5 Advantages, Applications and Limitations .... 1 - 149
Examples with Solutions .... 1 - 150
Review Questions .... 1 - 168

Chapter - 2 Zener Diode and Applications (2 - 1) to (2 - 26)

2.1 Introduction .... 2 - 1
2.2 Characteristics of Zener Diode .... 2 - 1
2.3 Equivalent Circuit of Zener Diode .... 2 - 3
2.4 Effect of Temperature on Zener Diode .... 2 - 4
2.5 Zener Power Dissipation and Derating .... 2 - 5
2.6 Zener Diode Data Sheet Interpretation .... 2 - 6
2.6.1 Electrical Characteristics .... 2 - 6
2.6.2 Graphical Information .... 2 - 7
2.7 Breakdown Mechanisms in Zener Diode .... 2 - 9
2.7.1 Zener Breakdown .... 2 - 10
2.7.2 Avalanche Breakdown .... 2 - 10

2.7.3 Comparison of Breakdown Mechanisms . . . . . 2 - 11
2.8 Comparison of Zener Diode and p-n Junction Diode . . . . . 2 - 11
2.9 Applications of Zener Diode . . . . . 2 - 12
2.10 Regulated Power Supply . . . . . 2 - 12
2.11 Zener Diode as a Shunt Regulator . . . . . 2 - 13
2.11.1 Regulation with Varying Input Voltage . . . . . 2 - 14
2.11.2 Regulation with Varying Load . . . . . 2 - 16
2.11.3 Circuit Protection . . . . . 2 - 17
2.11.4 Design of Zener Regulator with Varying Load and Varying Input Conditions . . . . . 2 - 18
Examples with Solutions . . . . . 2 - 19
Review Questions . . . . . 2 - 26
Chapter - 3 Bipolar Junction Transistor (3 - 1) to (3 - 92)
3.1 Introduction . . . . . 3 - 1
3.2 Basic Construction . . . . . 3 - 2
3.3 Transistor Action . . . . . 3 - 3
3.3.1 Unbiased Transistor . . . . . 3 - 3
3.3.2 Biased Transistor . . . . . 3 - 4
3.3.3 Working of NPN Transistor . . . . . 3 - 5
3.3.4 Working of PNP Transistor . . . . . 3 - 6
3.3.5 Transistor Currents . . . . . 3 - 7
3.4 BJT Configurations . . . . . 3 - 9
3.4.1 Common Base Configuration . . . . . 3 - 9
3.4.1.1 Common Base Characteristics . . . . . 3 - 10
3.4.2 Common-Emitter Configuration . . . . . 3 - 14
3.4.2.1 Common Emitter Characteristics . . . . . 3 - 15
3.4.2.2 Definition of α_{dc} and β_{dc} . . . . . 3 - 18
3.4.2.3 Relationship between α_{dc} and β_{dc} . . . . . 3 - 18
3.4.3 Common Collector Configuration . . . . . 3 - 20
3.4.4 Why CE Configuration is Widely used in Amplifier Circuits ? . . . . . 3 - 21
3.4.5 Comparison of Transistor Configurations . . . . . 3 - 22
3.4.6 Leakage Current . . . . . 3 - 22
3.5 Biasing of Transistor . . . . . 3 - 25
3.5.1 Operating Point . . . . . 3 - 25
3.5.2 Need for Biasing BJT . . . . . 3 - 25

3.6 Fixed Bias Circuit....3 - 26
3.6.1 Circuit Analysis....3 - 26
3.6.2 Load Line and Quiescent Point....3 - 28
3.6.3 Selection of Operating Point....3 - 30
3.6.4 Typical Junction Voltages and Conditions for Operating Region....3 - 32
3.6.5 Variation of Quiescent Point....3 - 34
3.6.6 Advantages of Fixed Bias Circuit....3 - 37
3.6.7 Disadvantages of Fixed Bias Circuit....3 - 37
3.7 Stability Factors....3 - 39
3.7.1 Stability Factor S....3 - 39
3.8 Collector to Base Bias Circuit....3 - 43
3.8.1 Circuit Analysis....3 - 43
3.8.2 Modified Collector to Base Bias Circuit....3 - 45
3.9 Voltage Divider Bias / Self Bias Circuit....3 - 51
3.9.1 Circuit Analysis....3 - 52
3.9.2 Simplified Circuit of Voltage Divider Bias....3 - 52
3.10 Emitter Stabilized Bias Circuit....3 - 67
3.10.1 Circuit Analysis....3 - 68
3.10.2 Stability Improvement....3 - 70
3.11 Comparison of Biasing Circuits....3 - 72
Examples with Solutions....3 - 72
Review Questions....3 - 87
Chapter - 4 Transistor Amplifier (4 - 1) to (4 - 52)
4.1 Introduction....4 - 1
4.2 Graphical Analysis of CE Amplifier....4 - 1
4.3 H-Parameter Model....4 - 5
4.4 Analysis of Single Stage Transistor Amplifier using h-Parameters....4 - 10
4.5 Guidelines for Analysis of a Transistor Circuit....4 - 15
4.6 Analysis of Transistor Amplifier using Simplified Hybrid-Model....4 - 22
4.6.1 Analysis of Common Emitter Circuit using Simplified Hybrid Model....4 - 22
4.6.2 Analysis of Common Collector Circuit using Simplified Hybrid Model....4 - 25
4.7 Analysis of Common Emitter Amplifier with Collector to Base Bias....4 - 29
4.7.1 Miller's Theorem....4 - 31

4.8 Analysis of Common-Emitter Amplifier with an Emitter Resistance ....4 - 34
    4.8.1 Approximate Analysis . . . . 4 - 35
Examples with Solutions..4 - 38
Review Questions...4 - 50

Chapter - 5 Field Effect Transistor (5 - 1) to (5 - 70)

5.1 Introduction .... 5 - 1
5.2 Basic Construction .... 5 - 3
    5.2.1 Construction of n-channel JFET and Symbol . . . . 5 - 3
    5.2.2 Construction of p-channel JFET and Symbol . . . . 5 - 4
5.3 Transistor Action .... 5 - 4
    5.3.1 Unbiased JFET . . . . 5 - 4
    5.3.2 Principle of Operation of JFET . . . . 5 - 5
5.4 JFET V-I Characteristics .... 5 - 6
    5.4.1 Drain V-I Characteristics for n-channel JFET . . . . 5 - 7
    5.4.2 Drain / V-I Characteristics for p-channel JFET . . . . 5 - 10
    5.4.3 Transfer Characteristics for n-channel JFET . . . . 5 - 11
    5.4.4 Transfer Characteristics for p-channel JFET . . . . 5 - 13
5.5 JFET Parameters .... 5 - 13
    5.5.1 Transconductance . . . . 5 - 13
    5.5.2 Input Resistance and Capacitance . . . . 5 - 15
    5.5.3 Drain to Source Resistance . . . . 5 - 16
    5.5.4 Amplification Factor . . . . 5 - 16
5.6 Biasing of JFET .... 5 - 17
    5.6.1 Fixed Bias Circuit . . . . 5 - 17
    5.6.2 Voltage Divider Bias Circuit . . . . 5 - 18
    5.6.3 Self Bias Circuit . . . . 5 - 22
    5.6.4 Graphical Solution for Self Bias . . . . 5 - 24
    5.6.5 Biasing for Zero Current Drift . . . . 5 - 27
    5.6.6 Biasing against Device Variation . . . . 5 - 30
    5.6.7 Use of JFET as a VVR or VDR . . . . 5 - 33
5.7 MOSFETs .... 5 - 34
    5.7.1 Depletion MOSFET (D-MOSFET) . . . . 5 - 34
        5.7.1.1 Construction of n-channel MOSFET . . . . 5 - 34
        5.7.1.2 Operation, Characteristics and Parameters of n-channel MOSFET . . . . 5 - 34

5.7.1.3 P-channel Depletion Type MOSFET : . . . . 5 - 37
5.7.1.4 D-MOSFET Symbols . . . . 5 - 37
5.7.2 Enhancement MOSFET (E-MOSFET) . . . . 5 - 38
5.7.2.1 Construction of n-channel E-MOSFET . . . . 5 - 38
5.7.2.2 Operation, Characteristics and Parameters of n-channel E-MOSFET . . . . 5 - 39
5.7.2.3 P-channel Enhancement Type MOSFET . . . . 5 - 41
5.8 JFET Amplifiers .... 5 - 42
5.8.1 JFET Low Frequency Small Signal Model . . . . 5 - 44
5.8.2 Common Source (CS) Amplifier . . . . 5 - 45
5.8.2.1 JFET with Fixed Bias . . . . 5 - 45
5.8.2.2 JFET with Self Bias (Bypassed R_s) . . . . 5 - 49
5.8.2.3 JFET with Self Bias (Unbypassed R_s) . . . . 5 - 50
5.8.2.4 JFET with Voltage Divider Bias (Bypassed R_s). . . . . 5 - 55
5.8.2.5 JFET with Voltage Divider Bias (Unbypassed R_s). . . . . 5 - 56
5.8.3 Common Drain (CD) Amplifier . . . . 5 - 59
5.8.4 Common Gate (CG) Amplifier . . . . 5 - 62
5.9 Comparison between BJT, JFET and MOSFET .... 5 - 66
5.9.1 Comparison of BJT and FET . . . . 5 - 66
5.9.2 Comparison of JFET and MOSFET . . . . 5 - 67
5.9.3 Comparison of D-MOSFET and E-MOSFET . . . . 5 - 68
Review Questions .... 5 - 69

Chapter - 6 Operational Amplifiers (6 - 1) to (6 - 58)

6.1 Introduction .... 6 - 1
6.2 Op-Amp Symbol and Terminals .... 6 - 1
6.2.1 Power Supply . . . . 6 - 3
6.3 Ideal Op-Amp .... 6 - 3
6.3.1 Ideal Differential Amplifier. . . . . 6 - 3
6.3.2 Differential Gain A_d . . . . 6 - 4
6.3.3 Common Mode Gain A_c . . . . 6 - 4
6.3.4 Common Mode Rejection Ratio (CMRR) . . . . 6 - 5
6.4 Ideal Op-Amp Characteristics .... 6 - 7
6.5 Saturable Property of Op-Amp .... 6 - 9
6.5.1 Comparator. . . . . 6 - 10

6.6 Ideal Voltage Transfer Curve .... 6 - 11
6.7 Equivalent Circuit of Practical Op-Amp .... 6 - 12
  6.7.1 Practical Op-Amp Characteristics .... 6 - 13
6.8 Other Important Op-Amp Parameters .... 6 - 16
  6.8.1 Power Supply Rejection Ratio .... 6 - 16
  6.8.2 Slew Rate .... 6 - 16
6.9 Block Diagram of IC Op-Amp .... 6 - 17
  6.9.1 Input Stage .... 6 - 17
  6.9.2 Intermediate Stage .... 6 - 18
  6.9.3 Level Shifting Stage .... 6 - 18
  6.9.4 Output Stage .... 6 - 18
6.10 Op-Amp IC 741 .... 6 - 18
  6.10.1 Pin Diagram .... 6 - 19
  6.10.2 Ideal Vs Practical Characteristics of IC 741 Op-Amp .... 6 - 19
  6.10.3 Features of IC 741 .... 6 - 20
6.11 Open Loop Configuration of Op-Amp .... 6 - 20
6.12 Closed Loop Configuration of Op-Amp .... 6 - 21
  6.12.1 Advantages of Negative Feedback .... 6 - 21
6.13 Realistic Simplifying Assumptions .... 6 - 21
  6.13.1 Zero Input Current .... 6 - 22
  6.13.2 Virtual Ground .... 6 - 22
6.14 Op-Amp Applications .... 6 - 23
6.15 Inverting Amplifier .... 6 - 23
6.16 Noninverting Amplifier .... 6 - 27
6.17 Important Point about Noninverting Amplifier .... 6 - 30
6.18 Voltage Follower (Unity Gain Amplifier) .... 6 - 33
  6.18.1 Advantages of Voltage Follower .... 6 - 34
  6.18.2 Practical use of Voltage Follower .... 6 - 35
6.19 Summer or Adder Circuit .... 6 - 36
  6.19.1 Inverting Summer .... 6 - 36
  6.19.2 Noninverting Summing Amplifier .... 6 - 37
  6.19.3 Average Circuit .... 6 - 38

6.20 Subtractor or Difference Amplifier .... 6 - 42
6.21 Integrator .... 6 - 44
  6.21.1 Ideal Active Op-Amp Integrator .... 6 - 45
  6.21.2 Input and Output Waveforms .... 6 - 46
  6.21.3 Applications of Practical Integrator .... 6 - 48
6.22 Differentiator .... 6 - 49
  6.22.1 Ideal Active Op-Amp Differentiator .... 6 - 49
  6.22.2 Input and Output Waveforms .... 6 - 51
  6.22.3 Applications of Practical Differentiator .... 6 - 54
Examples with Solutions .... 6 - 54
Review Questions .... 6 - 56

Chapter - 7 Switching Theory and Logic Design (7 - 1) to (7 - 152)

7.1 Number Systems .... 7 - 1
  7.1.1 Decimal Number System .... 7 - 1
  7.1.2 Binary Number System .... 7 - 2
  7.1.3 Octal Number System .... 7 - 3
  7.1.4 Hexadecimal Number System .... 7 - 3
  7.1.5 Counting in Radix (Base) r .... 7 - 5
7.2 Conversion of Base .... 7 - 6
  7.2.1 Binary to Octal Conversion .... 7 - 6
  7.2.2 Octal to Binary Conversion .... 7 - 7
  7.2.3 Binary to Hexadecimal Conversion .... 7 - 7
  7.2.4 Hexadecimal to Binary Conversion .... 7 - 8
  7.2.5 Octal to Hexadecimal Conversion .... 7 - 8
  7.2.6 Hexadecimal to Octal Conversion .... 7 - 9
  7.2.7 Converting any Radix to Decimal .... 7 - 9
  7.2.8 Conversion of Decimal Numbers to any Radix Number .... 7 - 10
7.3 Complements .... 7 - 17
  7.3.1 1's Complement Representation .... 7 - 17
  7.3.2 2's Complement Representation .... 7 - 17
7.4 Sign Extension .... 7 - 19
7.5 Addition Subtraction .... 7 - 20
  7.5.1 Binary Arithmetic .... 7 - 20
    7.5.1.1 Binary Arithmetic - Negative Numbers in 1's Complement Form .... 7 - 20

7.5.1.2 Binary Arithmetic-Negative Numbers in 2's Complement Form . . . . 7 - 22
7.5.2 Octal Arithmetic . . . . 7 - 24
7.5.3 Hexadecimal Arithmetic . . . . 7 - 27
7.5.3.1 Addition . . . . 7 - 27
7.5.3.2 Subtraction . . . . 7 - 28
7.6 BCD (8-4-2-1) . . . . 7 - 32
7.6.1 BCD Addition . . . . 7 - 33
7.6.2 BCD Subtraction . . . . 7 - 36
7.7 Other 4-Bit BCD Codes . . . . 7 - 39
7.7.1 2-4-2-1 Code . . . . 7 - 39
7.7.2 Other Codes . . . . 7 - 40
7.8 Excess-3 Code . . . . 7 - 40
7.8.1 Excess-3 Addition . . . . 7 - 41
7.8.2 Excess-3 Subtraction . . . . 7 - 42
7.8.3 Exess-3 Substraction using 9's Complement . . . . 7 - 44
7.9 Gray Code . . . . 7 - 46
7.9.1 Advantage of Gray Code . . . . 7 - 47
7.9.2 Gray-to-Binary Conversion . . . . 7 - 47
7.9.3 Binary to Gray Conversion . . . . 7 - 48
7.10 Five Bit Codes . . . . 7 - 48
7.11 Character Codes (Alphanumeric Codes) . . . . 7 - 49
7.11.1 ASCII . . . . 7 - 49
7.11.2 EBCDIC 7- 51
7.11.3 Hollerith Code 7- 52
7.12 Boolean Algebra 7- 54
7.12.1 Fundamental Postulates of Boolean Algebra 7- 55
7.12.2 Laws of Boolean Algebra 7- 56
7.12.3 Basic Theorems and Properties 7- 58
7.12.3.1 Duality 7- 58
7.12.3.2 Basic Theorems 7- 58
7.12.3.3 DeMorgan's Theorems 7- 62
7.12.3.4 Consensus Theorem 7- 63
7.12.3.5 Dual of Consensus Theorem 7- 63
7.13 Logic Gates 7- 64
7.13.1 NOT Gate (Inverter) 7- 64
7.13.2 AND Gate 7- 65

7.13.3 OR Gate . . . 7-67
7.13.4 The Exclusive-OR Gate . . . 7-69
7.13.5 The Exclusive-NOR Gate . . . 7-70
7.13.6 Properties of Exclusive - OR Gate . . . 7-71
7.14 Concept of Universal Gate . . . 7-73
7.14.1 NAND Gate . . . 7-73
7.14.2 NOR Gate . . . 7-74
7.14.3 Implementation of NOT, AND, OR and NOR Functions using NAND Gate . . . 7-75
7.14.4 Implementation of NOT, AND, OR and NAND Functions using NOR Gate . . . 7-77
7.15 Switching Functions / Boolean Functions . . . 7 - 81
7.15.1 Sum of Product Form . . . 7 - 82
7.15.2 Product of Sum Form . . . 7 - 83
7.16 Canonical Forms (Standard SOP and POS Forms) . . . 7 - 83
7.16.1 Standard POS Form or Minterm Canonical Form . . . 7 - 83
7.16.2 Standard POS Form or Maxterm Canonical Form . . . 7 - 84
7.16.3 Converting Expressions in Standard SOP or POS Forms . . . 7 - 84
7.16.4 M-Notations : Minterms and Maxterms . . . 7 - 88
7.16.5 Complements of Canonical Formulae . . . 7 - 90
7.17 Minimization using K-map . . . 7 - 91
7.17.1 One-Variable, Two-Variable, Three-Variable and Four-Variable Maps . . . 7 - 91
7.17.2 Plotting a Karnaugh Map . . . 7 - 93
7.17.2.1 Representation of Truth Table on Karnaugh Map . . . 7 - 94
7.17.2.2 Representing Standard SOP on K-map . . . 7 - 95
7.17.2.3 Representing Standard POS on K-map . . . 7 - 96
7.17.3 Grouping Cells for Simplification . . . 7 - 97
7.17.3.1 Grouping Two Adjacent Ones (Pair) . . . 7 - 97
7.17.3.2 Grouping Four Adjacent Ones (Quad) . . . 7 - 100
7.17.3.3 Grouping Eight Adjacent Ones (Octet) . . . 7 - 102
7.17.4 Simplification of Sum of Products Expressions (Minimal Sums) . . . 7 - 103
7.17.5 Essential Prime Implicants . . . 7 - 112
7.17.6 Simplification of Product of Sums Expressions (Minimal Products) . . . 7 - 112
7.18 Don't Care Conditions . . . 7 - 117
7.18.1 Describing Incomplete Boolean Function . . . 7 - 118
7.18.2 Don't Care Conditions in Logic Design . . . 7 - 118

7.19 Minimization of Incompletely Specified Function ....7 - 119
Solved Examples ....7 - 122
Review Questions ....7 - 148

Chapter - 8 Electronic Instruments (8 - 1) to (8 - 32)

8.1 Introduction .... 8 - 1
8.2 Digital Voltmeters .... 8 - 1
8.3 Advantages of Digital Voltmeters .... 8 - 2
8.4 Performance Parameters of Digital Voltmeters .... 8 - 2
8.5 Basic Block Diagram of DVM .... 8 - 3
8.6 Classification of Digital Voltmeters .... 8 - 4
8.7 Digital Multimeters .... 8 - 4
8.8 Specifications of Digital Multimeter .... 8 - 6
8.9 Introduction to C.R.O. .... 8 - 8
8.10 Cathode Ray Tube (CRT) .... 8 - 8
  8.10.1 Electron Gun .... 8 - 9
  8.10.2 Deflection System .... 8 - 10
  8.10.3 Fluorescent Screen .... 8 - 11
  8.10.4 Glass Tube .... 8 - 14
  8.10.5 Base .... 8 - 14
8.11 Basic Principle of Signal Display .... 8 - 14
8.12 Block Diagram of Simple Oscilloscope .... 8 - 16
  8.12.1 CRT .... 8 - 16
  8.12.2 Vertical Amplifier .... 8 - 16
  8.12.3 Delay Line .... 8 - 17
  8.12.4 Trigger Circuit .... 8 - 19
  8.12.5 Time Base Generator .... 8 - 19
  8.12.6 Horizontal Amplifier .... 8 - 19
  8.12.7 Power Supply .... 8 - 19
8.13 Front Panel Controls of Simple C.R.O. .... 8 - 20
  8.13.1 Basic Controls .... 8 - 20
  8.13.2 Vertical Section .... 8 - 21
  8.13.3 Horizontal Section .... 8 - 23
  8.13.4 Z-Axis Intensity Control .... 8 - 24

8.14 C.R.O. Measurements .... 8 - 24

8.14.1 Voltage Measurement .... 8 - 24

8.14.2 Current Measurement .... 8 - 25

8.14.3 Period and Frequency Measurement .... 8 - 26

8.14.4 Need of C.R.O. in Electronic Practicals .... 8 - 26

8.15 Lissajous Figures .... 8 - 26

8.15.1 Measurement of Phase Difference .... 8 - 27

8.15.2 Measurement of Frequency .... 8 - 28

8.16 Applications of C.R.O. .... 8 - 29

Review Questions .... 8 - 31

1

Semiconductor Diodes and Applications

1.1 Introduction

The materials such as copper, aluminium etc. are good **conductors** of electricity. While the materials such as wood, glass, mica etc. are very bad conductors of electricity and are called **insulators**. There is another class of materials, whose conductivity i.e. ability to carry electricity, lies between that of conductors and insulators. Such materials are called **semiconductors**. Germanium (Ge) and Silicon (Si) are two well known semiconductor materials.

Alongwith these two basic semiconductor materials, some impurities are used to obtain extrinsic semiconductor materials called n-type and p-type. These two materials are then chemically combined to obtain p-n junction. Such a semiconductor p-n junction forms a popular electronic device called diode. This chapter explains the diode characterstics and some applications of the diode.

1.2 The Structure of Matter

The matter which occupies the space may be solid, liquid or gaseous. The molecules and atoms, of which all the substances are composed, are not at all elements but are themselves made up of simpler entities. We know this because, we, up to certain extent, are successful in breaking atoms and studying the resulting products. For instance, such particles of atom are obtained by causing ultraviolet light to fall on cold metal surfaces, such particles are spontaneously ejected from the radioactive elements. So such particles are obtained from many different substances under widely varying conditions.

In fact, according to the modern electron theory, matter is composed of the three fundamental particles, which are invisible to bare eyes. These are the **neutron**, the **proton** and the **electron**. The proton is positively charged and the electron is negatively charged. The neutron is uncharged i.e. electrically neutral in nature possessing no charge. The mass of neutron and proton is same while the electron is very light, almost $1/1840^{th}$ the mass of neutron. The following table gives the information about these three particles.

Fundamental particle	Nature of charge	Mass in kg
Neutron	No charge	1675×10^{-27}
Proton	Positive	1672×10^{-27}
Electron	Negative	9.107×10^{-31}

Table 1.1

There is no difference between an electron of copper and an electron of aluminium or an electron of any other element. Similarly the neutrons and protons of various atoms are characteristicwise identical in nature. Then why do various elements behave differently ? This is because of the difference in the arrangement of electrons, protons and neutrons of which each atom is composed. Let us see the structure of an atom.

1.2.1 Structure of an Atom

The atoms have a planetary type of structure, according to classical **Bohr Model.**

All the protons and neutrons are bound together at the centre of an atom, which is called Nucleus. While all the electrons are moving round the nucleus. So nucleus can be thought of as a central sun, about which electrons revolve in a particular fashion like the planets.

In a normal atom the number of protons is equal to the number of electrons. As neutron is electrically neutral, an atom as a whole is electrically neutral. The number of protons in an atom is called as its **atomic number.** While the atomic weight is approximately equal to the total number of protons and neutrons in the nucleus of an atom.

The electrons which are revolving round the nucleus, do not move in the same orbit. The electrons are arranged in the different **orbits** or **shells** at fixed distances from the nucleus. Each shell can contain a fixed number of electrons. In general, a shell can contain a maximum of $\mathbf{2n^2}$ electrons where n is the number of the shell. The first shell can occupy maximum of two electrons (2×1^2) while the second shell can occupy maximum of eight electrons (2×2^2) and so on.

Each shell has an energy level associated with it. The closer an electron is to the nucleus, the stronger are the forces that bind it to the nucleus. So the first shell which is closest to the nucleus is always under the tremendous force of attraction. While the shell which is farthest from the nucleus is under very weak force of attraction. The electrons revolving in the last shell i.e. farthest from the nucleus are very loosely bound to the nucleus. Such electrons in the outermost shell are responsible for the electrical and chemical characteristics of an atom.

Key Point : *The outermost shell is called the* ***valence shell*** *and the electrons in this shell are called* ***valence electrons.***

The exception to the '$2n^2$' rule stated above is that the outermost shell in an atom cannot accommodate more than eight electrons. The valence electrons revolving in the outermost shell are said to be having highest energy level. **The amount of energy required to extract the valence electron from the outer shell is very less.**

Key Point :*Each shell has* ***energy level*** *associated with it. Closer the shell to the nucleus, more tightly it is bound the the nucleus and possesses lower energy level.*

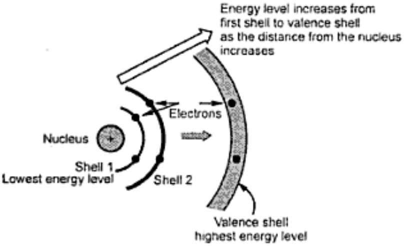

Energy level increases from first shell to valence shell as the distance from the nucleus increases
Electrons
Nucleus
Shell 1
Lowest energy level
Shell 2
Valence shell
highest energy level

Fig. 1.1 Concept of energy level

Thus energy level of shell one is lowermost while the energy level of valence shell is highest. More energy level indicates that the electrons of that shell are loosely bound to the nucleus. Hence valence electrons are loosely bound to the nucleus as having highest energy level. The concept of energy level is shown in the Fig. 1.1

When an atom absorbs energy from a heat source or from light or due to high atmospheric temperature, the energy levels of the electrons are raised. When such an additional energy is imparted to the electrons, the electrons move to the next orbit which is farther from the nucleus. If such an energy is imparted to a valence electron, it tries to jump to the next orbit. But as a valence electron is in the outermost orbit, actually it gets completely removed from the force of attraction of the nucleus.

Key Points:

1) *An electron which is not subjected to the force of attraction of the nucleus is called* ***a free electron****. Such free electrons are basically responsible to the flow of current.*

2) *More the number of free electrons, better is the conductivity of the metal.*

1.3 Group - IV Materials (Semiconductor Materials)

In the periodic table, the various elements are arranged according to the number of valence electrons. The elements having four valence electrons are called **tetravalent** elements and are classified as **Group - IV elements** in the periodic table. These are called semiconductor materials. The examples of such materials are germanium (Ge) and Silicon (Si). The materials having three valence electrons are called trivalent and classified as Group-III materials. The examples of trivalent materials are Boron (B), Gallium (Ga) etc. While the materials having five valence electrons are called pentavalent materials and classified as Group-V materials. The examples of pentavalent materials are Phosphorous (P), Arsenic (As) etc.

The table shows the part of periodic table indicating semiconductor materials.

Group →	III	IV	V
	B	Si	P
	Ga	Ge	As

Semiconductor materials

Table 1.2

Let us see the structure of these important semiconductor materials.

1.3.1 Structure of Semiconductor Materials

The semiconductor materials such as Ge and Si have four electrons in their valence shell i.e. outermost shell. The Fig. 1.2 shows atomic structure of the semiconductor materials, germanium and silicon.

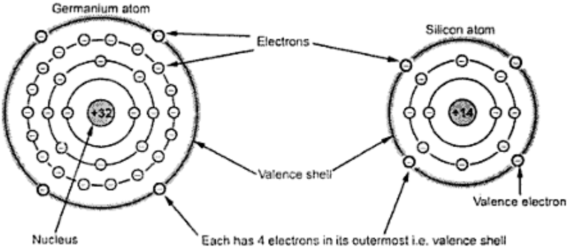

Germanium atom
Silicon atom
Electrons
+32
+14
Valence shell
Valence electron
Nucleus
Each has 4 electrons in its outermost i.e. valence shell

Fig. 1.2 Atomic structure of germanium and silicon atoms

The germanium has a nucleus with 32 protons. The electrons are distributed as follows : 2 electrons in the first orbit, 8 in the second orbit, and 18 in the third. The remaining four electrons are in the outer or valence orbit.

The silicon has nucleus with 14 protons and 14 electrons. As shown in Fig. 1.2 the first orbit contains 2 and the second orbit contains 8 electrons. The remaining four electrons are in the outermost orbit.

Key Point: *When there are four electrons in the outermost orbit, the semiconductor material is referred to as pure or intrinsic semiconductor.*

These intrinsic matrials can be manufactured to a very high purity level. The impurity levels are of the order of 1 part in 10 billion.

1.3.1.1 Properties of Intrinsic Materials

The important properties of such intrinsic semiconductor materials are,

1. High purity level.
2. The characteristics can be changed as per the requirement by the process of adding impurity called doping.
3. The characteristics can be changed significantly by the application of heat and light.
4. Most suitable for heat sensitive and light sensitive devices.

1.4 Ionization

If an electron is extracted from the outermost shell of an atom then the overall negative charge of that atom decreases as it looses negative charge in the form of an electron. But the number of protons remains same hence positive charge remains same. So atom as a whole looses its electrical neutral nature and becomes positively charged. Such an atom is called **positive ion.** Similarly by any means if an electrically neutral atom gains an additional electron then it becomes negatively charged and called **negative ion.** Thus by loosing or gaining electrons, an atom gets converted into a charged ion. This process of loosing or gaining an electron, which converts electrically neutral atom to a charged ion is called **ionization.**

1.5 The Energy-Band Theory

We have seen that every shell is associated with an energy level. An electron orbiting very close to the nucleus in the first shell is very much tightly bound to the nucleus and possesses only a small amount of energy. Hence first shell has lowest energy level. Greater the distance of an electron from the nucleus, the greater is its energy. Hence the energy level of the outermost shell is highest. Due to such high energy, the valence electrons in the outermost shell can be easily extracted out and hence such electrons take part in chemical reactions and in bonding the atoms together. Now this discussion is related to the electrons and shells of one isolated atom only.

In solids, atoms are brought close together. In such a case, outer shell electrons are shared by more than one atom. So these electrons come under the influence of forces from other atoms too. The valence electrons are shared by forming a bond with the valence electrons of an adjacent atom. Such bonds are called **covalent bonds**. Thus the valence electrons are not free under normal conditions, as they are shared by the adjacent atoms.

Now the valence electrons possess highest energy level. When such electrons form the covalent bonds, due to the coupling between the valence electrons, the energy levels associated with the valence electrons merge into each other. This merging forms an **energy band.**

Similarly the energy levels of various electrons present in the first orbit, second orbit etc. also merge to form the various energy bands.

So instead of the presence of widely separated energy levels as that of the isolated atoms, the closely spaced energy levels are present in a solid, which are called energy bands.

Out of all the energy bands, three bands are most important to understand the behaviour of solids. These bands are,

1] Valence band, 2] Conduction band, 3] Forbidden band or gap

> **Key Point** : *The energy band formed due to merging of energy levels associated with the valence electrons i.e. electrons in the last shell, is called* ***valence band.***

As mentioned earlier in normal condition, valence electrons form the covalent bonds and are not free. But when certain energy is imparted to them, they become free.

> **Key Point** : *The energy band formed due to merging of energy levels associated with the free electrons is called* ***conduction band.***

Under normal condition, the conduction band is empty and once energy is imparted, the valence electrons jump from valence band to conduction band and become free.

While jumping from valence band to conduction band, the electrons have to cross an energy gap.

> **Key Point** : *The energy gap which is present separating the conduction band and the valence band is called* ***forbidden band or forbidden gap.***

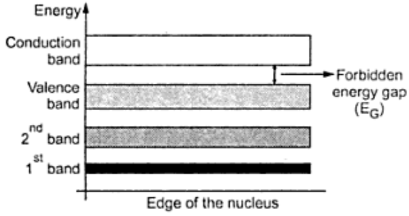


Fig. 1.3 Energy band diagram

The energy imparted to the electrons must be greater than the energy associated with the forbidden gap, to extract the electrons from valence band and transfer them to conduction band. The energy associated with forbidden band is denoted as E_G.

Key Point : *The electrons cannot exist in the forbidden gap.*

The graphical representation of the energy bands in a solid is called **energy band diagram.** Such an energy band diagram for a solid silicon is shown in the Fig. 1.3.

The electrons in the various orbits revolving around the nucleus occupy the various bands including fully or partly occupied valence band. The conduction band which is normally empty carries the electrons which get drifted from the valence band. These electrons present in the conduction band are free electrons and they drift about in the spaces between the atoms.

For any given type of material the forbidden energy gap may be large, small or nonexistent. The classification of materials as insulators, conductors or semiconductors is mainly dependent on the widths of the forbidden energy gap. Let us see the classification of materials as insulators, conductors and semiconductors based on energy band diagram. Before that let us see the unit in which energy associated with the bands is measured.

1.5.1 The eV, Unit of Energy

The energy is measured in joules (J) in the M.K.S. system. As mentioned earlier, each electron has an energy level associated with it. The unit joule is very large for the discussion of such energies associated with electrons. Hence such energies associated with the electrons are measured in electron volts denoted as eV.

The charge on a single electron is 1.6×10^{-19} coulomb. So one **electron volt is defined as the energy required by an electron to fall through a potential of one volt.**

$$\therefore \quad 1 \text{ eV} = 1.6 \times 10^{-19} \text{ (C)} \times 1 \text{ (V)} = 1.6 \times 10^{-19} \text{ J}$$

$$\therefore \quad \boxed{1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}}$$

1.6 Classification of Materials Based on Energy Band Theory

Based on the ability of various materials to conduct current, the materials are classified as conductors, insulators and the semiconductors.

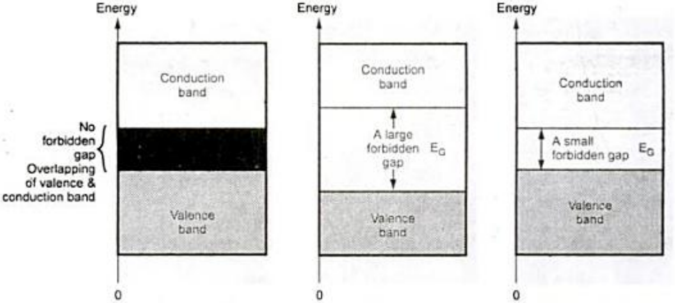
A metal which is very good carrier of electricity is called conductor. A very poor conductor of electricity is termed as insulator. A metal having conductivity which is between conductor and an insulator is called semiconductor. Copper and aluminium are good examples of a conductor. Glass, wood, mica, diamond are the examples of an insulator which do not conduct current. Silicon and germanium are the examples of a semiconductor which do not conduct current at low temperatures but as temperature increases these materials behave as good conductors. Let us see the energy band diagrams for these three types of metals.

1.6.1 Conductors

It has been mentioned earlier that a material having large number of free electrons can conduct very easily. For example, copper has 8.5×10^{28} free electrons per cubic metre which is a very large number. Hence copper is called good conductor. In fact, in metals like copper, aluminium there is no forbidden gap between valence band and conduction band. **The two bands overlap.** Hence even at room temperature, a large number of electrons are available for conduction. So without any additional energy, such metals contain a large number of free electrons and hence called good **conductors.** An energy band diagram for a conductor is shown in the Fig. 1.4 (a).

1.6.2 Insulators

An insulator has an energy band diagram as shown in the Fig. 1.4 (b). In case of such insulating material, there exists a large forbidden gap in between the conduction band and the valence band. Practically it is impossible for an electron to jump from the valence band to the conduction band. Hence such materials cannot conduct and are called **insulators.** The forbidden gap is very wide, approximately of about 7 eV is present in insulators. For a diamond, which is an insulator, the forbidden gap is about 6 eV. Such materials may conduct only at very high temperatures or if they are subjected to high voltage. Such a conduction is rare and is called breakdown of an insulator. The other insulating materials are glass, wood, mica, paper etc.


Energy
Conduction band
No forbidden gap
Overlapping of valence & conduction band
Valence band
0
Energy
Conduction band
A large forbidden gap
E_G
Valence band
0
Energy
Conduction band
A small forbidden gap
E_G
Valence band
0

(a) Conductor **(b) Insulator** **(c) Semiconductor**

Fig. 1.4 Energy band diagrams

1.6.3 Semiconductors

Now let us come to an important category of materials, which are neither insulators nor conductors. The forbidden gap in such materials is very narrow as shown in Fig. 1.4 (c). Such materials are called **semiconductors.** The forbidden gap is about 1 eV. In such materials, the energy provided by the heat at room temperature is sufficient to lift the electrons from the valence band to the conduction band. Therefore at room temperature, semiconductors are capable of conduction. But at 0 °K or absolute zero (– 273° C), all the electrons of semiconductor materials find themselves locked in the valence band. Hence at 0 °K, the semiconductor materials behave as perfect insulators. In case of semiconductors, forbidden gap energy depends on the temperature. For silicon and germanium, this energy is given by,

$$\boxed{\begin{aligned} E_G &= 1.21 - 3.6 \times 10^{-4} \times T \quad \text{eV (for Silicon)} \\ E_G &= 0.785 - 2.23 \times 10^{-4} \times T \quad \text{eV (for Germanium)} \end{aligned}}$$

where T = Absolute temperature in °K

Assuming room temperature to be 27 °C i.e. 300 °K, the forbidden gap energy for Si and Ge can be calculated from the above equations. The forbidden gap for the germanium is 0.72 eV while for the silicon it is 1.12 eV at room temperature. The silicon and germanium are the two widely used semiconductor materials in electronic devices, as mentioned earlier.

Key Point : *While calculating* E_G, *substitute* T *in °K.*

Why silicon is most widely used ?

Looking at the structure of silicon and germanium atom, it can be seen that valence shell of silicion is 3^{rd} shell while valence shell of germanium is 4^{th} shell. Hence valence electrons of germanium are at larger distance from nucleus than valence electrons of silicon. Hence valence electrons of germanium are more loosely bound to the nucleus than those of silicon. Thus valence electrons of germanium can easily escape from the atom, due to very small additional energy imparted to them. So at high temperature, germanium becomes unstable than silicon and and hence silicon is widely used as semiconductor material.

1.7 Intrinsic Semiconductors

A sample of semiconductor in its purest form is called an **intrinsic semiconductor**. The impurity content in intrinsic semiconductor is very very small, of the order of one part in 100 million parts of semiconductor. For achieving such a pure form, the semiconductor materials are carefully refined. To understand the conduction in an intrinsic semiconductor let us study the crystalline structure of an intrinsic semiconductor.

1.7.1 Crystal Structure of Intrinsic Semiconductor

Consider an atomic structure of an intrinsic semiconductor material like silicon. An outermost shell of an atom is capable of holding eight electrons. It is said to be completely filled and stable, if it contains eight electrons. But the outermost shell of an intrinsic semiconductor like silicon has only four electrons. Each of these four electrons form a bond with another valence electron of the neighbouring atoms. This is nothing but sharing of electrons. Such bonds are called **covalent bonds**. The atoms align themselves to form a three dimensional uniform pattern called a **crystal**.

The crystal structure of germanium and silicon materials consists of repetitive occurrence in three dimensions of a unit cell. This unit cell is in the form of a tetrahedron with an atom at each vertex. But such a three dimensional structure is very difficult to

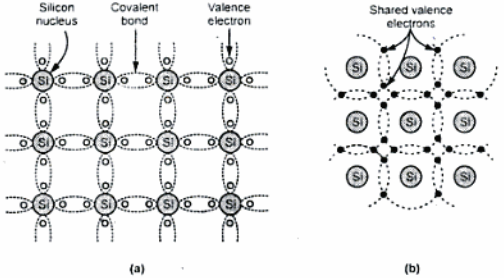

Silicon nucleus
Covalent bond
Valence electron
Si
Shared valence electrons
(a)
(b)

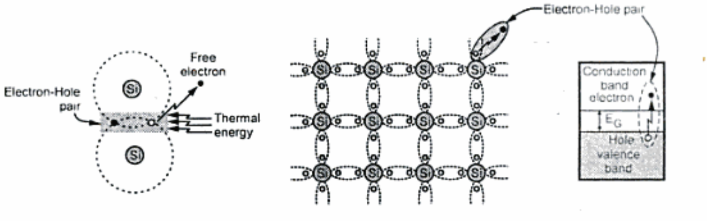
Fig. 1.5 Two dimensional representation of silicon crystal

represent pictorially. Hence a symbolic two dimensional structure is used to represent a three dimensional crystal form, as shown in the Fig.1.5(a).

The covalent bonds are represented by a pair of dotted lines encircling the two electrons forming the covalent bond. The more clear understanding of the covalent bonds can be obtained from the Fig. 1.5 (b) which shows the sharing of valence electrons. Both the electrons are shared by the two atoms. Hence the outermost shell of all the atoms is completely filled, and the valence electrons are tightly bound to the parent atoms. No free electrons are available at absolute zero temperature. **Hence such an intrinsic semiconductor behaves as a perfect insulator at absolute zero temperature.**

1.7.2 Charge Carriers in Intrinsic Semiconductors

Intrinsic semiconductors behave as a perfect insulator at absolute zero temperature. Let us see what happens at room temperature. At room temperature, the number of valence electrons absorb the thermal energy, due to which they break the covalent bond and drift to the conduction band. Such electrons become free to move in the crystal as shown in the Fig. 1.6 (a).


Free electron
Electron-Hole pair
Thermal energy
Si
Electron-Hole pair
Conduction band electron
E_G
Hole valence band

(a) Breaking of covalent bond (b) Electron-hole pair in a silicon crystal (c) Energy band diagram

Fig. 1.6 Thermal generation

Once the electrons are dislodged from the covalent bonds, then they become free. Such free electrons wander in a random fashion in a crystal. The energy required to break a covalent bond is 0.72 eV for germanium and 1.1 eV for silicon, at room temperature.

When a valence electron drifts from valence to conduction band breaking a covalent bond, a vacancy is created in the broken covalent bond. Such a vacancy is called a **hole**. Whenever an electron becomes free, the corresponding hole gets generated.

So free electrons and holes get generated in pairs. The formation of electron-hole pair is shown in the Fig. 1.6 (b) while the corresponding energy band diagram is shown in the Fig. 1.6 (c). Such a generation of electron hole pairs due to thermal energy is called **thermal generation.**

The concentration of free electrons and holes is always equal in an intrinsic semiconductor. The hole also serves as a carrier of electricity similar to that of free electron. **An electron is negatively charged particle. Thus a hole getting created due to electron drift is said to be positively charged.**

Key Point : *Thus in an intrinsic semiconductors both holes as well as free electrons are the charge carriers.*

1.7.3 Conduction by Electrons and Holes

The electrons and holes generated due to thermal generation move randomly and hence cannot constitute any current. Now consider that battery is connected across the intrinsic semiconductor.

Under the influence of applied voltage there is electron as well as hole motion in one particular direction, causing the flow of current.

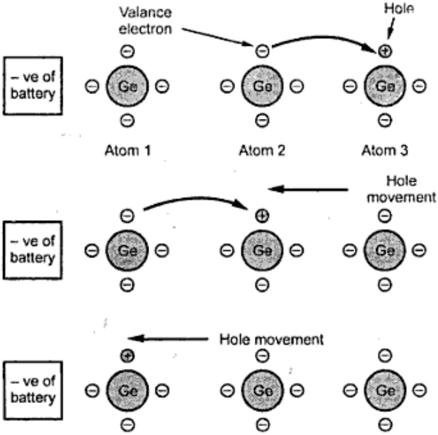


Fig. 1.7 Hole current

The free electrons which are available in the conduction band are moved under the influence of applied voltage. The electrons as negatively charged get repelled from the negative terminal of battery and attracted towards the positive terminal. Thus there is an electric current due to the movement of electrons in conduction band. This is called **electron current** .

There are electrons present in the valence band which are involved in forming the covalent bonds. Some holes are also present in the valence band due to escape of electrons from valence to conduction band. Under the influence of applied voltage, the electrons involved in covalent bonds break the covalent bonds and try to fill the holes present. The electron breaking the covalent bond jumps to the hole of neighbouring atom, leaving a hole behind. This is illustrated in the Fig. 1.7 (a), (b) and (c).

The atom x has a hole due to escape of an electron to the conduction band. The electron from atom y breaks its covalent bond and fill the hole of atom x. Now the hole is left in the valence shell of atom y. An electron from atom z jumps to fill the hole in atom y. The hole in y gets filled but a hole is left in the valence shell of atom z. Thus the hole moves from atom x to y to z and so on towards the negative terminal of battery.

Such a movement of holes in valence band constitute the current which is called **hole current**. The direction of motion of holes is in the opposite direction to that of electrons.

> **Key Point** : *The current due to movement of free electrons in the conduction band is an electron current. The current due to movement of holes in the valence band is a hole current. The electron as well as hole current together constitutes current in an intrinsic semiconductor.*

The movement of hole and electron can also be shown as in the Fig. 1.8.

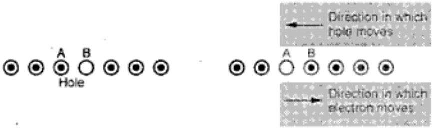

A
B
Hole
Direction in which hole moves
A
B
Direction in which electron moves

Fig. 1.8 Movement of hole

The electron from atom A jumps to B to fill the hole at B. And the hole gets created at A. Thus holes moves from B to A.

Thus the conduction of an electric current is due to the movement of electrons in the conduction band and holes in the valence band.

$$\boxed{\textbf{Total current = Electron current + Hole current}} \quad \dots (1)$$

1.7.4 Conduction in Intrinsic Semiconductors

In earlier sections, we have seen that the free electrons and holes are the two types of charge carriers in the intrinsic semiconductors. But the random motion of these carriers do not constitute any current.

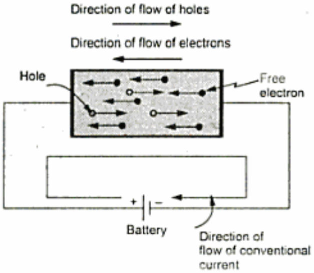

Direction of flow of holes
Direction of flow of electrons
Hole
Free electron
Battery
Direction of flow of conventional current

Fig. 1.9 Conduction in intrinsic semiconductor

Let us now consider that a battery is connected across an intrinsic semiconductor. The free electrons as negatively charged experience a force towards the positive terminal of the battery while the holes as positively charged experience a force towards negative terminal of the battery. This is shown in the Fig. 1.9.

Key Point : *The direction of current flow from positive to negative terminal of the battery is referred as the conventional current direction.*

Electron flow from negative to positive is known as the direction of electron flow. Every symbol used to represent an electronic device has an arrowhead which indicates conventional current direction. However, the operation of electronic devices is explained with the help of the electron movement.

1.8 Extrinsic Semiconductors

In order to change the properties of intrinsic semiconductors a small amount of some other material is added to it. The process of adding other material to the crystal of intrinsic semiconductors to improve its conductivity is called **doping**. The impurity added is called **dopant**. Doped semiconductor material is called **extrinsic semiconductor.** The doping increases the conductivity of the basic intrinsic semiconductors hence the extrinsic semiconductors are used in practice for manufacturing of various electronic devices such as diodes, transistors etc.

Depending upon the type of impurities, the two types of extrinsic semiconductors are,

1. n-type and 2. p-type

1.8.1 Types of Impurities

The impurity material having five valence electrons is called **pentavalent atom**. When this is added to an intrinsic semicondcutor, it is called **donor doping** as each impurity atom donates one free electron to an intrinsic material. Such an impurity is called **donor impurity.** The examples of such impurity are arsenic, bismuth, phosphorous etc. This creats an extrinsic semiconductor with large number of free electrons, called **n-type semiconductor.**

Another type of impurity used is **trivalent atom** which has only three valence electrons. Such an impurity is called **acceptor impurity**. When this is added to an intrinsic semiconductor, it creats more holes and ready to accept an electron hence the doping is called **acceptor doping**. The examples of such impurity are gallium, indium and boron. The resulting extrinsic semiconductor with large number of holes is called **p-type semiconductor**.

1.9 n-Type Semiconductor

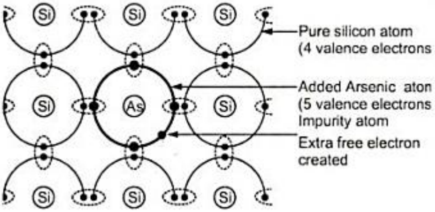

Si
As
Pure silicon atom
(4 valence electrons
Added Arsenic aton
(5 valence electrons
Impurity atom
Extra free electron
created

Fig. 1.10 n-type material formation

When a small amount of pentavalent impurity is added to a pure semiconductor, it is called **n-type semiconductor**. The pentavalent impurity has five valence electrons. These elements are such as arsenic, bismuth, phosphorous and antimony. Such an impurity is called **donor impurity**.

Consider the formation of n-type material by adding arsenic (As) into silicon (Si). The arsenic atom has five valence electrons. An arsenic atom fits in the silicon crystal in such a way that its four valence electrons form covalent bonds with four adjacent silicon atoms. The fifth electron has no chance of forming a covalent bond. This spare electron enters the conduction band as a free electron. Such n-type material formation is represented in the Fig. 1.10. This means that **each arsenic atom added into silicon atom gives one free electron**. The number of such free electrons can be controlled by the amount of impurity added to the silicon. Since the free electrons have negative charges, the material is known as n-type material and an impurity donates a free electron hence called donor impurity.

1.9.1 Conduction in n-Type Semiconductor

When the voltage is applied to the n-type semiconductor, the free electrons which are readily available due to added impurity, move in a direction of positive terminal of

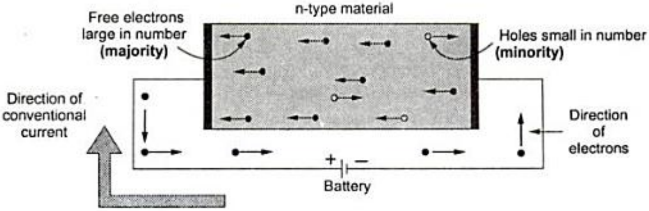

n-type material
Free electrons
large in number
(majority)
Holes small in number
(minority)
Direction of
conventional
current
Direction
of
electrons
+
−
Battery

Fig. 1.11 Conduction in n-type material

voltage applied. This constitutes a current. Thus the conduction is predominantly by free electrons. The holes are less in number hence electron current is dominant over the hole current. Hence in n-type semiconductors free electrons are called **majority carriers** while the holes which are small in number are called **minority carriers**. The conduction in n-type material is shown in the Fig. 1.11.

1.10 p-Type Semiconductor

When a small amount of trivalent impurity is added to a pure semiconductor, it is called **p-type semiconductor**. The trivalent impurity has three valence electrons. These elements are such as gallium, boron or indium. Such an impurity is called **acceptor impurity.**

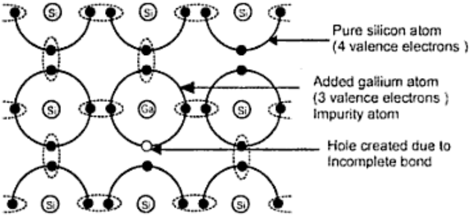


Fig. 1.12 p-type material formation

Consider the formation of p-type material by adding gallium (Ga) into silicon (Si). The gallium atom has three valence electrons. So gallium atom fits in the silicon crystal in such a way that its three valence electrons form covalent bonds with the three adjacent silicon atoms. Being short of one electron, the fourth covalent bond in the valence shell is incomplete. The resulting vacancy is called a hole. Such p-type material formation is represented in the Fig. 1.12. This means that each gallium atom added into silicon atom gives one hole. The number of such holes can be controlled by the amount of impurity added to the silicon. As the holes are treated as positively charged, the material is known as p-type material.

At room temperature, the thermal energy is sufficient to extract an electron from the neighbouring atom which fills the vacancy in the incomplete bond around impurity atom. But this creates a vacancy in the adjacent bond from where the electron had jumped, which is nothing but a hole. This indicates that a hole created due to added impurity is ready to accept an electron and hence is called acceptor impurity. Thus even for a small amount of impurity added, large number of holes get created in the p-type material.

1.10.1 Conduction in p-Type Semiconductor

If now such p-type material is subjected to an electric field by applying a voltage then the holes move in a valence band and are mainly responsible for the conduction. So the current conduction in p-type material is predominantly due to the holes. The free electrons are also present in conduction band but are very less in number. Hence holes are the **majority carriers** while electrons are **minority** carriers in p-type material. The conduction in p-type material is shown in the Fig. 1.13.

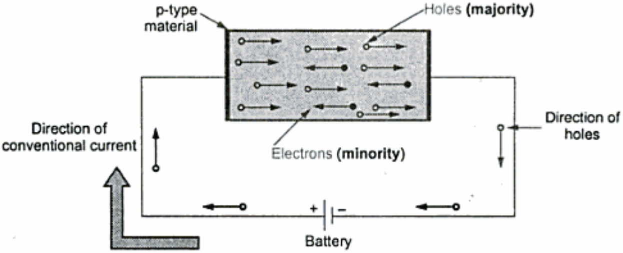


Fig. 1.13 Conduction in p-type material

1.11 P-N Junction

The two type of materials namely p-type and n-type are chemically combined with a special fabrication technique to form a **p-n junction.** The p-n junction forms a popular semiconductor device called diode. The diode is the basic element of number of electronic circuits. Hence the knowledge of p-n junction and its behaviour is very important in understanding the operation of number of electronic circuits, applications and devices.

Let us study first the features of unbiased p-n junction.

1.11.1 Unbiased P-N Junction

If in a given material if the doping is not uniform then at one place large number of charge carriers exist while at other place small number of charge carriers exist. In a high charge carrier concentration area, all charge carriers are of similar type, either electrons or holes and hence start repelling each other. Due to this, charge carriers start moving from high cocentration area towards low concentration area, to achieve uniform concentration all over the meterial. This process is called **diffusion** and exists when there is nonuniform concentration of charge carriers in the material. In a p-n junction, on n side there are large number of electrons while on p side electrons are minority in number. So there is high concentration of electrons on n side while low concentration of electrons on p side. Hence diffusion starts and electrons start moving from n side towards p side.

Similarly the holes from p-side diffuse across the junction into the n-region.

The initial diffusion is shown in the Fig. 1.14.

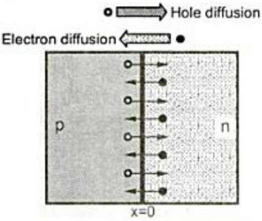


Fig. 1.14 Initial diffusion

1.11.2 Formation of Depletion Region

As holes enter the n region, they find number of donor atoms. The holes recombine with the donor atoms. As donor atoms accept additional holes, they become **positively charged immobile ions**. This happens immediately when holes cross the junction hence number of positively charged immobile ions get formed near the junction **on n side.**

Atoms on p side are acceptor atoms. The electrons diffusing from n side to p side recombine with the acceptor atoms on p side. As acceptor atoms accept additional electrons, they become **negatively charged immobile ions.** Such large number of negatively charged immobile ions get formed near the junction **on p-side.** The formation of immobile ions near the junction is shown in the Fig. 1.15.

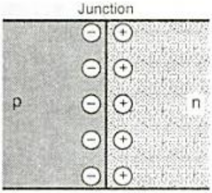


Fig. 1.15 Formation of immobile ions

As more number of holes diffuse on n side, large positive charge gets accumulated on n side near the junction. Eventually the diffusing holes which are positively charged, get repelled due to accumulated positive charge on n side. And the diffusion of holes stops.

Similarly due to large negative charge accumulated on p side, the diffusing electrons get repelled and eventually the diffusion of electrons also stops.

Thus in thermal equilibrium, in the region near the junction, there exists a wall of negative immobile charges on p side and a wall of positive immobile charges on n-side. In this region, there are no mobile charge carriers. Such a region is depleted of the free mobile charge carriers and hence called **depletion region or depletion layer.** The depletion region is also called **space-charge region. In equilibrium condition, the depletion region**

gets widened upto a point where no further electrons or holes can cross the junction. Thus depletion region acts as the **barrier**.

The physical distance from one side to other side of the depletion region is called **width of the depletion region.**

Practically width of the **depletion region** is very small of the order of few microns where 1 micron = 1×10^{-6} m

1.11.3 Barrier Potential

Due to immobile positive charges on n side and negative charges on p side, there exists an electric field across the junction. This creates potential difference across the junction which is called **barrier potential, junction potential, built-in potential or cut-in voltage of p-n junction.**

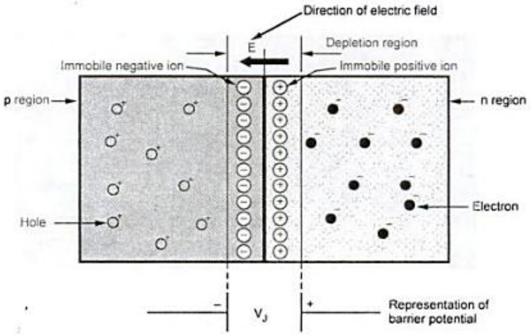

Direction of electric field
E
Depletion region
Immobile negative ion
Immobile positive ion
p region
n region
Electron
Hole
−
V_J
+
Representation of barrier potential

Fig. 1.16 Depletion region and barrier potential

The barrier potential depends on,

1. Type of semiconductor
2. The donor impurity added
3. The acceptor impurity added
4. The temperature

Semiconductor material	Symbol	Barrier potential
Silicon	Si	0.6 V
Germanium	Ge	0.2 V

1.12 Unbiased P-N Junction

If in a given material the doping is not uniform then at one place large number of charge carriers exist while at other place small number of charge carriers exist. In a high charge carrier concentration area, all charge carriers are of similar type, either electrons or holes and hence start repelling each other. Due to this, charge carriers start moving from high concentration area towards low concentration area, to achieve uniform concentration all over the material. This process is called **diffusion** and exists when there is nonuniform concentration of charge carriers in the material. In a p-n junction, on n side there are large number of electrons while on p side electrons are minority in number. So there is high concentration of electrons on n side while low concentration of electrons on p side. Hence diffusion starts and electrons start moving from n side towards p side.

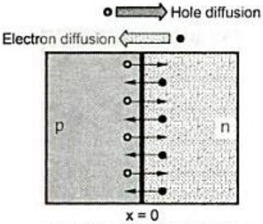


Fig. 1.17 Initial diffusion

Similarly the holes from p-side diffuse across the junction into the n-region.

The initial diffusion is shown in the Fig. 1.17.

1.12.1 Formation of Depletion Region

As holes enter the n region, they find number of donor atoms. The holes recombine with the donor atoms. As donor atoms accept additional holes, they become **positively charged immobile ions**. This happens immediately when holes cross the junction hence number of positively charged immobile ions get formed near the junction **on n-side.**

Atoms on p side are acceptor atoms. The electrons diffusing from n side to p side recombine with the acceptor atoms on p side. As acceptor atoms accept additional electrons, they become **negatively charged immobile ions**. Such large number of **negatively** charged immobile ions get formed near the junction **on p-side**. The formation of immobile ions near the junction is shown in the Fig. 1.18.

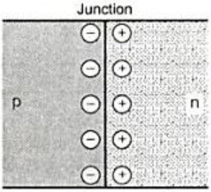


Fig. 1.18 Formation of immobile ions

As more number of holes diffuse on n side, large positive charge gets accumulated on n side near the junction. Eventually the diffusing holes which are positively charged, get repelled due to accumulated positive charge on n side. And the diffusion of holes stops.

Similarly due to large negative charge accumulated on p side, the diffusing electrons get repelled and eventually the diffusion of electrons also stops.

Thus in thermal equilibrium, in the region near the junction, there exists a wall of negative immobile charges on p side and a wall of positive immobile charges on n-side. In this region, there are no mobile charge carriers. Such a region is depleted of the free mobile charge carriers and hence called **depletion region** or **depletion layer**. The depletion region is also called **space-charge region. In equilibrium condition, the depletion region gets widened upto a point where no further electrons or holes can cross the junction.** Thus depletion region acts as the **barrier.**

The physical distance from one side to other side of the depletion region is called **width of the depletion region.**

Practically width of the **depletion region** is very small of the order of few microns where 1 micron = 1×10^{-6} m.

1.12.2 Barrier Potential

Due to immobile positive charges on n-side and negative charges on p side, there exists an electric field across the junction. This creates potential difference across the junction which is called **barrier potential, junction potential, built-in potential or cut-in voltage of p-n junction.**

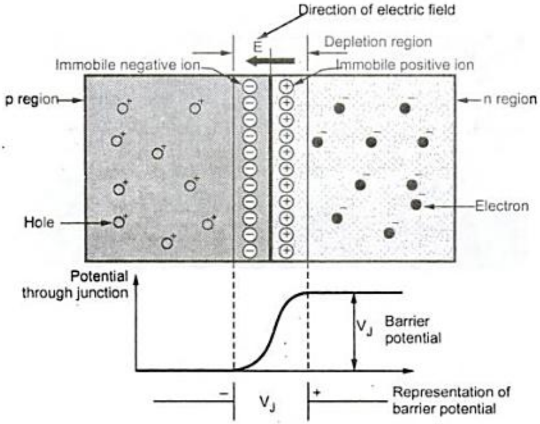

Direction of electric field
E
Depletion region
Immobile negative ion
Immobile positive ion
p region
n region
Electron
Hole
Potential through junction
V_J
Barrier potential
V_J
Representation of barrier potential

Fig. 1.19 Open circuited p-n junction

The barrier potential depends on,

1. Type of semiconductor
2. The donor impurity added
3. The acceptor impurity added
4. The temperature
5. Intrinsic concentration

Semiconductor material	Symbol	Barrier potential
Silicon	Si	0.6 V
Germanium	Ge	0.2 V

The barrier potential is called height of the depletion region and expressed in volts. Symbolically it is denoted as V_J, V_o or V_γ.

1.13 The p-n Junction Diode

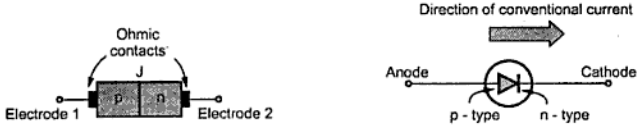
The p-n junction forms a popular semiconductor device called **p-n junction diode**. The p-n junction has two terminals called **electrodes**, one each from p-region and n-region. Due to the two electrodes it is called diode i.e. di + electrode.

To connect the n and p regions to the external terminals, a metal is applied to the heavily doped n and p type semiconductor regions. Such a contact between a metal and a heavily doped semiconductor is called **ohmic contact**. Such an ohmic contact has two important properties,

1. It conducts current equally in both the directions.
2. The drop across the contact is very small, which do not affect the performance of the device.

Thus ohmic contacts are used to connect n and p type regions to the electrodes.

The Fig. 1.20 (a) shows schematic arrangement of p-n junction diode while the Fig. 1.20 (b) shows the symbol of p-n junction diode. The **p-region** acts as **anode** while the **n-region** acts as cathode. The arrowhead in the symbol indicates the direction of the conventional current, which can flow when an external voltage is connected in a specific manner across the diode.



(a) Two electrodes

(b) Symbol of a diode

Fig. 1.20

1.13.1 Biasing of p-n Junction Diode

Applying external d.c. voltage to any electronic device is called **biasing**. As seen, there is no current in the unbiased p-n junction at equilibrium.

> **Key Point:** *The usefulness of p-n junction lies in the fact that it allows current flow only in one direction, under biased condition.*

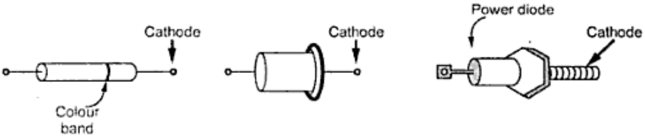
Depending upon the polarity of the d.c. voltage externally applied to it, the biasing is classified as **Forward biasing** and **Reverse biasing.**

1.13.2 Types of Diodes

When forward current flows under forward biasing, diode gets heated. Hence forward current should not exceed the particular maximum value. Similarly the diode can be damaged due to large reverse voltage applied to it during reverse biasing. This voltage also must be maintained below the particular maximum value. These maximum values are specified in the manufacturer's datasheet.

> **Key Point** : *Practically the diodes which can carry large forward current and handle large reverse voltage are physically large in size.*

The diodes which are small in size can carry low forward current and can handle low reverse voltage. The Fig. 1.21 shows the types of diodes based on forward current carrying and reverse voltage withstanding capacity.



(a) Low current (b) Medium current (c) Large current

Fig. 1.21 Types of diodes

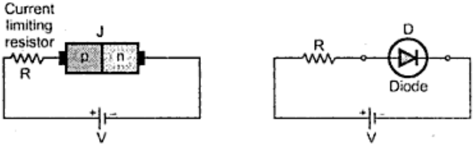
	Diode	Forward current capacity	Reverse voltage capacity
1.	Low current	Upto 100 mA	Upto 75 V
2.	Medium current	Upto 400 mA	Upto 200 V
3.	Large current	Few amperes	Several hundred volts

Let us see in detail, behaviour of a p-n junction under two biasing conditions.

1.14 Forward Biasing of p-n Junction Diode

If an external d.c. voltage is connected in such a way that the p-region terminal is connected to the positive of the d.c. voltage and the n-region is connected to the negative of the d.c. voltage, the biasing condition is called **forward biasing**. The p-n junction is said to be forward biased.

> **Key Point**: *Forward biasing means connecting p-region to +ve and n region to – ve of the battery.*



(a) Forward biasing (b) Symbolic representation

Fig. 1.22

The Fig. 1.22 (a) shows the connection of forward biasing of a p-n junction. To limit the current, practically a current limiting resistor is connected in series with the p-n junction diode. The Fig. 1.22 (b) shows the symbolic representation of a forward biased diode.

1.14.1 Operation of Forward Biased Diode

When the p-n junction is forward biased as long as the applied voltage is less than the barrier potential, there cannot be any conduction.

When the applied voltage becomes more than the barrier potential, the negative terminal of battery pushes the free electrons against barrier potential from n to p region. Similarly positive terminal pushes the holes from p to n region. Thus holes get repelled by positive terminal and cross the junction against barrier potential. Thus the applied voltage overcomes the barrier potential. This reduces the width of depletion region.

As forward voltage is increased, at a particular value the depletion region becomes very much narrow such that large number of majority charge carriers can cross the junction.

The large number of majority carriers constitute a current called **forward current.** Once the conduction electrons enter the p-region, they become valence electrons. Then they move from hole to hole towards the positive terminal of the battery. The movement of valence electrons is nothing but movement of holes in opposite direction to that of electrons, in the p-region. So current in the p-region is the movement of holes which are majority carriers. This is the **hole current.** While the current in the n-region is the movement of free electrons which are majority carriers. This is the **electron current.** Hence the overall forward current is due to the majority charge carriers. The action is shown in the Fig. 1.23. These majority carriers can then travel around the closed circuit and a relatively large current flows. The direction of flow of electrons is from negative to positive of the battery. While direction of the conventional current is from positive to negative of the battery as shown in the Fig. 1.23.

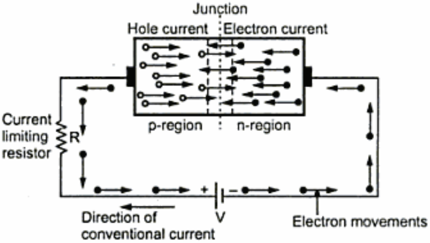
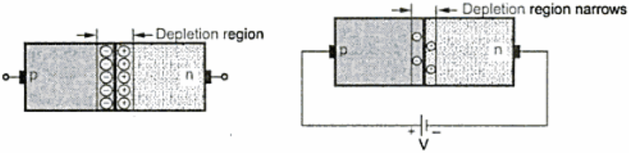

Junction
Hole current
Electron current
Current limiting resistor
R
p-region
n-region
+
−
V
Direction of conventional current
Electron movements

Fig. 1.23 Forward current in a diode

Key Point : *The direction of flow of electrons and conventional current is opposite to each other.*

1.14.2 Effect on the Depletion Region

Due to the forward bias voltage, more electrons flow into the depletion region, which reduces the number of positive ions. Similarly flow of holes reduces the number of negative ions. This reduces the width of the depletion region. This is shown in the Fig. 1.24.


Depletion region
p
n
Depletion region narrows
p
n
+
−
V

(a) Unbiased diode

(b) Forward biased diode

Fig. 1.24

Key Point: *Depletion region narrows due to forward bias voltage.*

1.14.3 Effect of the Barrier Potential

Under the influence of applied forward bias voltage, the free electrons get the energy equivalent to the barrier potential so that they can easily overcome the barrier, which is a sort of a hill, and cross the junction. While crossing the junction, the electrons give up the amount of energy equivalent to the barrier potential. This loss of energy produces a voltage drop across the p-n junction which is almost equal to the barrier potential.

Key Point : *The polarities of voltage drop across the p-n junction in forward biased condition are opposite to that of barrier potential but the value is almost equal to the barrier potential.*

Due to the internal resistance, there is additional small voltage drop across the diode.

Thus the total voltage drop across a p-n junction diode in a forward biased condition is V_f and it is made up of

1. Drop due to barrier potential
2. Drop due to internal resistance.

$$\boxed{V_f = V_\gamma + I_f\, r_f}$$

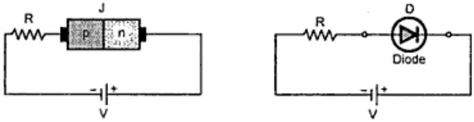
The total V_f is of the order of 0.7 V for silicon and 0.3 V for the germanium.

1.15 Reverse Biasing of p-n Junction Diode

If an external d.c. voltage is connected in such a way that the p-region terminal of a p-n junction is connected to the negative of the battery and the n-region terminal of a p-n junction is connected to the positive terminal of the battery, the biasing condition is called **reverse biasing** of a p-n junction.

Key Point: *Reverse biasing means connecting p-region to –ve and n-region to +ve of the battery.*

The Fig. 1.25 (a) shows the connection of a reverse biasing of a p-n junction while the Fig. 1.25 (b) shows the symbolic representation of a reverse biased diode.



(a) Reverse biasing (b) Symbolic representation

Fig. 1.25

1.15.1 Operation of Reverse Biased Diode

When the p-n junction is reverse biased the negative terminal attracts the holes in the p-region, away from the junction. The positive terminal attracts the free electrons in the n-region away from the junction. No charge carrier is able to cross the junction. As electrons and holes both move away from the junction, the depletion region widens. This creates more positive ions and hence more positive charge in the n-region and more negative ions

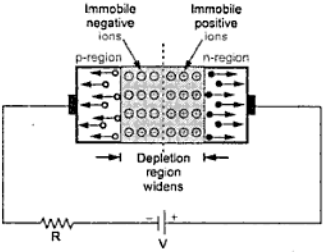


Fig. 1.26 Depletion region widens in reverse bias

and hence more negative charge in the n-region. This is because the applied voltage helps the barrier potential. This is shown in the Fig. 1.26.

Key Point: *Reverse biasing increases the width of the depletion region.*

As depletion region widens, barrier potential across the junction also increases. However, this process cannot continue for long time. In the steady state, majority current ceases as holes and electrons stop moving away from the junction.

The polarities of barrier potential are same as that of the applied voltage. Due to increased barrier potential, the positive side drags the electrons from p-region towards the positive of battery. Similarly negative side of barrier potential drags the holes from n-region towards the negative of battery. The electrons on p-side and holes on n-side are minority charge carriers, which constitute the current in reverse biased condition. Thus reverse conduction takes place.

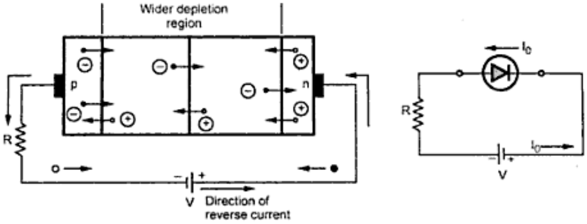
The reverse current flows due to minority charge carriers which are small in number. Hence reverse current is always very small.

Key Point : *The generation of minority charge carriers depends on the the temperature and not on the applied reverse bias voltage. Thus the reverse current depends on the temperature i.e. thermal generation and not on the reverse voltage applied.*

For a constant temperature, the reverse current is almost constant though reverse voltage is increased upto a certain limit. Hence it is called **reverse saturation current** and denoted as I_0.

Key Point: *Reverse saturation current is very small of the order of few microamperes for germanium and few nanoamperes for silicon p-n junction diodes.*

The reverse current and its direction is shown in the Fig. 1.27.



(a) Flow of minority charge carriers

(b) Direction of reverse current

Fig. 1.27 Reverse biased diode

The reverse biasing produces a voltage drop across the diode denoted as V_R which is almost equal to applied reverse voltage.

1.15.2 Breakdown in Reverse Biased

Though the reverse saturation current is not dependent on the applied reverse voltage, if reverse voltage is increased beyond particular value, large reverse current can flow damaging the diode. This is called **reverse breakdown** of a diode. Such a reverse breakdown of a diode can take place due to the following two effects,

1. Avalanche effect and 2. Zener effect

Breakdown Due to the Avalanche Effect

Though reverse current is not dependent on reverse voltage, if reverse voltage is increased, at a particular value, velocity of minority carriers increases. Due to the kinetic energy associated with the minority carriers,more minority carriers are generated when there is collision of minority carriers with the atoms. The collision make the electrons to break the co-valent bonds. These electrons are available as minority carriers and get accelerated due to high reverse voltage. They again collide with another atoms to generate more minority carriers. This is called **carrier multiplication.** Finally large number of minority carriers move across the junction, breaking the p-n junction. These large number of minority carriers give rise to a very high reverse current. This effect is called **avalanche effect** and the mechanism of destroying the junction is called **reverse breakdown** of a p-n junction. The voltage at which the breakdown of a p-n junction occurs is called **reverse breakdown voltage**. The series resistance must be used to avoid breakdown condition, limiting the reverse current.

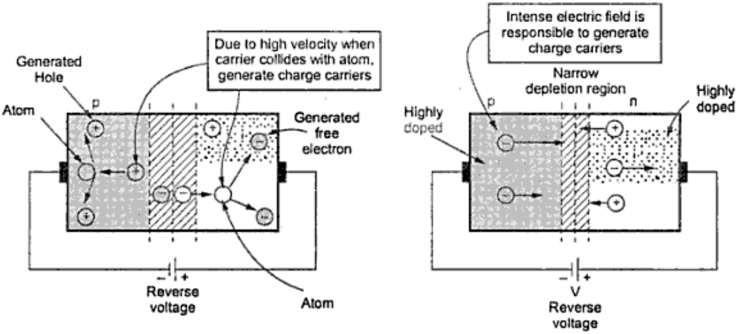
Breakdown Due to the Zener Effect

The breakdown of a p-n junction may occur because of one more effect called **zener effect**. When a p-n junction is heavily doped the depletion region is very narrow. So under reverse bias conditions, the electric field across the depletion layer is very intense. Electric field is voltage per distance and due to narrow depletion region and high reverse voltage, it is intense. Such an intense field is enough to pull the electrons out of the valence bands of the stable atoms. So this is not due to the collision of carriers with atoms. Such a creation of free electrons is called **zener effect** which is different than the avalanche effect. These minority carriers constitute very large current and mechanism is called **zener breakdown.**

> **Key Point** : *The normal p-n junction diode is practically not operated in reverse breakdown region though may be operated in reverse biased condition.*

The breakdown effects are not required to be considered for p-n junction diode. These effects are required to be considered for special diodes such as zener diode as such diodes are always operated in reverse breakdown condition.

The Fig. 1.28(a) shows the avalanche effect while the Fig. 1.28 (b) shows the zener effect.


Generated Hole
Atom
p
Due to high velocity when carrier collides with atom, generate charge carriers
Generated free electron
Reverse voltage
Atom
Intense electric field is responsible to generate charge carriers
Narrow depletion region
Highly doped
p
n
Highly doped
V
Reverse voltage

(a) Avalanche breakdown

(b) Zener effect

Fig. 1.28 Breakdown mechanisms

Why to avoid reverse breakdown ?

1. Large reverse voltage appears across the diode and large current flows through the diode in reverse breakdown condition.
2. So large power gets dissipated which appears in the form of heat at the junction.
3. This increases junction temperature beyond the safe limits and this may damage the diode permanently.

So reverse breakdown must be avoided for conventional diodes.

Some special diodes are manufactured to be operated in the reverse breakdown region and are called zener diodes.

1.16 The Volt-Ampere (V-I) Characteristics of a Diode

The response of a diode when connected in an electrical circuit, can be judged from its characteristics known as Volt-Ampere commonly called **V-I characteristics.** The V-I characteristics in the forward biased and reverse biased condition is the graph of voltage across the diode against the diode current.

1.16.1 Forward Characteristics of p-n Junction Diode

The response of p-n junction can be easily indicated with the help of characteristics called **V-I characteristics** of p-n junction. It is the graph of voltage applied across the p-n junction and the current flowing through the p-n junction.

The Fig. 1.29 shows the forward biased diode. The applied voltage is V while the voltage across the diode is V_f. The current flowing in the circuit is the forward current I_f. The graph of forward current I_f against the forward voltage V_f across the diode is called **forward characteristics** of a diode.

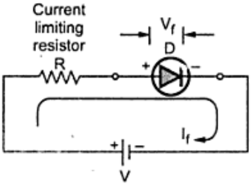


Fig. 1.29 Forward biased diode

The forward characteristics of a diode is shown in the Fig. 1.30.

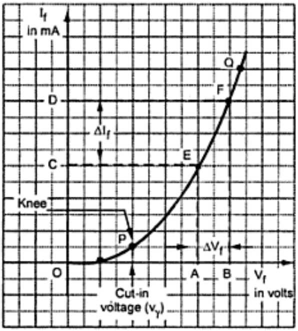


Fig. 1.30 Forward characteristics of a diode

Basically forward characteristics can be divided into two regions :

1. **Region O to P :** As long as V_f is less than cut-in voltage (V_γ), the current flowing is very small. Practically this current is assumed to be zero.

2. **Region P to Q and onwards :** As V_f increases towards V_γ the width of depletion region goes on reducing. When V_f exceeds V_γ i.e. cut-in voltage, the depletion region becomes very thin and current I_f increases suddenly. This increase in the current is **exponential** as shown in the Fig. 1.30 by the region P to Q.

The point P, after which the forward current starts increasing exponentially is called **knee** of the curve.

Key Point : *The normal forward biased operation of the diode is above the knee point of the curve. i.e. in the region P-Q.*

The forward current is the conventional current, hence it is treated as positive and the forward voltage V_f is also treated positive. Hence the forward characteristics is plotted in the **first quadrant**.

Forward Resistance of a Diode

The resistance offered by the p-n junction diode in forward biased condition is called **forward resistance.** The forward resistance is defined in two ways :

1) Static Forward Resistance :

This is the forward resistance of p-n junction diode when p-n junction is used in d.c. circuit and the applied forward voltage is d.c. This resistance is denoted as R_f and is calculated at a particular point on the forward characteristics.

Thus at a point E shown in the forward characteristics, the static resistance R_f is defined as the ratio of the d.c. voltage applied across the p-n junction to the d.c. current flowing through the p-n junction.

$$\boxed{R_f = \frac{\text{Forward d.c. voltage}}{\text{Forward d.c. current}} = \frac{OA}{OC} \text{ at point E}}$$

2) Dynamic forward resistance :

The resistance offered by the p-n junction under a.c. conditions is called **dynamic resistance** denoted as r_f.

Key Point: *The dynamic resistance is reciprocal of the slope of the forward characteristics.*

Consider the change in applied voltage from point A to B shown in the Fig. 1.30. This is denoted as ΔV_f. The corresponding change in the forward current is from point C to D. It is denoted as ΔI_f. Thus the slope of the characteristics is $\Delta I_f / \Delta V_f$. The reciprocal of the slope is dynamic resistance r_f.

$$\boxed{r_f = \frac{\Delta V_f}{\Delta I_f} = \frac{1}{(\Delta I_f / \Delta V_f)} = \frac{1}{\text{Slope of forward characteristics}}}$$

Key Point : *Generally the value of r_f is very small of the order of few ohms, in the operating region i.e. above the knee.*

The dynamic forward resistance can also be obtained as,

$$\boxed{r'_f = \frac{26 \text{ mV}}{I_f}}$$

This gives resistance only for the junction and does not include d.c. resistance of semiconductor material. Hence r'_f is slightly less than r_f.

1.16.2 Reverse Characteristics of p-n Junction Diode

The Fig. 1.31 shows the reverse biased diode. The reverse voltage across the diode is V_R while the current flowing is reverse current I_R flowing due to minority charge carriers. The graph of I_R against V_R is called **reverse characteristics** of a diode.

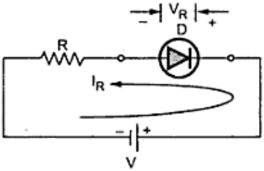


Fig. 1.31 Reverse biased diode

The polarity of reverse voltage applied is opposite to that of forward voltage. Hence in practice reverse voltage is taken as negative. Similarly the reverse saturation current is due to minority carriers and is opposite to the forward current. Hence in practice reverse saturation current is also taken as negative. Hence the reverse characteristics is plotted in the **third quadrant** as shown in the Fig. 1.32.

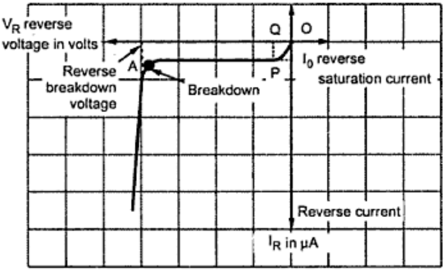


Fig. 1.32

Key Point : *Typically the reverse breakdown voltage is greater than 50 V for normal p-n junctions.*

As reverse voltage is increased, reverse current increases initially but after a certain voltage, the current remains constant equal to reverse saturation current I_0 though reverse voltage is increased. The point A where breakdown occurs and reverse current increases rapidly is called knee of the reverse characteristics.

Reverse Resistance of a Diode

The p-n junction offers large resistance in the reverse biased condition called **reverse resistance**. This is also defined in two ways.

1. Reverse static resistance :

This is reverse resistance under d.c. conditions, denoted as R_r. It is the ratio of applied reverse voltage to the reverse saturation current I_0.

$$\therefore \quad \boxed{R_r = \frac{OQ}{I_0} = \frac{\text{Applied reverse voltage}}{\text{Reverse saturation current}}}$$

2. Reverse dynamic resistance :

This is the reverse resistance under the a.c. conditions, denoted as r_r. It is the ratio of incremental change in the reverse voltage applied to the corresponding change in the reverse current.

$$\therefore \quad \boxed{r_r = \frac{\Delta V_R}{\Delta I_R} = \frac{\text{Change in reverse voltage}}{\text{Change in reverse current}}}$$

The dynamic resistance is most important in practice whether the junction is forward or reverse biased.

1.16.3 Complete V-I Characteristics of a Diode

The complete V-I characteristics of a diode is the combination of its forward as well as reverse characteristics. This is shown in the Fig. 1.33.

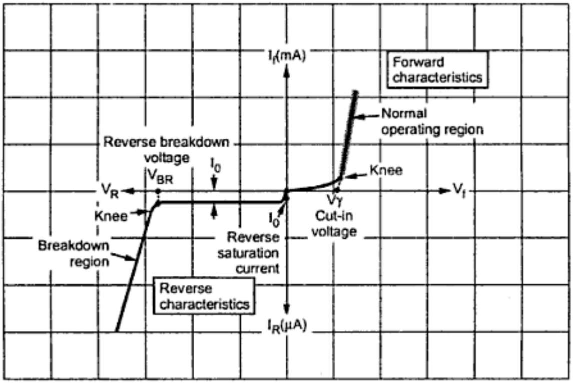


Fig. 1.33 Complete V-I characteristics of a diode

In forward characteristics, it is seen that initially forward current is small as long as the bias voltage is less than the barrier potential. At a certain voltage close to barrier potential, current increases rapidly. The voltage at which diode current starts increasing rapidly is called as cut-in voltage. It is denoted by V_γ. Below this voltage, current is less than 1% of maximum rated value of diode current. The cut-in voltage for germanium is about 0.2 V while for silicon it is 0.6 V.

It is important to note that the breakdown voltage is much higher and practically diodes are not operated in the breakdown condition. **The voltage at which breakdown occurs is called reverse breakdown voltage denoted as V_{BR}.**

> **Key Point** : *Reverse current before the breakdown is very very small and can be practically neglected.*

1.16.4 V-I Characteristics of Typical Ge and Si Diodes

The combined forward and reverse characteristics is called V-I characteristics of a diode. As mentioned earlier, the barrier potential for germanium (Ge) diode is about 0.3 V while for Silicon (Si) diode is as about 0.7 V. The potential at which current starts increasing exponentially is also called **offset potential, threshold potential** or **firing potential** of a diode. The Fig. 1.34 shows the V-I characteristics of typical Ge and Si diodes.

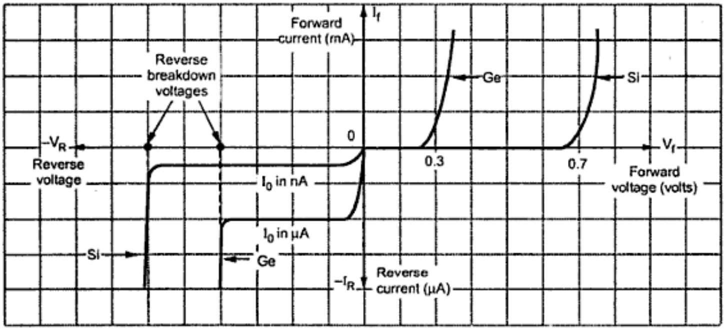


Fig. 1.34 V-I characteristics of typical Ge and Si diodes

The reverse saturation current in a germanium diode is about 1000 times more than the reverse saturation current in a silicon diode of a comparable rating. The reverse saturation current I_0 is of the order of nA for silicon diode while it is of the order of μA for germanium diode. Reverse breakdown voltage for Si diode is higher than that of the Ge diode of a comparable rating.

➡ **Example 1.1 :** *A particular diode carries forward current of 60 mA when forward voltage applied is 0.2 V. Find its d.c. forward resistance. It carries reverse current of 25 μA when reverse voltage is 60 V, find its d.c. reverse resistance.*

Solution : $V_f = 0.2$ V, $I_f = 60$ mA, $V_R = 60$ V, $I_0 = 25\ \mu A$

$$\therefore \quad R_f = \frac{V_f}{I_f} = \frac{0.2}{60 \times 10^{-3}} = \mathbf{3.333\ \Omega}$$

$$\therefore \quad R_r = \frac{V_R}{I_0} = \frac{60}{25 \times 10^{-6}} = \mathbf{2.4\ M\Omega}$$

➡ **Example 1.2 :** *The forward characteristics of a diode is shown in the Fig. 1.35.*

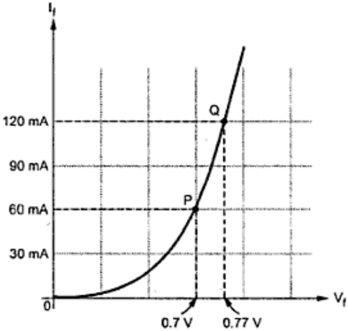


Fig. 1.35

i) Find the d.c. forward resistance at point P.

ii) Find the dynamic forward resistance from the characteristics.

Solution : From the characteristics, at point P, $V_f = 0.7$ V, $I_f = 60$ mA

$$\text{i)} \quad R_f = \text{d.c. forward resistance} = \frac{V_f}{I_f} = \frac{0.7}{60 \times 10^{-3}} = \mathbf{11.66\ \Omega}$$

ii) As the forward voltage changes from P to Q,

$$\Delta V_f = 0.77 - 0.7 = 0.07 \text{ V} \quad \text{and} \quad \Delta I_f = 120 - 60 = 60 \text{ mA}$$

$$\therefore \quad r_f = \frac{\Delta V_f}{\Delta I_f} = \frac{0.07}{60 \times 10^{-3}} = \mathbf{1.166\ \Omega}$$

1.17 Equation of V-I Characteristics of Diode

The diode current depends on the voltage applied to it. The relationship between applied voltage V and the diode current I is exponential and is mathematically given by the equation called **diode current equation**. It is expressed as,

$$\boxed{I = I_0\left[e^{V/\eta V_T} - 1\right] \text{ A}}$$

where I_0 = reverse saturation current in amperes

V = applied voltage

η = 1 for germanium diode

= 2 for silicon diode

V_T = voltage equivalent of temperature in volts

The **voltage equivalent of temperature** indicates dependence of diode current on temperature. The voltage equivalent of temperature V_T for a given diode at temperature T is calculated as,

$$\boxed{V_T = kT \text{ volts}}$$

where k = Boltzmann's constant = 8.62×10^{-5} eV/° K

T = temperature in °K.

Thus at room temperature of 27 °C i.e. T = 27 + 273 = 300 °K the value of V_T is,

$$\boxed{V_T = 8.62 \times 10^{-5} \times 300 = 0.02586 \text{ V} \approx 26 \text{ mV}}$$

The value of V_T also can be expressed as,

$$V_T = \frac{T}{\left(\frac{1}{k}\right)} = \frac{T}{\left(\frac{1}{8.62\times 10^{-5}}\right)} = \frac{T}{11600}$$

$$\therefore \quad \boxed{V_T = \frac{T}{11600}}$$

Thus at room temperature of T = 300 °K, we get V_T = 26 mV.

The diode current equation is applicable for all the conditions of diode i.e. unbiased, forward biased and reverse biased.

When unbiased, V = 0 hence we get,

$$I = I_0\,[e^0 - 1] = 0 \text{ A}$$

Thus there is no current through diode when unbiased.

> For forward biased, **V must be taken positive** and we get current I positive which is forward current. For reverse biased, **V must be taken negative** and we get negative current I which indicates that it is reverse current.

1.17.1 Nature of V-I Characteristics from Equation of Diode

Consider a current equation of diode as,

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

Now for a forward biased condition, the bias voltage V is considered positive and hence exponential index has positive sign. Due to this, $1 << e^{V/\eta V_T}$ hence neglecting 1 we get the equation for a forward current as,

$$\boxed{I_f = I_0 \, e^{V/\eta V_T}}$$

This indicates that once bias voltage exceeds cut in voltage, the forward current increases exponentially. In reverse biased condition, the bias voltage V is treated negative and due to this exponential index has negative sign. So $e^{-V/\eta V_T} << 1$, hence neglecting exponential term we get,

$$\boxed{\alpha I_R \equiv I_0 (-1) \equiv - I_0}$$

The above equation indicates that under reverse biased condition, the current is reverse saturation current which is negative indicating that it flows in opposite direction to that of

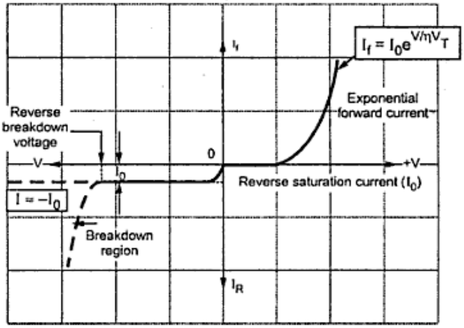


Fig. 1.36 V-I characteristics of p-n junction diode

forward current and almost constant. Such nature of diode characteristics is already been discussed and it is as shown in Fig. 1.36. The dashed portion represents **breakdown region.**

Key Point : *The entire V-I characteristics of a p-n junction diode depends on the temperature, as reverse current and V_T are temperature dependent.*

➠ **Example 1.3 :** *Using the diode equation, find the p-n junction [germanium] diode current for a forward bias of 0.22 V at room temperature 25 °C with reverse saturation current equal to 2 mA. Take $\eta = 1$.*

Solution : The diode current equation is,

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right]$$

Now $V = 0.22 \text{ V}, \eta = 1, I_0 = 2 \text{ mA}, T = 25\ ^\circ\text{C} = (25+273)\ ^\circ\text{K}$

$$V_T = kT = 8.62 \times 10^{-5} \times [25+273]$$

$$= 0.02568 \text{ V}$$

$$\therefore \quad I = 2 \times 10^{-3} \left[e^{0.22/0.02568} - 1 \right]$$

$$= \mathbf{10.5084 \text{ A}}$$

1.18 Effect of Temperature on Diode

The temperature has following effects on the diode parameters,

1. The cut-in voltage decreases as the temperature increases. The diode conducts at smaller voltages at large temperature.
2. The reverse saturation current increases as temperature increases.

This increase in reverse current I_0 is such that it **doubles at every 10 °C rise in temperature.** Mathematically,

$$\boxed{I_{02} = 2^{(\Delta T/10)}\, I_{01}}$$

where I_{02} = Reverse current at T_2 °C

I_{01} = Reverse current at T_1 °C

$\Delta T = (T_2 - T_1)$

3. The voltage equivalent of temperature V_T also increases as temperature increases.
4. The reverse breakdown voltage increases as temperature increases.

This is shown in the Fig. 1.37.

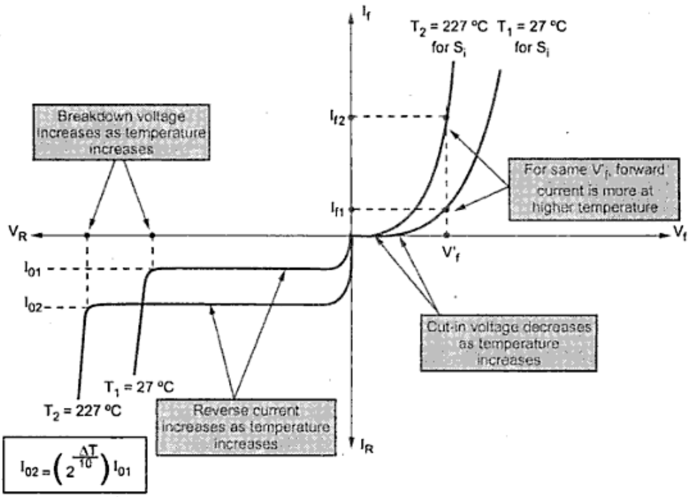

I_f
T₂ = 227 °C for Si
T₁ = 27 °C for Si
Breakdown voltage increases as temperature increases
I_f2
I_f1
For same V'_f, forward current is more at higher temperature
V_R
V_f
V'_f
I_01
I_02
Cut-in voltage decreases as temperature increases
T₁ = 27 °C
T₂ = 227 °C
Reverse current increases as temperature increases
I_R
I_02 = (2^(ΔT/10)) I_01

Fig. 1.37 Effect of temperature on diode

Example 1.4 : *The reverse saturation current of a silicon diode is 3 nA at 27 °C. Find,*

i) Reverse saturation current at 82 °C.

ii) Forward current at 82 °C if forward voltage applied is 0.25 V.

Solution : $I_{01} = 3$ nA at $T_1 = 27$ °C, $T_2 = 82$ °C

i) $$\Delta T = T_2 - T_1 = 82 - 27 = 55\ ^\circ C$$

$$\therefore \quad I_{02} = 2^{(\Delta T/10)} \times I_{01} = 2^{\left(\frac{55}{10}\right)} \times 3 = \mathbf{135.764\ nA}$$

ii) $$V = 0.25\ V,\ I_{02} = 135.764\ nA \text{ at } 82\ ^\circ C$$

$$\therefore \quad I_f = I_0\left[e^{V/\eta V_T} - 1\right]$$

$$V_T = \frac{T}{11600} = \frac{(82+273)}{11600} = 0.0306\ V,\ \eta = 2 \text{ for Si}$$

$$\therefore \quad I_f = 135.764 \times 10^{-9}\left[e^{0.25/2\times0.0306} - 1\right] = \mathbf{7.934\ \mu A}$$

1.19 Junction Capacitances

Depending upon the biasing condition, two types of capacitive effects exist in the diodes. These are,

1) Transition capacitance (C_T) is reverse biased condition.
2) Diffusion capacitance (C_D) is forward biased condition.

1.19.1 Transition Capacitance (C_T or C_{pn})

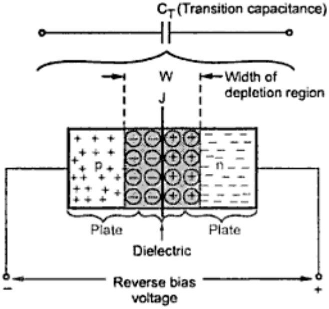


Fig. 1.38

When a diode is reverse biased, the width of the depletion region increases. So there are more positive and negative charges present in the depletion region.

Due to this, the p-region and n-region act like the plates of capacitor while the depletion region acts like dielectric. Thus there exists a capacitance at the p-n junction called **transition capacitance, junction capacitance, space charge capacitance, barrier capacitance** or **depletion region capacitance.** It is denoted as C_T.

Mathematically it is given by the expression,

$$\boxed{C_T = \frac{\varepsilon A}{W}} \quad \dots (1)$$

where ε = permittivity of semiconductor = $\varepsilon_0 \varepsilon_r$

$$\varepsilon_0 = \frac{1}{36\pi \times 10^9} = 8.849 \times 10^{-12} \text{ F/m}$$

ε_r = relative permittivity of semiconductor = 16 for Ge, 12 for Si

A = area of cross section

W = width of depletion region

As the reverse biased applied to the diode increases, the width of the depletion region (W) increases. Thus the transition capacitance C_T decreases. In short, the capacitance can be controlled by the applied voltage. The variation of C_T with respect to the applied reverse bias voltage is shown in the Fig. 1.39.

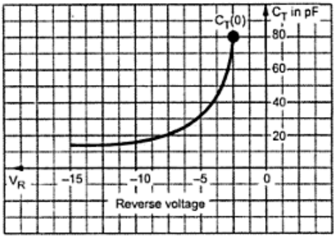


Fig. 1.39

As reverse voltage is negative, graph is shown in the second quadrant. For a particular diode shown, C_T varies from 80 pF to less than 5 pF as V_R changes from 2 V to 15 V.

Key Point : *The transition capacitance is also called depletion layer capacitance and denoted as* C_{pn}.

1.19.2 Diffusion Capacitance (C_D)

During forward biased condition, an another capacitance comes into existence called **diffusion capacitance** or **storage capacitance,** denoted as C_D.

In forward biased condition, the width of the depletion region decreases and holes from p-side get diffused in n-side while electrons from n side move into the p-side. As the applied voltage increases, concentration of injected charged particles increases. This rate of change of the injected charge with applied voltage is defined as a capacitance called **diffusion capacitance.**

$$\therefore \quad C_D = \frac{dQ}{dV} \quad \text{... (2)}$$

The diffusion capacitance can be determined by the expression

$$\boxed{C_D = \frac{\tau I}{\eta V_T}} \quad \text{... (3)}$$

where τ = mean life time for holes.

So diffusion capacitance is proportional to the current. For forward biased condition, the value of diffusion capacitance is of the order of nano farads to micro farads while transition capacitance is of the order of pico farads. So C_D is much larger than C_T.

However in forward biased condition, C_D appears in parallel with the forward resistance which is very very small. Hence the time constant which is function of product of the forward resistance and C_D is also very small for ordinary signals.

Key Point : *Hence for normal signals* C_D *has no practical significance but for fast signals* C_D *must be considered.*

The graph of C_D against the applied forward voltage is shown in the Fig. 1.40.

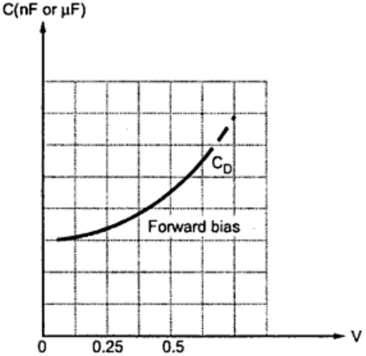
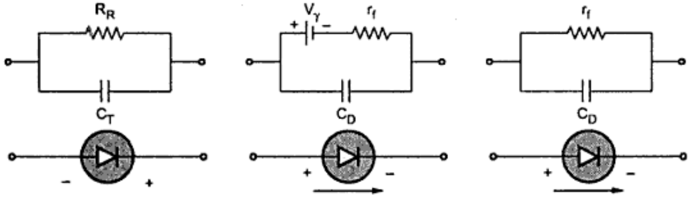


Fig. 1.40 Diffusion capacitance versus applied forward biased voltage

1.20 A.C. Equivalent Circuits

In reverse biased condition, the a.c. equivalent circuit consists of very high reverse resistance R_R in parallel with transition capacitance C_T. It is shown in the Fig. 1.41 (a).

In forward biased condition, the battery of voltage V_γ and series dynamic resistance r_f are in parallel with the diffusion capacitance C_D, to represent complete equivalent circuit. This is shown in the Fig. 1.41 (b). In a.c. equivalent circuit, the d.c. voltage drop V_γ is not included. Thus a.c. equivalent circuit of forward biased diode is as shown in the Fig. 1.41 (c).



(a) A.C. equivalent circuit of reverse biased.

(b) Complete equivalent circuit of forward biased.

(c) A.C. equivalent circuit of forward biased.

Fig. 1.41

1.21 Diode Ratings

The manufacturer of the diode provides the detail information about the diode, in the form of **datasheet**. The selection of diode or replacement of diode in an application circuit becomes easy by referring the diode datasheet specificaions.

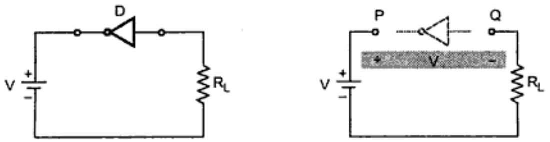
The following are the most important specifications related to a diode which are available in all the datasheets.

No.	Symbol	Specifications
1.	V_F	The forward voltage mentioned at specific current and temperature.
2.	I_F	The maximum forward current mentioned at specific temperature.
3.	I_R	The maximum reverse saturation current mentioned at specific temperature.
4.	PIV/PRV or V_{BR}	It is maximum reverse voltage rating at specific temperature. It is also called Peak Inverse Voltage, Peak Reverse Voltage or Reverse Breakdown Voltage.
5.	$P_{D\,max}$	The maximum power dissipation capacity at specific temperature
6.	C_D, C_T	The capacitance levels of diffusion and transition capacitances.
7.	t_{rr}	Reverse recovery time.
8.	T_J, T_{stg}	Operating junction temperature and storage temperature ranges.

Table 1.3 Diode datasheet specifications

The specifications V_F and I_F are maximum limits which diode can handle safely, at a specific temperature. The I_R is generally specified at two temperatures to indicate the effect of temperature on it.

To understand PIV specification, consider reverse biased diode as shown in the Fig. 1.42 (a). It is replaced by its model i.e. open circuit in the Fig. 1.42 (b).



(a) Reverse biased diode

(b) Open circuit model

Fig. 1.42 PIV rating of diode

It can be seen that the voltage between the two points P and Q is the voltage across the diode in the reverse direction. This is the voltage that diode must withstand without breakdown. The maximum value of such a reverse voltage which diode can withstand safely is called **PIV** or **PRV rating** of the diode.

The product of the current through diode and voltage across the diode, at a particular point of operation is the power dissipation across the diode.

$$P_D = V_D I_D$$

The maximum value of P_D i.e. $P_{D\,max}$ which diode can withstand safely, without increasing the temperature of the junction above its limiting value is called **power dissipation rating** of the diode.

The values of C_D and C_T indicate capacitance levels of the diode.

If the diode is going to be switched from ON to OFF and OFF-ON in the circuit frequently then the reverse recovery time is important consideration. This specification is important for the switching diodes and not much important for general purpose rectifier diodes.

The T_J indicates the safe range of junction temperature, which should not be exceeded while the circuit operation. The T_{stg} indicates the safe range of storage temperature.

1.21.1 Datasheet Specifications of 1N4001 - 1N4007

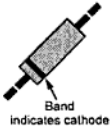


Fig. 1.43 D041

The range of diodes 1N4001 - 1N4007 is a range of general purpose rectifier diodes. Its outline is shown in the Fig. 1.43. The leads are of copper clad steel which are tin plated. These diodes have following features.

1. Low forward voltage drop
2. High surge current capability

In case of rectifiers with filters, a current surge is possible to occur. The diode must be able to withstand such current surges. The capacity of diode to withstand surge current is indicated by the rating $I_{FM\,Surge}$ called **peak forward surge current rating.**

The various specifications are given below.

Absolute Maximum Ratings* T_A = 25 °C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
PIV	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	**Average Rectified Forward Current .375" lead length @ T_A = 75 °C**	**1.0**							**A**
$I_{FM\ Surge}$	**Non-repetitive Peak Forward Surge Current**	**30**							**A**
T_{stg}	Storage Temperature Range	– 55 to + 175							°C
T_J	Operating Junction Temperature	– 55 to + 175							°C

*These ratings are limiting values above which the serviceability of an semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
$P_{D\ max}$	**Power Dissipation**	**3.0**	**W**
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

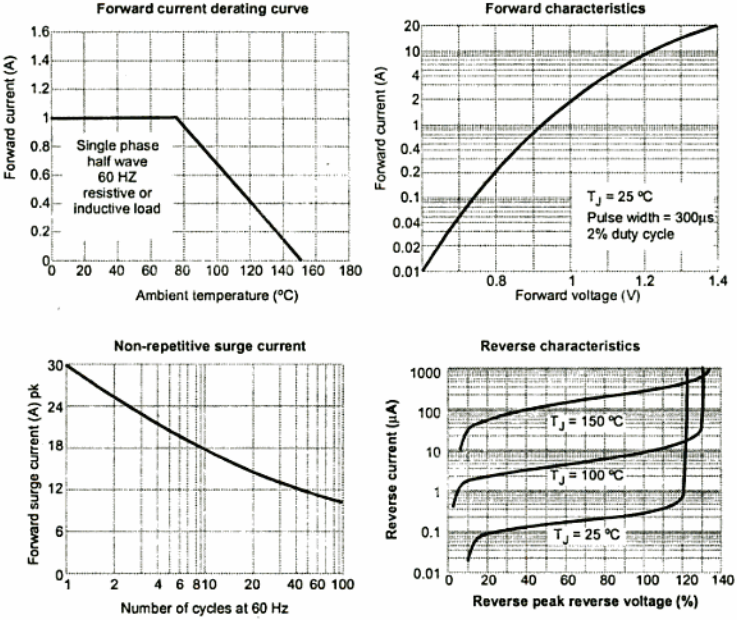
Electrical Characteristcs T_A = 25 °C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	**Forward voltage @ 1.0 A**	**1.1**							**V**
I_{rr}	Maximum Full Load Revers Current, Full cycle T_A = 75 °C	30							µA
I_R	**Reverse Current @ rated V_R T_A = 25 °C**	**5.0**							**µA**
	T_A = 100 °C	**500**							**µA**
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Table 1.4

The various typical characteristic curves are also provided in the datasheet. The curves give idea about behaviour of diode under various varying parameters such as how forward current varies as temperature, how forward current varies as forward voltage and so on.

The characteristic curves for the series 1N4001 – 1N4007 general purpose rectifier diodes are given below.



Forward current derating curve

Forward characteristics

Non-repetitive surge current

Reverse characteristics

Fig. 1.44 Typical characteristics curves for 1N4001 - 1N4007

1.22 Mathematical Expression for the Dynamic Resistance

We have seen earlier that the dynamic resistance is the reciprocal of the slope of the V-I characteristic of a diode. For the incremental changes in voltage and current we can write,

$$r = \frac{1}{\text{Slope of graph}} = \frac{1}{\left[\frac{dI}{dV}\right]} \qquad \text{... (1)}$$

Now current equation of a diode is given by,

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

$$\therefore \qquad \frac{dI}{dV} = I_0 \left[\frac{1}{\eta V_T} \cdot e^{V/\eta V_T}\right]$$

$$\therefore \quad \frac{dI}{dV} = \frac{I_0\, e^{V/\eta V_T}}{\eta V_T} \qquad \text{... (2)}$$

$$\therefore \quad \boxed{r = \frac{1}{\left[\frac{dI}{dV}\right]} = \frac{\eta V_T}{I_0\, e^{V/\eta V_T}}} \qquad \text{... (3)}$$

But from the current equation we can write,

$$I = I_0\, e^{V/\eta V_T} - I_0$$

$$\therefore \quad I_0\, e^{V/\eta V_T} = I + I_0 \qquad \text{... (4)}$$

Substituting in equation (3), we get,

$$\boxed{r = \frac{\eta V_T}{I + I_0} = \text{Dynamic resistance}} \qquad \text{... (5)}$$

While determining the value of dynamic resistance under forward biased and reverse biased conditions, the general expression, equation (3) is used.

Key Point : *For forward biased condition treat V positive while for reverse biased condition treat V as negative, while using the expression.*

The following example will clear the use of the generalised expression in calculating forward and reverse dynamic resistance.

➡ **Example 1.5 :** *For a germanium diode, the reverse saturation current is 2 μA at a reverse voltage of 0.26 V. Calculate forward and reverse dynamic resistance values if forward biased voltage is also 0.26 V, at room temperature.*

Solution : The given values are

$I_0 = 2\ \mu A$, $V = +\,0.26$ V for forward biased, $V = -\,0.26$ V for reverse biased.

$\eta = 1$ for germanium, $V_T = 26$ mV at room temperature.

$$\therefore \quad r_f = \frac{\eta V_T}{I_0\, e^{V/\eta V_T}} = \frac{1 \times 26 \times 10^{-3}}{2 \times 10^{-6} \times e^{(0.26/1 \times 26 \times 10^{-3})}}$$

$$= \mathbf{0.5901\ \Omega} \quad \text{Forward dynamic resistance}$$

$$\text{and} \quad r_r = \frac{\eta V_T}{I_0\, e^{V/\eta V_T}} = \frac{1 \times 26 \times 10^{-3}}{2 \times 10^{-6} \times e^{(-0.26/1 \times 26 \times 10^{-3})}}$$

$$= \mathbf{286.34\ M\Omega} \quad \text{Reverse dynamic resistance}$$

Ans. : $r_f = 0.5901\ \Omega$, $r_r = 286.34\ M\Omega$

1.23 What is Rectifier ?

A **rectifier** is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more p-n junction diodes.

The p-n junction diode conducts only in one direction. It conducts when forward biased while practically it does not conduct when reverse biased. Thus if an alternating voltage is applied across a p-n junction diode, during positive half cycle the diode will be forward biased and will conduct successfully. While during the negative half cycle it will be reversed biased and will not conduct at all. Thus the conduction occurs only during positive half cycle. If the resistance is connected in series with the diode, the output voltage across the resistance will be unidirectional i.e. d.c. Thus p-n junction diode subjected to an a.c. voltage acts as a rectifier converting alternating voltage to a pulsating d.c. voltage.

1.24 The Important Characteristics of a Rectifier Circuit

The important points to be studied while analysing the various rectifier circuits are,

a) **Waveform of the load current :** As rectifier converts a.c. to pulsating d.c., it is important to analyze the nature of the current through load which ultimately determines the waveform of the load voltage.

b) **Regulation of the output voltage :** As the load current changes, load voltage changes. Practically load voltage should remain constant. So concept of regulation is to study the effect of change in load current on the load voltage.

c) **Rectifier efficiency :** It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

d) **Peak value of current in the rectifier circuit :** The peak value is the maximum value of an alternating current in the rectifier circuit. This decides the rating of the rectifier circuit element which is diode.

e) **Peak value of voltage across the rectifier element in the reverse direction (PIV) :** When the diode is not conducting, the reverse voltage gets applied across the diode. The peak value of such voltage decides the peak inverse voltage i.e. PIV rating of a diode.

f) **Ripple factor :** The output of the rectifier is of pulsating d.c. type. The amount of a.c. content in the output can be mathematically expressed by a factor called ripple factor. Less is the ripple factor, better is the performance of the circuit.

Using one or more diodes, following rectifier circuits can be designed.

1. Half wave rectifier 2. Full wave rectifier 3. Bridge rectifier

This chapter explains various rectifying circuits using diodes and introduces the concept of filtering alongwith the detail discussion of capacitor input filter.

1.25 Half Wave Rectifier

In half wave rectifier, rectifying element conducts only during positive half cycle of input a.c. supply. The negative half cycles of a.c. supply are eliminated from the output.

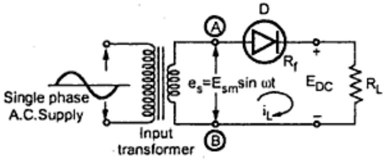


Fig. 1.45 Half wave rectifier

This rectifier circuit consists of resistive load, rectifying element, i.e. p-n junction diode, and the source of a.c. voltage, all connected in series. The circuit diagram is shown in the Fig. 1.45. Usually, the rectifier circuits are operated from ac mains supply. To obtain the desired d.c. voltage across the load, the a.c. voltage is applied to rectifier circuit using suitable step-up or step-down transformer, mostly a step-down one, with necessary turns ratio.

The input voltage to the half-wave rectifier circuit shown in the Fig. 1.45 is a sinusoidal a.c. voltage, having a frequency which is the supply frequency, 50 Hz.

The transformer decides the peak value of the secondary voltage. If N_1 are the primary number of turns and N_2 are the secondary number of turns and E_{pm} is the peak value of the primary voltage then,

$$\boxed{\frac{N_2}{N_1} = \frac{E_{sm}}{E_{pm}}}$$

where E_{sm} = the peak value of the secondary a.c. voltage.

As the nature of E_{sm} is sinusoidal the instantaneous value will be,

$$\boxed{e_s = E_{sm} \sin \omega t}$$

$$\omega = 2\pi f$$

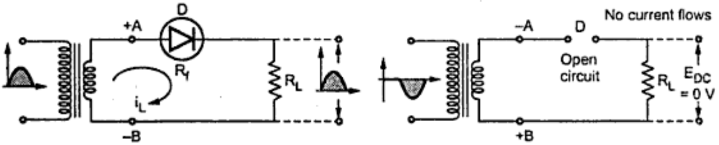
$$f = \text{supply frequency}$$

Let R_f represents the forward resistance of the diode. Assume that, under reverse biased condition, the diode acts almost as an open circuit, conducting no current.

1.25.1 Operation of the Circuit

During the positive half cycle of secondary a.c voltage, terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction, as shown in the Fig. 1.46 (a). The current will flow for almost full positive half cycle. This current is also flowing through load resistance R_L hence denoted as i_L, the load current.

During negative half cycle when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Hence no current flows in the circuit as shown in the Fig. 1.46 (b). Thus the circuit current, which is also the load current, is in the form of half sinusoidal pulses.



(a) Diode forward biased **Fig. 1.46** **(b) Diode reverse biased**

The load voltage, being the product of load current and load resistance, will also be in the form of half sinusoidal pulses. The different waveforms are illustrated in Fig. 1.47.

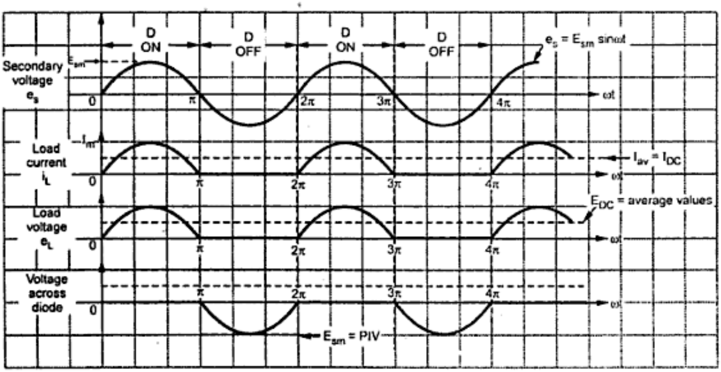


Fig. 1.47 Load current and load voltage waveforms for half wave rectifier

The d.c. output waveform is expected to be a straight line but the half wave rectifier **gives** output in the form of positive sinusoidal pulses. Hence the output is called **pulsating d.c.** It is discontinuous in nature. Hence it is necessary to calculate the average value of load current and average value of output voltage.

1.25.2 Average D.C. Load Current (I_{DC})

The average or d.c. value of alternating current is obtained by integration.

For finding out the average value of an alternating waveform, we have to determine the area under the curve over one complete cycle i.e. from 0 to 2π and then dividing it by the base i.e. 2π.

Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \qquad \text{for } 0 \leq \omega t \leq \pi$$

$$i_L = 0 \qquad \text{for } \pi \leq \omega t \leq 2\pi$$

where I_m = peak value of load current

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(\omega t)\, d(\omega t)$$

As no current flows during negative half cycle of a.c. input voltage, i.e. between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t) = \frac{I_m}{2\pi}\left[-\cos(\omega t)\right]_0^{\pi}$$

$$= -\frac{I_m}{2\pi}\left[\cos(\pi) - \cos(0)\right] = -\frac{I_m}{2\pi}[-1-1] = \frac{I_m}{\pi}$$

$$\therefore \quad \boxed{I_{DC} = \frac{I_m}{\pi} = \text{average value}}$$

Applying Kirchhoff's voltage law we can write,

$$\boxed{I_m = \frac{E_{sm}}{R_f + R_L + R_s}}$$

where R_s = resistance of secondary winding of transformer. If R_s is not given it should be neglected while calculating I_m.

1.25.3 Average D.C. Load Voltage (E_{DC})

It is the product of average D.C. load current and the load resistance R_L.

$$E_{DC} = I_{DC}R_L$$

Substituting value of I_{DC}, $E_{DC} = \frac{I_m}{\pi} R_L = \frac{E_{sm}}{(R_f + R_L + R_s)\pi} R_L$

The winding resistance R_s and forward diode resistance R_f are practically very small compared to R_L.

$$\therefore \quad \boxed{E_{DC} = \frac{E_{sm}}{\pi\left[\frac{R_f + R_s}{R_L} + 1\right]}}$$

But as R_f and R_s are small compared to R_L , $(R_f + R_s)/R_L$ is negligibly small compared to 1. So neglecting it we get,

$$\therefore \quad \boxed{E_{DC} \approx \frac{E_{sm}}{\pi}}$$

Note : When R_f and R_s are finite, calculate I_m, then I_{DC} and from that calculate E_{DC} as $I_{DC}R_L$.

Key Point *: Do not calculate E_{DC} as E_{sm}/π directly for finite R_f and R_s. Calculate I_{m1} then I_{DC} and then $E_{DC} = I_{DC} R_L$.*

1.25.4 R.M.S. Value of Load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S. value of load current can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin \omega t)^2 \, d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} \left(I_m{}^2 \sin^2 \omega t \, d(\omega t)\right)}$$

$$= I_m \sqrt{\frac{1}{2\pi}\int_0^{\pi} \frac{[1 - \cos(2\omega t)]\, d(\omega t)}{2}} = I_m \sqrt{\frac{1}{2\pi}\left\{\frac{\omega t}{2} - \frac{\sin(2\omega t)}{4}\right\}_0^{\pi}}$$

$$= I_m \sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2}\right)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$= \frac{I_m}{2}$$

$$\therefore \quad \boxed{I_{RMS} = \frac{I_m}{2}}$$

Note : Students must remember that this R.M.S. value is for **half wave rectified** waveform hence it is $I_m/2$. For full sine wave it is $I_m/\sqrt{2}$, which is derived later.

1.25.5 R.M.S. Value of the Load Voltage

The r.m.s. value of the load voltage is the r.m.s. value of the total output voltage which includes d.c. output and the a.c. ripples. As the load is resistive, the r.m.s. value of the load voltage is given by,

$$\therefore \quad \boxed{E_{L\,(RMS)} = I_{RMS}\,R_L = \frac{I_m}{2}\,R_L}$$

$$\therefore \quad E_{L\,(RMS)} = \frac{E_{sm}}{2\,(R_f+R_L+R_s)} \times R_L = \frac{E_{sm}}{2\left[1+\frac{R_f+R_s}{R_L}\right]}$$

Now $\quad R_L >> R_f + R_s$ hence $\frac{R_f+R_s}{R_L} << 1$

$$\therefore \quad E_{L\,(RMS)} \approx \frac{E_{sm}}{2}$$

1.25.6 D.C. Power Output (P_{DC})

The d.c. power output can be obtained as,

$$\therefore \quad \boxed{P_{DC} = E_{DC}\,I_{DC} = I_{DC}^2 R_L}$$

$$\text{D.C. Power output} = I_{DC}^2 R_L = \left[\frac{I_m}{\pi}\right]^2 R_L = \frac{I_m{}^2}{\pi^2} R_L$$

$$\therefore \quad P_{DC} = \frac{I_m{}^2}{\pi^2} R_L$$

where $\quad I_m = \frac{E_{sm}}{R_f+R_L+R_s}$

$$\therefore \quad \boxed{P_{DC} = \frac{E_{sm}{}^2 R_L}{\pi^2\,[R_f+R_L+R_s]^2}}$$

1.25.7 A.C. Power Input (P_{AC})

The power input taken from the secondary of transformer is the power supplied to three resistances namely load resistance R_L, the diode resistance R_f and winding resistance R_s. The a.c. power is given by,

$$\boxed{P_{AC} = I_{RMS}^2 [R_L + R_f + R_s]}$$

but $$I_{RMS} = \frac{I_m}{2}$$ for half wave,

$$\therefore \quad \boxed{P_{AC} = \frac{I_m^2}{4}[R_L + R_f + R_s]}$$

1.25.8 Rectifier Efficiency (η)

The rectifier efficiency is defined as the ratio of output d.c. power to input a.c. power.

$$\therefore \quad \eta = \frac{\text{D.C. output power}}{\text{A.C. input power}} = \frac{P_{DC}}{P_{AC}}$$

$$\therefore \quad \eta = \frac{\frac{I_m^2}{\pi^2}R_L}{\frac{I_m^2}{4}[R_f + R_L + R_s]} = \frac{(4/\pi^2)R_L}{(R_f + R_L + R_s)}$$

$$\therefore \quad \boxed{\eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{R_L}\right)}}$$

If $(R_f + R_s) << R_L$ as mentioned earlier, we get the maximum theoretical efficiency of half wave rectifier as,

$$\therefore \quad \boxed{\%\eta_{max} = 0.406 \times 100 = 40.6\ \%}$$

Thus in half wave rectifier, maximum 40.6% a.c. power gets converted to d.c. power in the load. If the efficiency of rectifier is 40% then what happens to the remaining **60%** power. It is **present** interms of ripples in the output which is fluctuating component present in the output.

Key Point : *Thus more the rectifier efficiency, less are the ripple contents in the output.*

1.25.9 Ripple Factor (γ)

It is seen that the output of half wave rectifier is not pure d.c. but a pulsating d.c. The output contains pulsating components called **ripples**. Ideally there should not be any ripples in the rectifier output. The measure of such ripples present in the output is with the help of a factor called **ripple factor** denoted by γ. It tells how smooth is the output.

Key Point : *Smaller the ripple factor closer is the output to a pure d.c.*

The ripple factor expresses how much successful the circuit is, in obtaining pure d.c. from a.c. input.

Definition :

Mathematically **ripple factor** is defined as the ratio of R.M.S. value of the a.c. component in the output to the average or d.c. component present in the output.

$$\boxed{\text{Ripple factor } \gamma = \frac{\text{R.M.S. value of a.c. component of output}}{\text{Average or d.c. component of output}}}$$

Now the output current is composed of a.c. component as well as d.c. component.

Let I_{ac} = r.m.s. value of a. c. component present in output

I_{DC} = d.c. component present in output

I_{RMS} = R.M.S. value of total output current

$$\therefore \quad I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$\therefore \quad I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

Now $$\boxed{\text{Ripple factor} = \frac{I_{ac}}{I_{DC}}}$$ as per definition

$$\therefore \quad \gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}}$$

$$\therefore \quad \boxed{\gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}}$$

This is the general expression for ripple factor and can be used for any rectifier circuit.

Now for a half wave circuit,

$$I_{RMS} = \frac{I_m}{2} \quad \text{while} \quad I_{DC} = \frac{I_m}{\pi}$$

$$\therefore \quad \gamma = \sqrt{\left[\frac{\left(\frac{I_m}{2}\right)}{\left(\frac{I_m}{\pi}\right)}\right]^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674}$$

$$\therefore \quad \boxed{\gamma = 1.211}$$ .. **Half wave**

This indicates that the ripple contents in the output are 1.211 times the d.c. component i.e. 121.1 % of d.c. component.

Key Point : *The ripple factor for half wave is very high which indicates that the half wave circuit is a poor converter of a.c. to d.c.*

The ripple factor is minimised using filter circuits along with the rectifiers.

1.25.10 Load Current

The load current i_L which is composed of a.c. and d.c. components can be expressed using Fourier series as,

$$i_L = I_m\left[\frac{1}{\pi}+\frac{1}{2}\sin\omega t-\frac{2}{3\pi}\cos 2\,\omega t-\frac{2}{15\pi}\cos 4\,\omega t\ \ldots\right]$$

This expression shows that the current may be considered to be the sum of an infinite number of current components, according to Fourier series.

The first term of the series is the average or d.c. value of the load current. The second term is a varying component having frequency same as that of a.c. supply voltage. This is called fundamental component of the current having frequency same as the supply. The third term is again a varying component having frequency twice the frequency of supply voltage. This is called second harmonic component. Similarly all the other terms represent the a.c. components and are called harmonics.

Thus ripple in the output is due to the fundamental component alongwith the various harmonic components. And the average value of the total pulsating d.c. is the d.c. value of the load current, given by the constant term in the series, I_m / π.

1.25.11 Peak Inverse Voltage (PIV)

The **Peak Inverse Voltage** is the peak voltage across the diode in the reverse direction i.e. when the diode is reverse biased. In half wave rectifier, the load current is ideally zero when the diode is reverse biased and hence the maximum value of the voltage that can exist across the diode is nothing but E_{sm}. This is shown in the Fig. 1.48.

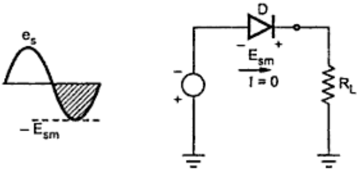


Fig. 1.48 PIV rating of diode

Thus PIV occurs at the peak of each negative half cycle of the input, when diode is reverse biased and not conducting.

$$\therefore \quad \boxed{\text{PIV of diode} = E_{sm} = \text{Maximum value of secondary voltage} = \pi E_{DC}\big|_{I_{DC}=0}}$$

This is called **PIV rating** of a diode. So diode must be selected based on this PIV rating and the circuit specifications.

1.25.12 Transformer Utilization Factor (T.U.F.)

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (T.U.F.).

Definition :

The T.U.F. is defined as the ratio of d.c. power delivered to the load to the a.c power rating of the transformer. While calculating the a.c. power rating, it is necessary to consider r.m.s. value of a.c. voltage and current.

The T.U.F. for half wave rectifier can be obtained as,

$$\text{A.C. power rating of transformer} = E_{RMS}\, I_{RMS}$$

$$= \frac{E_{sm}}{\sqrt{2}} \cdot \frac{I_m}{2} = \frac{E_{sm}\, I_m}{2\sqrt{2}}$$

Remember that the secondary voltage is purely sinusoidal hence its r.m.s. value is $1/\sqrt{2}$ times maximum while the current is half sinusoidal hence its r.m.s. value is 1/2 of the maximum, as derived earlier.

$$\text{D.C. power delivered to the load} = I_{DC}^2\, R_L$$

$$= \left(\frac{I_m}{\pi}\right)^2 R_L$$

$$\therefore \quad \boxed{\text{T.U.F.} = \frac{\text{D.C. Power delivered to the load}}{\text{A.C. Power rating of the transformer}}}$$

$$\therefore \quad \text{T.U.F.} = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{E_{sm} I_m}{2\sqrt{2}}\right)}$$

Neglecting the drop across R_f and R_s we can write,

$$E_{sm} = I_m R_L$$

$$\therefore \quad \text{T.U.F} = \frac{I_m{}^2}{\pi^2} \cdot \frac{R_L \cdot 2\sqrt{2}}{I_m{}^2 R_L} = \frac{2\sqrt{2}}{\pi^2} = \mathbf{0.287}$$

Key Point *: The value of T.U.F. is low which shows that in half wave circuit, the transformer is not fully utilized.*

1.25.13 Voltage Regulation

The secondary voltage should not change with respect to the load current. The voltage regulation is the factor which tells us about the change in the d.c. output voltage as load changes from no load to full load condition.

If $(V_{dc})_{NL}$ = D.C. voltage on no load

$(V_{dc})_{FL}$ = D.C. voltage on full load

then voltage regulation is defined as,

$$\boxed{\text{Voltage regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}} \qquad \dots (1)$$

Key Point : *Less the value of voltage regulation, better is the performance of rectifier circuit.*

For a half wave circuit,

$$(V_{dc})_{NL} = \frac{E_{sm}}{\pi}$$

While

$$(V_{dc})_{FL} = I_{DC}\,R_L = \frac{I_m}{\pi}\,R_L = \frac{E_{sm}}{\pi[R_f + R_s + R_L]} \times R_L$$

$$\therefore \qquad \% R = \frac{\dfrac{E_{sm}}{\pi} - \dfrac{E_{sm}}{\pi}\cdot\dfrac{R_L}{[R_f + R_s + R_L]}}{\dfrac{E_{sm}}{\pi}\cdot\dfrac{R_L}{R_f + R_s + R_L}} \times 100$$

$$= \frac{1 - \dfrac{R_L}{R_f + R_s + R_L}}{\dfrac{R_L}{R_f + R_s + R_L}} \times 100 = \frac{R_f + R_s}{R_L} \times 100$$

Neglecting winding resistance,

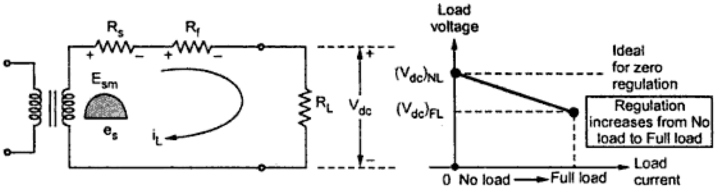
$$\boxed{\% R \approx \frac{R_f}{R_L} \times 100} \qquad \text{where } R_f = \text{Diode forward resistance}$$

Key Point : *Ideally the load regulation is zero as ideal value of R_f is zero in forward biased condition.*

1.25.13.1 Regulation Characteristics

Consider the equivalent circuit of the half wave rectifier, for positive half cycle of the transformer secondary voltage as shown in the Fig. 1.49 (a).

As load current increases (R_L decreases), the drop across R_s and R_f goes on increasing, but the transformer, secondary voltage remains same. Hence the d.c. output voltage decreases. Hence load voltage decreases as load changes from no load to full load. To keep the drop across R_s and R_f minimum, values of R_s and R_f. must be as small as possible. The graph of load voltage against load current is called **regulation characteristics** which is drooping in nature as shown in the Fig. 1.49 (b).



R_s
R_f
E_{sm}
e_s
i_L
R_L
V_{dc}
Load voltage
(V_{dc})_{NL}
(V_{dc})_{FL}
Ideal for zero regulation
Regulation increases from No load to Full load
0 No load → Full load
Load current

(a) Equivalent circuit

(b) Regulation characteristics

Fig. 1.49

1.25.14 Disadvantages of Half Wave Rectifier Circuit

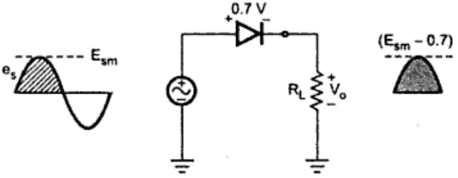
The various disadvantages of the half wave rectifier circuit are,

1. The ripple factor of half wave rectifier circuit is 1.21, which is quite high. The output contains lot of varying components.
2. The maximum theoretical rectification efficiency is found to be 40%. The practical value will be less than this. This indicates that half wave rectifier circuit is quite inefficient.
3. The circuit has low transformer utilization factor, showing that the transformer is not fully utilized.
4. The d.c. current is flowing through the secondary winding of the transformer which may cause dc saturation of the core of the transformer. To minimize the saturation, transformer size have to be increased accordingly. This increases the cost.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

1.25.15 Effect of Barrier Potential

Consider a half wave rectifier shown in the Fig. 1.50.



E_{sm}
e_s
0.7 V
+
−
R_L
V_o
(E_{sm} − 0.7)

Fig. 1.50 Effect of barrier potential

Due to the barrier potential of 0.7 V for Si diode, the peak value of the output is 0.7 V less than peak value of the input voltage

$$\therefore \quad \boxed{V_p(\text{output}) = E_{sm} - 0.7\text{ V}}$$

This effect is generally neglected as peak value of the input voltage is much greater than the barrier potential of 0.7 V. For Ge diodes, barrier potential is about 0.2 V which is very small and practically neglected.

➡ **Example 1.6 :** *A half wave rectifier circuit is supplied from a 230 V, 50 Hz supply with a step down ratio of 3:1 to a resistive load of 10 kΩ. The diode forward resistance is 75 Ω while transformer secondary resistance is 10 Ω. Calculate maximum, average, RMS values of current, D.C. output voltage, efficiency of rectification and ripple factor.*

Solution : The circuit is shown in the Fig. 1.51.

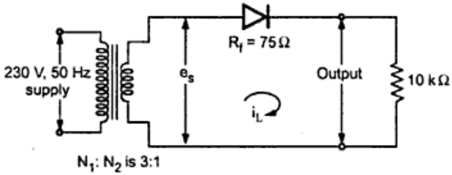


Fig. 1.51

The given values are,

$R_f = 75\ \Omega$, $R_L = 10\ \text{k}\Omega$, $R_s = 10\ \Omega$

The given supply voltages are always r.m.s. values.

$$E_p(\text{RMS}) = 230\text{ V}, \quad \frac{N_1}{N_2} = \frac{3}{1} \text{ i.e. } \frac{N_2}{N_1} = \frac{1}{3}$$

$$\frac{N_2}{N_1} = \frac{E_s(\text{RMS})}{E_p(\text{RMS})}$$

$$\therefore \quad \frac{1}{3} = \frac{E_s(\text{RMS})}{230}$$

$$\therefore \quad E_s(\text{RMS}) = 76.667\text{ V}$$

This is r.m.s. value of the transformer secondary voltage.

$$\therefore \quad E_{sm} = \sqrt{2}\,E_s(\text{RMS}) = \sqrt{2}\times 76.667 = 108.423\text{ V}$$

$$\therefore \quad I_m = \frac{E_{sm}}{R_s + R_f + R_L} = \frac{108.423}{10+75+10\times 10^3}$$

$$= \mathbf{10.75\ mA}$$

$$\therefore \quad I_{av} = I_{DC} = \frac{I_m}{\pi} = \frac{10.75}{\pi} = \mathbf{3.422\ mA}$$

$$I_{RMS} = \frac{I_m}{2} \quad \text{for half wave}$$

$$= \frac{10.75}{2} = \mathbf{5.375\ mA}$$

$$E_{DC} = \text{d.c output voltage} = I_{DC}\, R_L$$

$$= 3.422 \times 10^{-3} \times 10 \times 10^{3} = \mathbf{34.22\ V}$$

$$P_{DC} = \text{d.c. output power} = E_{DC}\, I_{DC} = 34.22 \times 3.422 \times 10^{-3}$$

$$= \mathbf{0.1171\ W}$$

This also can be obtained as,

$$P_{DC} = \frac{I_m^2}{\pi^2} R_L = \frac{\left(10.75 \times 10^{-3}\right)^2}{\pi^2} \times 10 \times 10^{3}$$

$$= \mathbf{0.1171\ W}$$

$$P_{AC} = \text{a.c. input power} = I_{RMS}^2 \left[R_s + R_f + R_L\right]$$

$$= \left(5.375 \times 10^{-3}\right)^2 \left[10 + 75 + 10 \times 10^{3}\right] = 0.2913\ \mathrm{W}$$

$$\therefore \quad \%\,\eta = \frac{P_{DC}}{P_{AC}} \times 100 = \frac{0.1171}{0.2913} \times 100 = \mathbf{40.19\%}$$

The ripple factor is constant for half wave rectifier and is 1.21.

$$\therefore \quad \gamma = \mathbf{1.21}$$

➡ **Example 1.7 :** *a) Assuming ideal diode, calculate the d.c. output voltage for the network shown in the Fig. 1.52.*

b) Repeat part (a) if the ideal diode is replaced by a silicon diode, having a cut-in voltage of 0.7 V. Neglect diode forward-resistance.

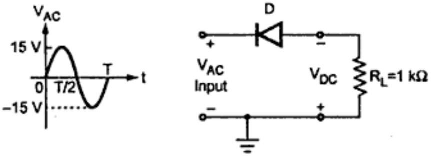


Fig. 1.52

Solution : In the circuit of the Fig. 1.52, the diode will be forward biased during negative half cycle of a.c. input voltage, and d.c. output voltage will be negative w.r.t. common ground terminal, as shown.

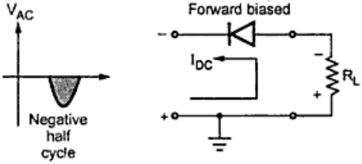


Fig. 1.52 (a)

a) For an ideal diode, cut-in voltage $V_\gamma = 0$, $R_f = 0$

$$\text{D.C. output voltage} = \frac{-\text{ Maximum value of a.c. input voltage}}{\pi}$$

$$= -\frac{15}{\pi} = -\mathbf{4.77\ V}$$

Negative sign indicates that voltage is negative w.r.t. ground.

b) For a silicon diode, $V_\gamma = 0.7$ V, R_f is assumed to be zero.

$$\therefore \quad \text{D.C. output voltage} = \frac{-[\text{ Maximum A.C. voltage} - V_\gamma\ ]}{\pi}$$

$$= \frac{-[15-0.7]}{\pi} = -\mathbf{4.55\ V}$$

➡ **Example 1.8 :** *A half wave rectifier with $R_L = 1$ kΩ is given an input of 10 V peak from step down transformer. Calculate D.C. voltage and load current for ideal and silicon diode.*

Solution : Given values are $R_L = 1$ kΩ, $V_m = 10$ V peak

Case i) Ideal diode

Cut-in voltage $V_\gamma = 0$ V, $R_f = 0\ \Omega$

$$\therefore \quad E_{DC} = \frac{V_m}{\pi} = \frac{10}{\pi} = \mathbf{3.18\ V}$$

$$\therefore \quad I_{DC} = \frac{E_{DC}}{R_L} = \frac{3.18}{1\times 10^3} = \mathbf{3.18\ mA}$$

Case ii) Silicon diode

$$\text{Cut-in voltage } V_\gamma = 0.7 \text{ V}$$

$$\therefore \quad E_{DC} = \frac{V_m - V_\gamma}{\pi} = \frac{10-0.7}{\pi} = \mathbf{2.96\ V}$$

$$\therefore \quad I_{DC} = \frac{E_{DC}}{R_L} = \mathbf{2.96\ mA}$$

1.26 Full Wave Rectifier

The full wave rectifier conducts during both positive and negative half cycles of input a.c. supply. In order to rectify both the half cycles of a.c. input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center tap transformer. The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

The full wave rectifier circuit is shown in the Fig. 1.53.

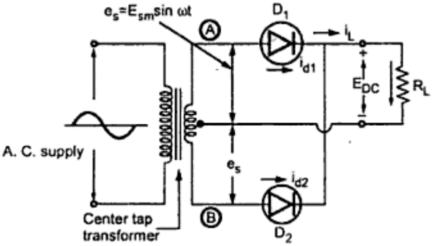
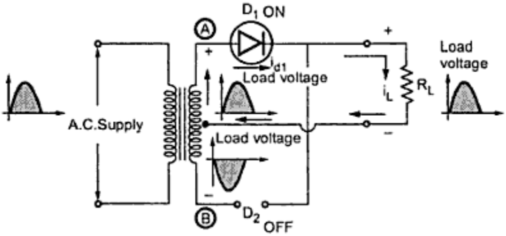


Fig. 1.53 Full wave rectifier

For the proper operation of the circuit, a center-tap on the secondary winding of the transformer is essential.

1.26.1 Operation of the Circuit

Consider the positive half cycle of a.c. input voltage in which terminal (A) is positive and terminal (B) negative. The diode D_1 will be forward biased and hence will conduct; while diode D_2 will be reverse biased and will act as an open circuit and will not conduct. This is illustrated in the Fig. 1.54.

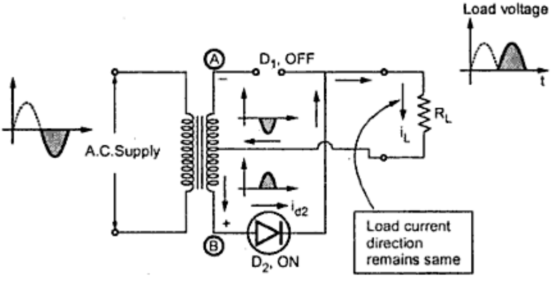


D1 ON
A
+
i_{d1}
Load voltage
A.C.Supply
Load voltage
-
B
D2 OFF
+
i_L
R_L
-
Load voltage

Fig. 1.54 Current flow during positive half cycle

The diode D_1 supplies the load current, i.e. $i_L = i_{d1}$. This current is flowing through upper half of secondary winding while the lower half of secondary winding of the transformer carries no current since diode D_2 is reverse biased and acts as an open circuit.

In the next half cycle of a.c. voltage, polarity reverses and terminal (A) becomes negative and (B) positive. The diode D_2 conducts, being forward biased, while D_1 does not, being reverse biased. This is shown in the Fig. 1.55.



Load voltage
t
A
D1, OFF
-
A.C.Supply
R_L
i_L
i_{d2}
+
B
D2, ON
Load current direction remains same

Fig. 1.55 Current flow during negative half cycle

The diode D_2 supplies the load current, i.e. $i_L = i_{d2}$. Now the lower half of the secondary winding carries the current but the upper half does not.

It is noted that the load current flows in both the half cycles of a.c. voltage and in the same direction through the load resistance. Hence we get rectified output across the load. The load current is sum of individual diode currents flowing in corresponding half cycles. It is also noted that the two diodes do not conduct simultaneously but in alternate half cycles.The individual diode currents and the load current are shown in the Fig. 1.56.

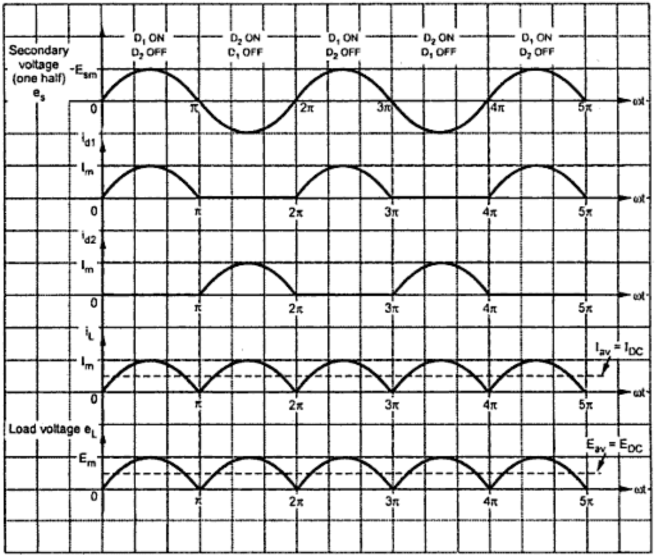


Fig. 1.56 Load current and voltage waveforms for full wave rectifier

Thus the full wave rectifier circuit essentially consists of two half-wave rectifier circuits working independently (working in alternate half cycles of a.c.) of each other but feeding a common load. The output load current is still pulsating d.c. and not pure d.c.

1.26.2 Maximum Load Current

Let R_f = forward resistance of diodes

R_s = winding resistance of each half of secondary

R_L = load resistance

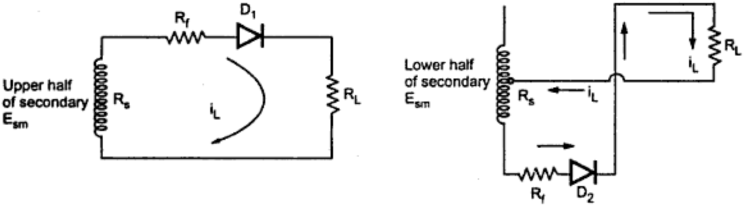
e_s = instantaneous a.c. voltage across each half of secondary

$$\therefore \quad \boxed{e_s = E_{sm} \sin \omega t}$$

$$\omega = 2\pi f$$

E_{sm} = maximum value of a.c. input voltage across each half of secondary winding

Hence we can write the expression for the maximum value of the load current, looking at equivalent circuit shown in the Fig 1.57.



(a) Fig. 1.57 (b)

$$\therefore \quad \boxed{I_m = \frac{E_{sm}}{R_s + R_f + R_L}}$$

where I_m = maximum value of load current i_L

1.26.3 Average D.C. Load Current (I_{DC})

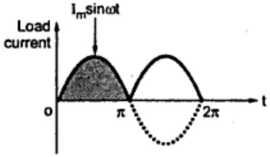


Fig. 1.58 Load current waveform

Consider one cycle of the load current i_L from 0 to π to obtain the average value which is d.c. value of load current.

$$i_L = I_m \sin \omega t \qquad 0 \le \omega t \le \pi$$

$$I_{av} = I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin \omega t \, d(\omega t)$$

$$\therefore \quad = \frac{I_m}{\pi}\left[(-\cos \omega t)_0^{\pi}\right]$$

$$= \frac{I_m}{\pi}[-\cos \pi - (-\cos 0)] \qquad \ldots \cos \pi = -1$$

$$= \frac{I_m}{\pi}(+1-(-1)]$$

$$\therefore \quad \boxed{I_{DC} = \frac{2I_m}{\pi}} \qquad \text{for full wave rectifier}$$

For half wave it is I_m/π and full wave rectifier is the combination of two half wave circuits acting alternately in two half cycles of input. Hence obviously the d.c. value for full wave circuit is $2\ I_m/\pi$.

1.26.4 Average D.C. Load Voltage (E_{DC})

The d.c. load voltage is,

$$E_{DC} = I_{DC}R_L = \frac{2I_m R_L}{\pi}$$

Substituting value of I_m,

$$E_{DC} = \frac{2\,E_{sm}\ R_L}{\pi\left[R_f + R_s + R_L\right]} = \frac{2\,E_{sm}}{\pi\left[1 + \frac{R_f + R_s}{R_L}\right]}$$

But as R_f and $R_s << R_L$ hence $\frac{R_f + R_s}{R_L} << 1$

$$\therefore \quad \boxed{E_{DC} = \frac{2E_{sm}}{\pi}}$$

1.26.5 RMS Load Current (I_{RMS})

The R.M.S. value of current can be obtained as follows :

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 d(\omega t)}$$

Since two half wave rectifier are similar in operation we can write,

$$I_{RMS} = \sqrt{\frac{2}{2\pi}\int_0^{\pi} [I_m \sin \omega t]^2 d(\omega t)}$$

$$= I_m\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{1-\cos 2\omega t}{2}\right]d(\omega t)} \qquad \text{as } \sin^2 \omega t = \frac{1-\cos 2\,\omega t}{2}$$

$$\therefore \quad I_{RMS} = I_m\sqrt{\frac{1}{2\pi}\left[[\omega t]_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]} = I_m\sqrt{\frac{1}{2\pi}[\pi - 0]}$$

$$= I_m\sqrt{\frac{1}{2\pi}(\pi)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$\therefore \quad \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

1.26.6 R.M.S. Value of the Load Voltage

As the load is resistive, the r.m.s. value of the load voltage is given by,

$$\therefore \quad \boxed{E_{L\,(RMS)} = I_{RMS}\,R_L = \frac{I_m}{\sqrt{2}}\,R_L}$$

1.26.7 D.C. Power Output (P_{DC})

$$\text{D.C. Power output} = E_{DC}I_{DC} = I_{DC}^2\,R_L$$

$$\therefore \quad P_{DC} = I_{DC}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$\therefore \quad P_{DC} = \frac{4}{\pi^2}\,I_m^2\,R_L$$

Substituting value of I_m we get,

$$\therefore \quad \boxed{P_{DC} = \frac{4}{\pi^2}\,\frac{E_{sm}^2}{\left(R_s + R_f + R_L\right)^2} \times R_L}$$

Key Point : *Instead of remembering this formula, students can use the expression* $E_{DC}\,I_{DC}$ *or* $I_{DC}^2 R_L$ *to calculate* P_{DC} *while solving the problems.*

1.26.8 A.C. Power Input (P_{AC})

The a.c. power input is given by,

$$\therefore \quad \boxed{P_{AC} = I_{RMS}^2\left(R_f + R_s + R_L\right) = \left(\frac{I_m}{\sqrt{2}}\right)^2\left(R_f + R_s + R_L\right)}$$

$$\therefore \quad P_{AC} = \frac{I_m^2\left(R_f + R_s + R_L\right)}{2}$$

Substituting value of I_m we get,

$$\therefore \quad P_{AC} = \frac{E_{sm}^2}{\left(R_f + R_s + R_L\right)^2} \times \frac{1}{2} \times \left(R_f + R_s + R_L\right)$$

$$\therefore \quad \boxed{P_{AC} = \frac{E_{sm}^2}{2\left(R_f + R_s + R_L\right)}}$$

1.26.9 Rectifier Efficiency (η)

$$\therefore \quad \boxed{\eta = \frac{P_{DC}\text{ output}}{P_{AC}\text{ input}}}$$

$$\therefore \quad \eta = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}}$$

$$\therefore \quad \eta = \frac{8\ R_L}{\pi^2 (R_f + R_s + R_L)}$$

But if $R_f + R_s << R_L$, neglecting it from denominator

$$\eta = \frac{8\ R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2}$$

$$\therefore \quad \boxed{\%\ \eta_{max} = \frac{8}{\pi^2} \times 100 = \mathbf{81.2\ \%}}$$

This is the maximum theoretical efficiency of full wave rectifier.

1.26.10 Ripple Factor (γ)

As derived earlier in case of half wave rectifier the ripple factor is given by a general expression,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

For full wave $I_{RMS} = I_m / \sqrt{2}$ and $I_{DC} = 2I_m / \pi$ so,

substituting in the above equation,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_m / \sqrt{2}}{2I_m / \pi}\right]^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\therefore \quad \boxed{\text{Ripple factor} = \gamma = 0.48}$$

Key Point : *This indicates that the ripple contents in the output are 48 % of the d.c. component which is much less than that for the half wave circuit.*

1.26.11 Load Current (i_L)

The Fourier series for the load current is obtained by taking the sum of the series for the individual rectifier current. The two diodes conduct in alternate half cycles, i.e. there is a phase difference of π radians between two diode currents. Hence,

$$i_{d_1} = I_m\left[\frac{1}{\pi}+\frac{1}{2}\sin\omega t-\frac{2}{3\pi}\cos 2\omega t-\frac{2}{15\pi}\cos 4\omega t...\right]$$

and $$i_{d_2} = i_{d_1} \text{ with } \omega t \text{ replaced by } (\omega t+\pi)$$

$$\therefore \quad i_{d_2} = I_m\left[\frac{1}{\pi}+\frac{1}{2}\sin(\omega t+\pi)-\frac{2}{3\pi}\cos 2(\omega t+\pi)-\frac{2}{15\pi}\cos 4(\omega t+\pi)...\right]$$

$$= I_m\left[\frac{1}{\pi}-\frac{1}{2}\sin\omega t-\frac{2}{3\pi}\cos(2\omega t+2\pi)-\frac{2}{15\pi}\cos(4\omega t+4\pi)...\right]$$

$$= I_m\left[\frac{1}{\pi}-\frac{1}{2}\sin\omega t-\frac{2}{3\pi}\cos 2\omega t-\frac{2}{15\pi}\cos 4\omega t...\right]$$

Then the Fourier series for the load current is,

$$i_L = i_{d_1}+i_{d_2} = I_m\left[\frac{2}{\pi}-\frac{4}{3\pi}\cos 2\omega t-\frac{4}{15\pi}\cos 4\omega t\cdots\right]$$

The first term in the above series represents the average or d.c. value, while the remaining terms "ripple". It is seen that the lowest frequency of the ripple is 2f, i.e. twice the supply frequency of a.c. supply. The lowest ripple frequency in the load current of the full-wave connection, is double than that in the half-wave connection.

As seen from the Fig. 1.54 and Fig 1.55 the individual diode currents are flowing in opposite directions through the two halves of the secondary winding. Hence the net secondary current will be difference of individual diode currents.

Thus, $$\boxed{i_{sec} = i_{d_1}-i_{d_2}}$$

The Fourier series of i_{sec} is obtained by the difference between the series of individual diode currents. Using above relations we can write,

$$i_{sec} = I_m \sin\omega t$$

Hence under ideal conditions, the secondary current is purely sinusoidal. No d.c. component flows through the secondary hence there is no danger of saturation. This reduces the transformer losses and overall size and cost of the circuit. Thus the **transformer gets utilised effectively.**

1.26.12 Peak Inverse Voltage (PIV)

It can be observed from the circuit diagram that when the diode is reversed biased then full transformer secondary voltage gets impressed across it. The drop across conducting diode is assumed zero. Thus the peak value of the inverse voltage to which diode gets subjected is voltage across both the parts of the transformer secondary. This is shown in the Fig. 1.59.

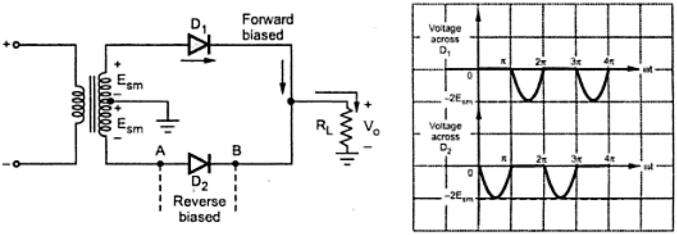


Fig. 1.59 PIV rating of diodes

It can be seen that when D_2 is reverse biased, point A is at $-E_{sm}$ with respect to ground while point B is at $+E_{sm}$ with respect to ground, neglecting diode drop. Thus total peak voltage across D_2 is $2E_{sm}$.

$$\therefore \quad \boxed{\text{PIV of diode} = 2\,E_{sm} = \pi E_{DC}\big|_{I_{DC}=0}}$$

where E_{sm} = maximum value of a.c. voltage across half the secondary of transformer.

If the diode drop is considered to be 0.7 V then the PIV of reverse biased diode is,

$$\boxed{\text{PIV of diode} = 2E_{sm} - 0.7}$$

This is because only one diode conducts at a time.

1.26.13 Transformer Utilization Factor (T.U.F.)

In full wave rectifier, the secondary current flows through each half separately in every half cycle. While the primary of transformer carries current continuously. Hence T.U.F is calculated for primary and secondary windings separately and then the average T.U.F. is determined.

$$\text{Secondary T.U.F} = \frac{\text{D.C. power to the load}}{\text{A.C. power rating of secondary}}$$

$$= \frac{I_{DC}^2\,R_L}{E_{RMS}\,I_{rms}} = \frac{\left(\frac{2}{\pi}I_m\right)^2 R_L}{\frac{E_{sm}}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

Neglecting forward resistance R_f of diode, $E_{sm} \approx I_m R_L$.

$$\therefore \quad \text{Secondary T.U.F.} = \frac{\frac{4}{\pi^2} \times I_m{}^2\,R_L}{\frac{I_m{}^2\,R_L}{2}} = \frac{8}{\pi^2} = 0.812$$

The primary of the transformer is feeding two half-wave rectifiers separately. These two half wave rectifiers work independently of each other but feed a common load. We have already derived the T.U.F. for half wave circuit to be equal to 0.287. Hence

$$\text{T.U.F. for primary winding} = 2 \times \text{T.U.F. of half wave circuit}$$

$$= 2 \times 0.287 = 0.574.$$

The average T.U.F for full wave circuit will be

$$\begin{array}{l}\text{Average T.U.F. for}\\ \text{full wave rectifier circuit}\end{array} = \frac{\text{T.U.F of primary} + \text{T.U.F of secondary}}{2}$$

$$= \frac{0.574 + 0.812}{2} = \mathbf{0.693}$$

∴ $\boxed{\text{Average T.U.F. for full wave rectifier} = 0.693}$

Key Point : *Thus in full wave circuit transformer gets utilized more than the half wave rectifier circuit.*

1.26.14 Voltage Regulation

For a full wave circuit,

$$(V_{dc})_{NL} = \frac{2E_{sm}}{\pi} \quad \text{... (1)}$$

and $$(V_{dc})_{FL} = I_{DC} R_L \quad \text{... (2)}$$

The regulation can be expressed as,

$$\% R = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

$$\boxed{\% R = \frac{\frac{2E_{sm}}{\pi} - I_{DC} R_L}{I_{DC} R_L} \times 100}$$

Now $$I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

∴ $$E_{sm} = I_m(R_f + R_L + R_s)$$

and $$I_{DC} = \frac{2I_m}{\pi}$$

∴ $$\% R = \frac{\frac{2I_m}{\pi}[R_f + R_L + R_s] - \frac{2I_m}{\pi} R_L}{\frac{2I_m}{\pi} R_L} \times 100$$

$$= \frac{R_f + R_L + R_s - R_L}{R_L} \times 100$$

$$\therefore \qquad \boxed{\% \, R = \frac{R_f + R_s}{R_L} \times 100}$$

Neglecting winding resistance R_s, the regulation can be expressed as,

$$\boxed{\% \, R \approx \frac{R_f}{R_L} \times 100}$$

where R_f = forward resistance of the diode.

The regulation characteristics is drooping, as discussed earlier in case of half wave rectifier as **output voltage decreases as load increases from no load to full load.**

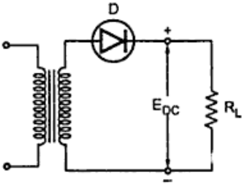
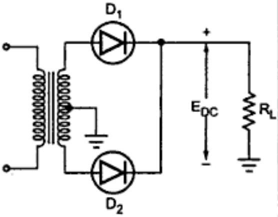
1.26.15 Advantages of Full Wave Rectifier

1. The d.c. load voltage and current are more than half wave.
2. No d.c. current through transformer windings hence no possibility of saturation.
3. T.U.F. is better as transformer losses are less.
4. The efficiency is higher.
5. The large d.c. power output.
6. The ripple factor is less.

1.26.16 Disadvantages of Full Wave Rectifier

1. The PIV rating of diode is higher.
2. Higher PIV diodes are larger in size and costlier.
3. The cost of centre tap transformer is higher.

1.26.17 Comparison of Half Wave and Full Wave Rectifiers

	Half Wave	**Full Wave**
1. Circuit		

2. E_{DC}	$E_{DC} = \frac{E_{sm}}{\pi}$	$E_{DC} = \frac{2E_{sm}}{\pi}$, Higher
3. I_{DC}	$I_{DC} = \frac{I_m}{\pi}$	$I_{DC} = \frac{2I_m}{\pi}$, Higher
4. P_{DC}	$P_{DC} = \frac{I_m^2}{\pi^2} R_L$	$P_{DC} = \frac{4I_m^2}{\pi^2} R_L$, Four times higher
5. % η_{max}	40.6 %	81.2 %
6. Ripple factor	$\gamma = 1.211$	$\gamma = 0.48$, Ripple contents are less
7. Ripple frequency	f = 50 Hz	f = 100 Hz, Higher ripple frequency reduces the size of filter components, reducing the cost.
8. PIV	PIV = E_{sm}	PIV = 2 E_{sm}, Large rating diodes are. required.
9. Transformer	Normal is required	Center tap is required so cost is high.
10. T.U.F.	T.U.F. = 0.287	T.U.F. = 0.693, transformer gets more utilized.
11. Core saturation	Transformer core saturation possible	No d.c. current through transformer so core saturation not possible.

➡ **Example 1.9 :** *A full wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from either end of secondary to center tap is 30 V. If the diode forward resistance is 2 Ω and that of the half secondary is 8 Ω, for a load of 1 kΩ, calculate,*

a) Power delivered to load, *b) % Regulation at full load,*
c) Efficiency of rectification, *d) T.U.F. of secondary.*

Solution : Given : $E_s = 30\,V$, $R_f = 2\Omega$, $R_s = 8\Omega$, $R_L = 1k\Omega$

$$E_s = E_{RMS} = 30\ V$$

$$E_{sm} = E_s\sqrt{2} = 30\sqrt{2}\ \text{volt} = 42.426\ V$$

$$I_m = \frac{E_{sm}}{R_f + R_L + R_s} = \frac{30\sqrt{2}}{2+1000+8}\ A = 42\ mA$$

$$I_{DC} = \frac{2}{\pi} I_m = 26.74\ mA$$

a) Power delivered to the load $= I_{DC}^2\ R_L = (26.74 \times 10^{-3})^2\ (1\text{k}\Omega)$

$= \mathbf{0.715\ W}$

b) $$V_{DC}\text{, no load} = \frac{2}{\pi}\ E_{sm} = \frac{2}{\pi} \times 30\sqrt{2} = 27\text{ V}$$

$$V_{DC}\text{, full load} = I_{DC}\ R_L = (26.74\text{ mA})\ (1\text{ k}\Omega)$$

$$= 26.74\text{ V}$$

$$\%\text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{27 - 26.74}{26.74} \times 100$$

$$= \mathbf{0.97\ \%}$$

c) $$\text{Efficiency of rectification} = \frac{\text{D.C. output}}{\text{A.C. input}}$$

$$= \frac{8}{\pi^2} \times \frac{1}{1 + \dfrac{R_f + R_s}{R_L}} = \frac{8}{\pi^2} \times \frac{1}{1 + \dfrac{(2+8)}{1000}}$$

$= 0.802$ **i.e. 80.2%**

d) $$\text{Transformer secondary rating} = E_{RMS}\ I_{RMS} = [30\text{ V}]\left[\frac{42\text{ mA}}{\sqrt{2}}\right]$$

$= \mathbf{0.89\ W}$

∴ $$\text{T.U.F.} = \frac{\text{D.C. power output}}{\text{A.C. rating}}$$

$$= \frac{0.715}{0.89} = 0.802$$

Example 1.10 : *For the full-wave rectifier circuit shown in the Fig. 1.60, V is a sinusoidal voltage. If the maximum allowable average d.c. current in each diode is 1 A, calculate the maximum allowable peak-to-peak value of V. Assume two diodes to be identical, and neglect diode resistance in forward direction.*

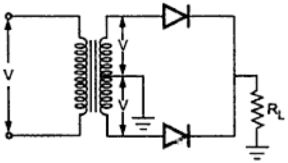


Fig. 1.60

Solution : Given : F.W. rectifier with $R_L = 100\ \Omega$, A.C. input voltage is V.

Let V_m is maximum value or amplitude of sinusoidal voltage, across **each half** of the secondary winding.

$$\text{Maximum } I_{DC} \text{ for each diode } = 1\text{ A}$$

A full wave rectifier essentially consists of two independent half wave rectifiers feeding a common load.

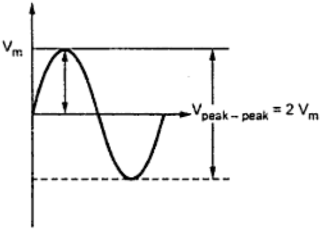


Fig. 1.60 (a)

The average I_{DC} per H.W. rectifier diode

$$= \frac{1}{\pi} I_m = \frac{1}{\pi} \frac{V_m}{R_L} \qquad \text{where } I_m = \frac{V_m}{R_L} \text{ as } R_f = 0$$

$$\therefore \quad 1\text{A} = \frac{1}{\pi} \frac{V_m}{R_L}$$

$$\therefore \quad V_m = \pi R_L = \pi \times 100$$

$$= 314.16 \text{ V}$$

$$\therefore \quad V_{\text{peak to peak}} = V_{max} \times 2$$

$$= 628.32 \text{ V}$$

Example 1.11 : *A full wave rectifier uses a diode with forward resistance of 1 Ω. The transformer secondary is centre tapped with output 10-0-10 V_{rms} and has resistance of 5 Ω for each half section. Calculate*

i) No-load d.c. voltage

ii) D.C. output voltage at 100 mA

iii) % Regulation at 100 mA

Solution : $R_f = 1\ \Omega,\ E_s(\text{rms}) = 10\text{ V},\ R_s = 5\ \Omega$

$$E_{sm} = \sqrt{2}\, E_s(\text{rms}) = \sqrt{2} \times 10 = 14.1421 \text{ V}$$

i) $$E_{DC}(NL) = \frac{2E_{sm}}{\pi} = 2\times\frac{14.1421}{\pi}$$

$$= \mathbf{9.0031\ V}$$

ii) $$I_{DC} = 100\ mA = \frac{2I_m}{\pi}$$

∴ $$I_m = \frac{\pi\times 100}{2} = 157.079\ mA$$

But $$I_m = \frac{E_{sm}}{R_f + R_s + R_L}$$

∴ $$157.079\times 10^{-3} = \frac{14.1421}{1+5+R_L}$$

∴ $$R_L = \mathbf{84.0317\ \Omega}$$

∴ $$E_{DC}(\text{on load}) = I_{DC}R_L = 100\times 10^{-3}\times 84.0317$$

$$= \mathbf{8.4031\ V}$$

iii) $$\%\ \text{Regulation} = \frac{E_{DC}(NL) - E_{DC}(\text{on load})}{E_{DC}(\text{on load})}\times 100$$

$$= \frac{9.0031 - 8.4031}{8.4031}\times 100$$

$$= \mathbf{7.14\ \%}$$

Example 1.12 : *What is the necessary A.C. input power from the transformer secondary used in a half wave rectifier to deliver 500 W of D.C. power to the load ? What would be the A.C. input power for the same load in a full wave rectifier ?*

Solution : P_{DC} = 500 W, Half wave rectifier

For half wave rectifier, $\%\,\eta = 40.6\%$ ... (Assuming maximum)

∴ $$40.6 = \frac{P_{DC}}{P_{AC}}\times 100$$

∴ $$40.6 = \frac{500}{P_{AC}}\times 100$$

∴ $$P_{AC} = \mathbf{1231.527\ W}$$

For the same load, with full wave rectifier the maximum rectifier efficiency is 81.2%.

∴ $$81.2 = \frac{500}{P_{AC}}\times 100$$

∴ $$P_{AC} = \mathbf{615.76355\ W}$$

1.27 Bridge Rectifier

The basic bridge rectifier circuit is shown in Fig. 1.61.

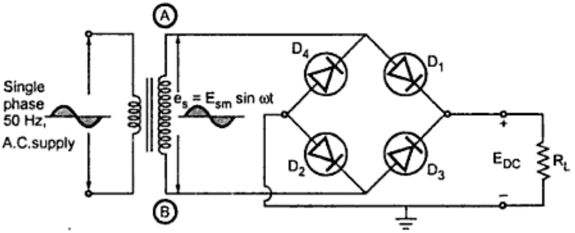


Fig. 1.61 Bridge rectifier circuit

The bridge rectifier circuit is essentially a **full-wave rectifier circuit, using four diodes,** forming the four arms of an electrical bridge. To one diagonal of the bridge, the a.c. voltage is applied through a transformer if necessary, and the rectified d.c. voltage is taken from the other diagonal of the bridge. The main advantage of this circuit is that it does not require a center tap on the secondary winding of the transformer. Hence wherever possible, a.c. voltage can be directly applied to the bridge.

1.27.1 Operation of the Circuit

Consider the positive half of a.c. input voltage. The point A of secondary becomes positive. The diodes D_1 and D_2 will be forward biased, while D_3 and D_4 reverse biased. The two diodes D_1 and D_2 conduct in series with the load and the current flows as shown in Fig. 1.62.

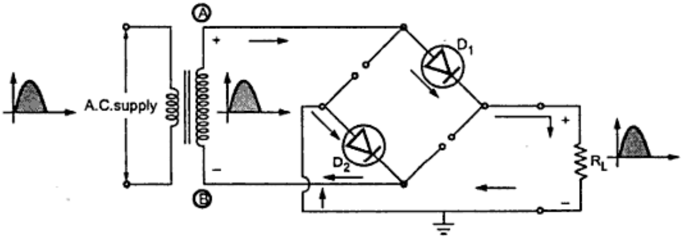


Fig. 1.62 Current flow during positive half cycle

In the next half cycle, when the polarity of a.c. voltage reverses hence point B becomes positive diodes D_3 and D_4 are forward biased, while D_1 and D_2 reverse biased. Now the diodes D_3 and D_4 conduct is series with the load and the current flows as shown in Fig. 1.63.

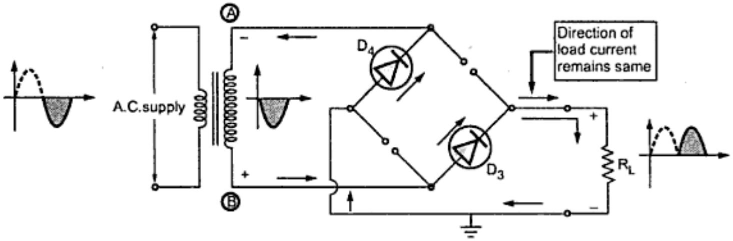


Fig. 1.63 Current flow during negative half cycle

It is seen that in both cycles of a.c., the load current is flowing in the same direction hence, we get a full wave rectified output.

The waveforms of load current and voltage remain exactly same as shown in the Fig. 1.64. (see Fig. 1.64 on next page).

1.27.2 Expressions for Various Parameters

The bridge rectifier circuit, being basically a full wave rectifier circuit; all the characteristic discussed previously for a full wave circuit using two diodes, are the characteristic of a bridge rectifier circuit.

The relation between I_m the maximum value of load current and I_{DC} , I_{RMS} remains same as derived earlier for the full wave rectifier circuit.

$$\boxed{I_{DC} = \frac{2I_m}{\pi} \quad \text{and} \quad I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

The expression for I_m will change slightly. This will be clear from the equivalent circuit shown in the Fig. 1.65.

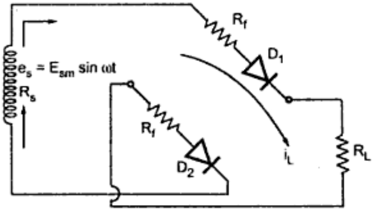


Fig. 1.65

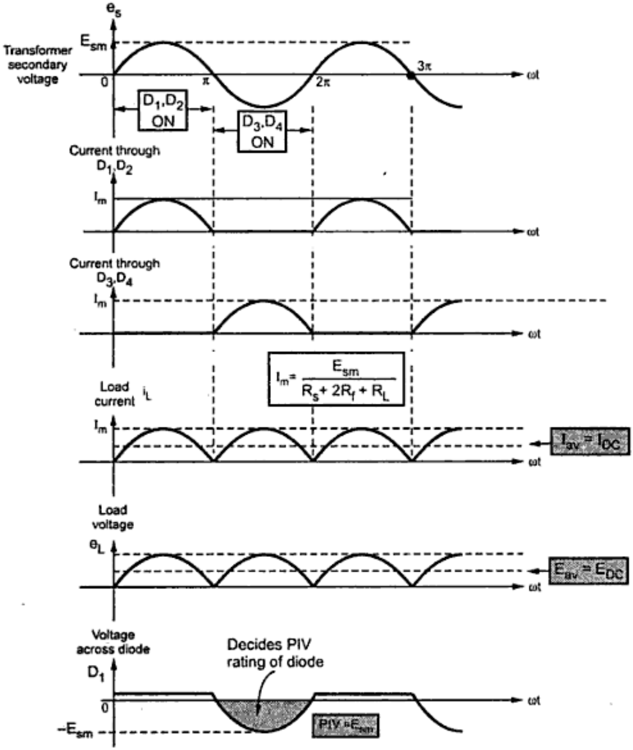

e_s
Transformer secondary voltage
E_sm
0
π
2π
3π
ωt
D1,D2 ON
D3,D4 ON
Current through D1,D2
I_m
ωt
Current through D3,D4
I_m
ωt
I_m = E_sm / (R_s + 2R_f + R_L)
Load current i_L
I_m
ωt
I_av = I_DC
Load voltage
e_L
ωt
E_av = E_DC
Voltage across diode D1
0
-E_sm
ωt
Decides PIV rating of diode
PIV = E_sm

Fig. 1.64 Waveforms of bridge rectifier

In each half cycle two diodes conduct simultaneously. Hence maximum value of load current is,

$$\boxed{I_m = \frac{E_{sm}}{R_s + 2R_f + R_L}}$$

So the only modification is that instead of R_f , which is forward resistance of each diode, the term **2 R_f appears in the denominator.**

The remaining expressions are identical to those derived for two diode full wave rectifier and reproduced for the convenience of the reader.

$$E_{DC} = I_{DC} R_L = \frac{2E_{sm}}{\pi}$$

$$P_{DC} = I_{DC}^2 R_L = \frac{4}{\pi^2} I_m^2 R_L$$

$$P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L) = \frac{I_m^2 (2R_f + R_s + R_L)}{2}$$

$$\eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}, \quad \% \eta_{max} = 81.2\%$$

$$\gamma = 0.48$$

Key Point : *The E_{sm} is the maximum value of a.c. voltage across full secondary winding of the transformer used.*

As the current flows through the entire secondary of the transformer for all the time, the transformer utilization factor is 0.812. This is more than the T.U.F for full wave rectifier circuit.

1.27.3 PIV Rating of Diodes

The reverse voltage appearing across the reverse biased diodes is $2E_{sm}$ but two diodes are sharing it. Hence **PIV rating of the diode is E_{sm}** and not 2 E_{sm} as in case of full wave rectifier.

1.27.4 What Happens if Input and Output Terminals are Reversed?

The bridge rectifier can be represented in a simplified way as shown in the Fig. 1.66.

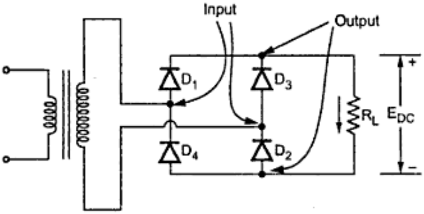


Fig. 1.66

For positive half cycle of input D_1, D_2 conduct while for negative half cycle D_3, D_4 conduct.

It can be noted that if **input and output terminals in bridge rectifier are reversed** without any change in diodes then it will not work. For one cycle, supply will get shorted through the forward biased diodes across the supply while for other cycle the circuit will be open. **The output will be zero.**

1.27.5 Advantages of Bridge Rectifier Circuit

1) The current in both the primary and secondary of the power transformer flows for the entire cycle and hence for a given power output, power transformer of a small size and less cost may be used.

2) No center tap is required in the transformer secondary. Hence, wherever possible, a.c. voltage can directly be applied to the bridge.

3) The current in the secondary of the transformer is in opposite direction in two half cycles. Hence net d.c. component flowing is zero which reduces the losses and danger of saturation.

4) Due to pure alternating current in secondary of transformer, the transformer gets utilised effectively and hence the circuit is suitable for applications where large powers are required.

5) As two diodes conduct in series in each half cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage applications. Such a peak reverse voltage appearing across diode is called peak inverse voltage rating (PIV) of diode.

1.27.6 Disadvantages of Bridge Rectifier

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This causes additional voltage drop as indicated by term $2R_f$ present in expression of I_m instead of R_f . This reduces the output voltage.

1.27.7 Applications

1. Used as rectifier in power circuits to convert a.c. to d.c.
2. In rectifier type meters, to convert a.c. voltage to be measured to d.c.
3. In power supply circuits.

➡ **Example 1.13 :** *The four semiconductor diodes used in a bridge rectifier circuit each having a forward resistance of 0.1 Ω and infinite reverse resistance, feed a d.c. current of 10 A to a resistive load from a sinusoidally varying alternating supply of 30 V (r.m.s). Determine the resistance of the load and the efficiency of the circuit.*

Solution : The given values are,

$$R_f = 0.1\ \Omega\ ,\ I_{DC} = 10\ \text{A},\ R_s = 0\ \Omega\ ,\ E_s(\text{R.M.S.}) = 30\ \text{V}$$

Now $$E_{sm} = E_{sm}(\text{R.M.S.}) \times \sqrt{2} = \sqrt{2} \times 30$$

$$= 42.4264\ \text{V}$$

$$I_{DC} = \frac{2I_m}{\pi}$$

∴ $$I_m = \frac{\pi \times I_{DC}}{2} = \frac{\pi \times 10}{2}$$

$$= 15.7079\ \text{A}$$

Now $$I_m = \frac{E_{sm}}{2R_f + R_s + R_L}$$

∴ $$15.7079 = \frac{42.4264}{2 \times 0.1 + R_L}$$

∴ $$R_L + 0.2 = 2.7$$

∴ $$R_L = \mathbf{2.5\ \Omega}$$

Now $$P_{DC} = I_{DC}^2 R_L = \left(10^2\right) \times 2.5 = 250\ \text{W}$$

$$P_{AC} = I_{RMS}^2\left(2R_f + R_s + R_L\right)$$

and $$I_{RMS} = \frac{I_m}{\sqrt{2}} = \frac{15.7079}{\sqrt{2}} = 11.1071\ \text{A}$$

∴ $$P_{AC} = (11.1071)^2\ [\,2 \times 0.1 + 2.5] = 333.092\ \text{W}$$

∴ $$\%\,\eta = \frac{P_{DC}}{P_{AC}} \times 100 = \frac{250}{333.092} \times 100$$

$$= \mathbf{75.05\ \%}$$ ... Rectifier efficiency

Example 1.14 : *A 5 kΩ load is fed from a bridge rectifier connected across a tranformer secondary whose primary is connected to 460 V, 50 Hz supply. The ratio of number of primary turns to secondary turns is 2:1.*
Calculate d.c. load current, d.c. load voltage, ripple voltage and P.I.V. rating of diode.

Solution : $R_L = 5\ \text{k}\Omega = 5\times 10^3\ \Omega$, $N_1 : N_2$ is 2:1

$$E_p = 460\ \text{V} \quad \text{RMS value}$$

$$\therefore \quad \frac{E_s}{E_p} = \frac{N_2}{N_1} = \frac{1}{2}$$

$$\therefore \quad E_s = \frac{1}{2}\times E_p = 230\ \text{V}$$

$$\therefore \quad E_{sm} = \sqrt{2}\times E_s = 230\times\sqrt{2} = 325.269\ \text{V.}$$

now

$$I_{DC} = \frac{2\,I_m}{\pi} \qquad \text{where } I_m = \frac{E_{sm}}{R_L} \text{ neglecting } R_f.$$

$$\therefore \quad I_{DC} = \frac{2\,E_{sm}}{\pi R_L} = \frac{2\times 325.269}{\pi\times 5\times 10^3} = \mathbf{41.41\ mA}$$

$$\text{D.C. load voltage } E_{DC} = I_{DC}\times R_L = 41.41\times 10^{-3}\times 5\times 10^3$$

$$= \mathbf{207.072\ V}$$

$$\text{Ripple voltage} = \text{Ripple factor}\times V_{DC}$$

Ripple factor for bridge rectifier is 0.482.

$$\therefore \quad \text{Ripple voltage} = 0.482\times 207.072 = \mathbf{99.8\ V}$$

$$\text{P.I.V. rating of each diode} = E_{sm} \text{ for bridge rectifier } = \mathbf{325.27\ V}$$

Example 1.15 : *A full wave bridge rectifier is supplied from 230 V, 50 Hz and uses a transformer of turns ratio of 15 : 1. It uses load resistance of 50 Ω. Calculate load voltage and ripple voltage. Assume ideal diode and transformer. Assume standard value of ripple factor for full wave rectifier.*

Solution :

$$E_p\,(\text{rms}) = 230\ \text{V},\ \frac{N_2}{N_1} = \frac{1}{15},\ R_L = 50\ \Omega$$

$$R_f = R_s = 0\ \Omega \quad \text{as ideal}$$

Now

$$\frac{E_p\,(\text{rms})}{E_s\,(\text{rms})} = \frac{N_1}{N_2}$$

$$\therefore \quad E_s\,(\text{rms}) = \frac{N_2}{N_1} \times E_P\,(\text{rms}) = \frac{1}{15} \times 230 = 15.333 \text{ V}$$

$$\therefore \quad E_{sm} = \sqrt{2}\;\; E_s\,(\text{rms}) = 21.684 \text{ V}$$

$$\therefore \quad I_m = \frac{E_{sm}}{R_s + 2\;R_f + R_L} = \frac{21.684}{50} = 0.4336 \;\; \text{A}$$

$$\therefore \quad I_{DC} = \frac{2\;I_m}{\pi} = \frac{2 \times 0.4336}{\pi} = 0.276 \;\; \text{A}$$

$$\therefore \quad E_{DC} = \text{Load voltage} = I_{DC}\;\; R_L \;=\; 0.276 \times 50 = \mathbf{13.8} \;\; \text{V}$$

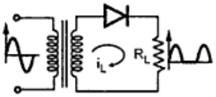
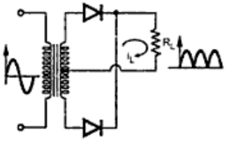
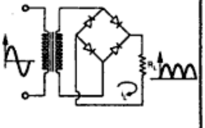
$$\text{Ripple factor} = 0.482 \qquad \text{... For full wave rectifier}$$

$$\text{Ripple factor} = \frac{\text{a.c. rms output}}{\text{d.c. output}} = \frac{\text{ripple voltage}}{E_{DC}}$$

$$\therefore \quad 0.482 = \frac{\text{ripple voltage}}{13.8}$$

$$\therefore \quad \text{Ripple voltage} = 13.8 \times 0.482 = \mathbf{6.6516} \;\; \text{V}$$

1.28 Comparison of Rectifier Circuits

Circuit Diagrams		
Half Wave	**Full Wave**	**Bridge**
		

Sr. No.	Parameter	Half Wave	Full Wave	Bridge
1.	Number of diodes	1	2	4
2.	Average D.C. current (I_{DC})	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3.	Average D.C. voltage (E_{DC})	$\frac{E_{sm}}{\pi}$	$\frac{2E_{sm}}{\pi}$	$\frac{2E_{sm}}{\pi}$
4.	RMS current (I_{RMS})	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
5.	D.C. power output (P_{DC})	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4}{\pi^2} I_m^2 R_L$	$\frac{4}{\pi^2} I_m^2 R_L$

6.	A.C. power input (P_{AC})	$\frac{I_m^2(R_L+R_f+R_s)}{4}$	$\frac{I_m^2(R_f+R_s+R_L)}{2}$	$\frac{I_m^2(2R_f+R_s+R_L)}{2}$
7.	Maximum rectifier efficiency (η)	40.6 %	81.2 %	81.2 %
8.	Ripple factor (γ)	1.21	0.482	0.482
9.	Maximum load current (I_m)	$\frac{E_{sm}}{R_s+R_f+R_L}$	$\frac{E_{sm}}{R_s+R_f+R_L}$	$\frac{E_{sm}}{R_s+2R_f+R_L}$
10.	PIV rating of diode	E_{sm}	2 E_{sm}	E_{sm}
11.	Ripple frequency	50 Hz	100 Hz	100 Hz
12.	T.U.F.	0.287	0.693	0.812

1.29 Filter Circuits

It is seen that the output a half-wave or full wave rectifier circuit is not pure d.c.; but it contains fluctuations or ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load, as shown in the Fig. 1.67.

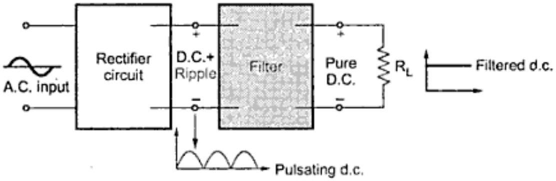


Fig. 1.67 Power supply using rectifier and filter

An a.c. input is applied to the rectifier. At the output of the rectifier, there will be d.c. and ripple voltage present, which is the input to the filter. Ideally the output of the filter should be pure d.c. Practically, the filter circuit will try to minimize the ripple at the output, as far as possible.

Basically the ripple is a.c., i.e. varying with time, while d.c. is a constant w.r.t. time. Hence in order to separate d.c. from ripple, the filter circuit should use components which have widely different impedance for a.c. and d.c. Two such components are inductance and capacitance. Ideally, the inductance acts as a short circuit for d.c., but it has a large impedance for a.c.. Similarly, the capacitor acts as open for d.c. and almost short for a.c. if the value of capacitance is sufficiently large enough.

Since ideally, inductance acts as short circuit for d.c., it cannot be placed in shunt arm across the load, otherwise the d.c. will be shorted.

Key Point : *Hence, in a filter circuit, the inductance is always connected in series with the load.*

The inductance used in filter circuits is also called "**choke**".

Similarly, since the capacitance is open for d.c., i.e. it blocks d.c.; hence it cannot be connected in series with the load.

Key Point : *It is always connected in shunt arm, parallel to the load.*

Thus filter is an electronic circuit composed of capacitor, inductor or combination of both and connected between the rectifier and the load so as to convert pulsating d.c. to pure d.c.

There are basically two types of filter circuits,

- Capacitor input filter
- Choke input filter

Looking from the rectifier side, if the first element, in the filter circuit is capacitor then the filter circuit is called **capacitor input filter**. While if the first element is an inductor, it is called **choke input filter**. The choke input filter is not in use now a days as inductors are bulky, expensive and consume more power. Let us discuss the operation of a capacitor input filter.

1.30 Capacitor Input Filter

The block schematic of capacitor input filter is shown in the Fig. 1.68. Looking from the rectifier side the first element in filter is a capacitor.

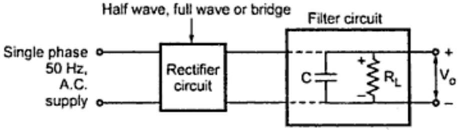


Fig. 1.68

1.30.1 Operation of the Filter with Half Wave Rectifier

The Fig. 1.69 shows a half wave rectifier with a capacitor input filter. The filter uses a single capacitor connected in parallel with the load, represented by the resistance R_L. In order to minimize the ripple in the ouput, the capacitor C used in the filter circuit is quite large, of the order of tens of microfarads. The half wave recitifier is considered to explain the principle of operation and then the concept is applied to a full wave rectifier.

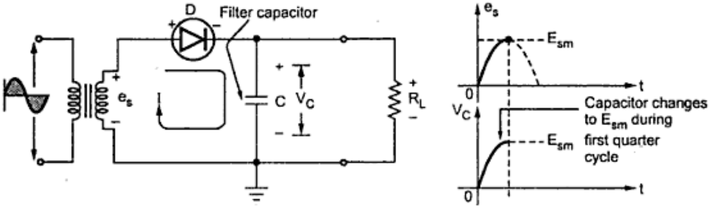

D
Filter capacitor
e_s
C
V_C
R_L
E_{sm}
t
0
Capacitor changes to E_{sm} during first quarter cycle

Fig. 1.69 Operation of capacitor input filter

During the positive quarter cycle of the input signal e_s, the diode is forward biased. This charges the capacitor C to peak value of input i.e. E_{sm}. Practically the capacitor C charges to $(E_{sm} - 0.7)$ V, due to diode forward voltage drop.

Key Point : *This initial charging happens only once, immediately when the power is turned on.*

When the input starts decreasing below its peak value, the **capacitor remains charged at E_{sm}** and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode. So during the entire negative half cycle and some part of the next positive half cycle, capacitor discharges through R_L as shown in the Fig. 1.70.

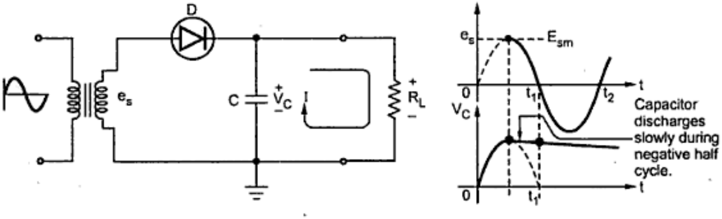

D
e_s
C
V_C
I
R_L
E_{sm}
t_1
t_2
t_1'
t
0
Capacitor discharges slowly during negative half cycle.

Fig. 1.70 Capacitor discharges through load resistance

The discharging of capacitor is decided by R_LC time constant which is very large and hence capacitor discharges very little from E_{sm}. In the next positive half cycle, when e_s becomes more than capacitor voltage, the diode becomes forward biased and charges the capacitor C back to E_{sm}. This is shown in the Fig. 1.71.

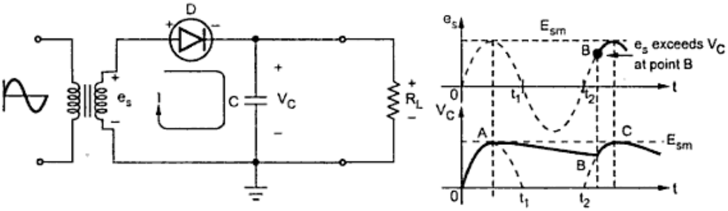


Fig. 1.71 Capacitor starts charging again

The capacitor starts charging at point B where e_s exceeds the capacitor voltage which is slightly less than E_{sm}. So from B onwards the capacitor starts charging again and gets charged to E_{sm}.

Key Point : *The discharging of the capacitor is from A to B.*

The capacitor voltage is same as the output voltage as it is in parallel with R_L. It can be seen that the diode conducts only from point B till capacitor gets charged back to E_{sm}. **Thus diode conducts only for part of the positive half cycle.** From point A to B, the diode remains non-conducting and conducts only for the period from B to C. This is shown in the Fig. 1.72.

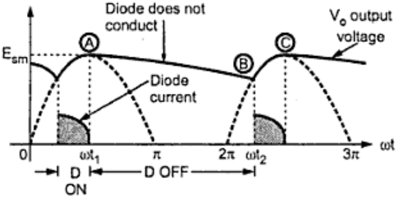


Fig. 1.72 Diode conducts only for part of positive cycle

When the diode is non-conducting the capacitor supplies the load current. As the time required by the capacitor is very small to charge while its discharging time constant is very large, the ripple in the output gets reduced considerably.

1.30.2 Operation with Full Wave Rectifier

The same concept can now be extended to the capacitor filter used in full wave rectifier circuit as shown in the Fig. 1.73.

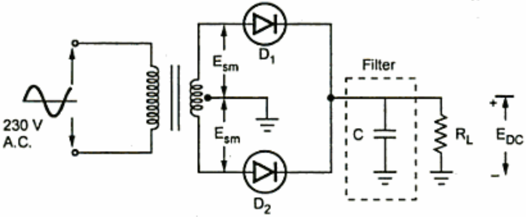

230 V
A.C.
E_{sm}
E_{sm}
D_1
D_2
Filter
C
R_L
+
E_{DC}
–

Fig. 1.73 Capacitor input filter in full wave rectifier

Immediately when power is turned on, the capacitor C gets charged through forward biased diode D_1 to E_{sm}, during first quarter cycle of the rectified output voltage. In the next quarter cycle from $\frac{\pi}{2}$ to π, the capacitor starts discharging through R_L. Once capacitor gets charged to E_{sm}, the diode D_1 becomes reverse biased and stops conducting. So during the period from $\frac{\pi}{2}$ to π, the capacitor C supplies the load current. It discharges to point B shown in the Fig. 1.74. At point B, lying in the quarter π to $\frac{3\pi}{2}$ of the rectified output voltage, the input voltage exceeds capacitor voltage, making D_2 forward biased. This charges capacitor back to E_{sm} at point C.

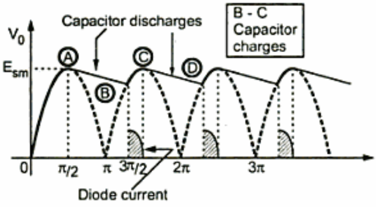
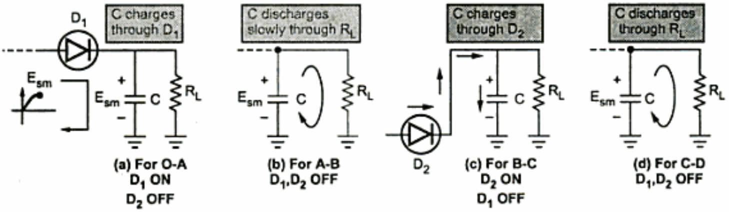


Fig. 1.74 Capacitor filter with FWR

The time required by capacitor C to charge to E_{sm} is quite small and only for this period, diode D_2 is conducting. Again at point C, diode D_2 stops conducting and capacitor supplies load and starts discharging upto point D in the next quarter cycle of the rectified output voltage as shown in the Fig. 1.30. At this point, the diode D_1 conducts to charge capacitor back to E_{sm}. The diode currents are shown shaded in the Fig. 1.74.


D_1
C charges through D_1
E_{sm}
+
E_{sm}
C
–
R_L
C discharges slowly through R_L
+
E_{sm}
C
–
R_L
C charges through D_2
+
C
–
R_L
D_2
C discharges through R_L
+
E_{sm}
C
–
R_L

(a) For O-A
D_1 ON
D_2 OFF

(b) For A-B
D_1,D_2 OFF

(c) For B-C
D_2 ON
D_1 OFF

(d) For C-D
D_1,D_2 OFF

Fig. 1.75 Operation of capacitor filter for full wave rectifier

> **Key Point:** *The diodes are not conducting for the entire half cycle but only for a part of the half cycle, during which the capacitor is getting charged.*

When the capacitor is discharging through the load resistance R_L, both the diodes are non-conducting. The capacitor supplies the load current.

> **Key Point:** *As the time required by capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably.*

Though the diodes conduct partly, the load current gets maintained due to the capacitor. This filter is very popularly used in practice.

1.30.3 Approximate Analysis of Capacitor Input Filter

Consider an output waveform for a full wave rectifier circuit using a capacitor input filter, as shown in the Fig. 1.76.

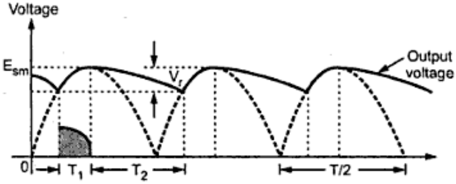


Fig. 1.76 Derivation of ripple factor

Let T = Time period of the a.c. input voltage

$\frac{T}{2}$ = Half of the time period

T_1 = Time for which diode is conducting

T_2 = Time for which diode is non-conducting

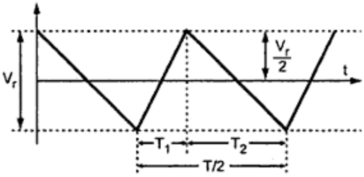


Fig. 1.76 (a) Triangular approximation of ripple voltage

During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant R_LC is very large, discharging process is very slow and hence $T_2 >> T_1$.

Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the Fig. 1.76 (a).

It is known mathematically that the r.m.s. value of such a **triangular waveform** is,

$$\boxed{V_{rms} = \frac{V_r}{2\sqrt{3}}} \qquad \text{... (1)}$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L. The charge lost is,

$$Q = CV_r \qquad \text{... (2)}$$

But $$i = \frac{dQ}{dt}$$

$\therefore$ $$Q = \int_0^{T_2} i\,dt = I_{DC}\,T_2$$

As integration gives average or d.c. value

Hence $$I_{DC}\,T_2 = CV_r \qquad \text{... (3)}$$

$\therefore$ $$V_r = \frac{I_{DC}\,T_2}{C}$$

Now, $$T_1 + T_2 = \frac{T}{2} \qquad \text{Normally, } T_2 >> T_1$$

$\therefore$ $$T_1 + T_2 \approx T_2 = \frac{T}{2} \qquad \text{where } T = \frac{1}{f}$$

$\therefore$ $$V_r = \frac{I_{DC}}{C}\left[\frac{T}{2}\right] = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2\,fC}$$

But $$I_{DC} = \frac{E_{DC}}{R_L}$$

$\therefore$ $$\boxed{V_r = \frac{E_{DC}}{2\,f\,C\,R_L} = \textbf{peak to peak ripple voltage}} \qquad \text{... (4)}$$

$$\text{Ripple factor} = \frac{V_{rms}}{E_{DC}} = \frac{\frac{E_{DC}}{2\,f\,C\,R_L}}{2\sqrt{3}} \times \frac{1}{E_{DC}}, \text{ Since } V_{rms} = \frac{V_r}{2\sqrt{3}}$$

$\therefore$ $$\boxed{\text{Ripple factor} = \frac{1}{4\sqrt{3}\,f\,C\,R_L} \quad \textbf{for full wave}} \qquad \text{... (5)}$$

For **half wave rectifier** with capacitor input filter the ripple factor is,

$$\boxed{\text{Ripple factor} = \frac{1}{2\sqrt{3}\,f\,C\,R_L} \quad \textbf{for half wave}} \qquad \text{... (6)}$$

The product CR_L is the time constant of the filter circuit.

From the expression of the ripple factor, it is clear that increasing the value of capacitor C, the ripple factor gets decreased. Thus the output can be made smoother, reducing the ripple content **by selecting large value of capacitor.** However very large value of capacitor cannot be used because larger the value of capacitor, larger the initial charging surge current. This may exceed the current rating of the diodes in the rectifier. Otherwise the diodes used must be of higher current rating which increases the cost.

1.30.4 Why Capacitor Filter is not Suitable for Variable Loads?

The another factor controlling the ripple factor is load resistance R_L. As the load current drawn increases, for the same d.c. output voltage, the load resistance decreases. This increases the ripple contents in the output. Hence the **filter is not suitable for the variable loads**. The desirable feature of the filter is **high voltage and less ripple at the output for small load currents.**

1.30.5 How to Decrease Ripple Factor ?

It can be seen from the expression of ripple factor that to decrease its value,

1. Increase the value of filter capacitor.
2. Increase the value of load resistance.

But higher C means larger initial surge current for which higher rating diodes must be used.

As R_L decreases, the load current increases but ripple increases. Hence **filter is not suitable for variable loads or higher loads**. The capacitor filter is suitable for lighter loads i.e. small load currents.

1.30.6 D.C. Output Voltage with Capacitor Filter

The d.c. output voltage from a **capacitor filter** fed from a **full wave rectifier** is given by,

$$\boxed{E_{DC} = E_{sm} - I_{DC}\left[\frac{1}{4\,fC}\right]} \quad \text{... Full wave} \quad ...(7)$$

While the d.c. output voltage from a **capacitor filter** fed from a **half wave rectifier** is given by,

$$\boxed{E_{DC} = E_{sm} - I_{DC}\left[\frac{1}{2\,fC}\right]} \quad \text{... Half wave} \quad ...(8)$$

From the above expressons, it can be seen that as the current drawn by the load increases, the d.c. output voltage decreases. Hence **this filter circuit is having poor**

regulation. The load regulation graph i.e. regulation characteristics for the capacitor input filter is shown in the Fig. 1.77.

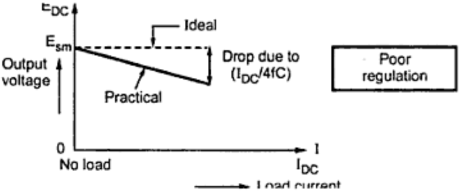


Fig. 1.77 Load regulation with capacitor input filter

1.30.7 Expression for Ripple Voltage

The **ripple voltage** present in the output can be obtained from the ripple factor.

$$\text{Ripple factor} = \frac{V_{r(rms)}}{E_{DC}}$$

Thus

$$\boxed{V_{r(rms)} = \text{R.M.S. ripple voltage} = E_{DC} \times \text{ripple factor}}$$

For full wave rectifier,

$$\frac{1}{4\sqrt{3}\, f C R_L} = \frac{V_{r(rms)}}{E_{DC}} = \frac{V_{r(rms)}}{I_{DC} R_L}$$

$$\therefore \quad V_{r(rms)} = \frac{I_{DC}}{4\sqrt{3} f C} \text{ volts} \qquad \text{(For full wave)} \qquad \ldots (9)$$

$$V_{r\,(rms)} = \frac{I_{DC}}{2\sqrt{3}\, f C} \text{ volts} \qquad \text{(For half wave)} \qquad \ldots (10)$$

Thus the ripple voltage with capacitor input filter can be obtained by multiplying ripple factor with d.c. output voltage or by using equation (9) if the d.c. load current is known.

1.30.8 Surge Current in a Capacitor Input Filter

Consider a bridge rectifier as shown in the Fig. 1.78 where switch is closed at t = 0. Due to this, the diodes D_1 and D_2 are forward biased and conducting. Initially capacitor acts as a short circuit hence momentarily it does not offer any resistance to the initial current.

The forward resistance of diodes is very small hence a large current flows through the two forward biased diodes D_1 and D_2 instantaneously. This is called **surge current.** If the instant of closing the switch is such that the secondary voltage is at its peak, the surge current is also at its maximum. Such a peak surge current can destroy the diodes.

Such a peak surge current is shown in the Fig. 1.79 for a half wave rectifier circuit.

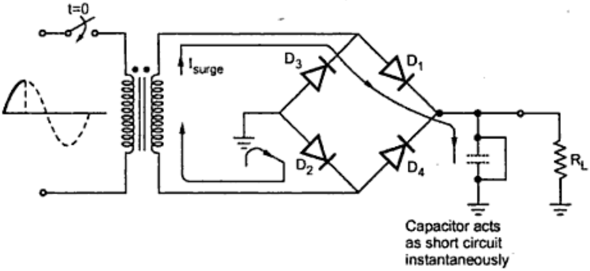
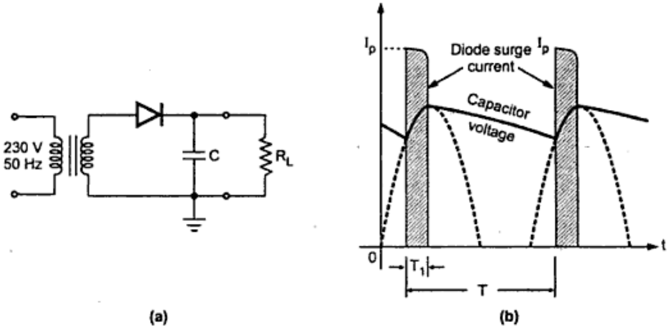

t=0
I_{surge}
D_3
D_1
D_2
D_4
R_L
Capacitor acts as short circuit instantaneously

Fig. 1.78 Surge current

The diode is forward biased only for short period of time and conducts only during this time interval to charge the filter capacitance. The instant at which the diode gets forward biased, the capacitor instantaneously acts as short circuit and a surge current flows through a diode. When the diode is non-conducting, the capacitor discharges through load resistance R_L.


230 V
50 Hz
C
R_L
I_p
Diode surge current
I_p
Capacitor voltage
0
T_1
T
t

(a) (b)

Fig. 1.79 Surge current in half wave rectifier using capacitor filter

Thus total amount of charge that flows through conducting diode or diodes to recharge the capacitor must be equal to the amount of charge lost during the period when the diode or diodes are nonconducting and capacitor is discharging through- load resistance R_L. It can be seen that conduction period T_1 is very small compared to time period T, for the diode.

Let I_{DC} = average d.c. current

$I_{p\ (surge)}$ = peak value of the surge current

Assume the current pulse to be rectangular assuming peak surge current flows for the entire conduction period of diode which is T_1.

$$\text{Then Q (discharge)} = \text{Q (charge)} \qquad \dots (11)$$

$$\therefore \quad I_{DC}T = I_{p(surge)}\,T_1$$

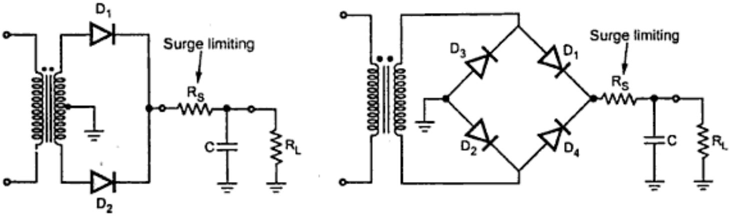
$$\therefore \quad \boxed{I_{p(surge)} = I_{DC}\left(\frac{T}{T_1}\right)} \qquad \dots (12)$$

As $T_1 << T$, it can be observed that $I_{p\ (surge)}$ can be many times larger than the average d.c. current supplied to the load. The diodes must be selected having current rating equal to the maximum value of forward surge current.

We have seen that to decrease the ripples, the value of C must be large. But large C means large time constant R_LC and hence capacitor discharges to a very small value. Hence conduction period T_1 of diodes is also small, required to recharge the capacitor. This increases peak surge current value. Hence it is necessary to limit the surge current.

1.30.8.1 Limiting the Surge Current

To limit the surge current, a surge limitinig resistor R_S is used in the circuit, as shown in the Fig. 1.80.



(a) (b)

Fig. 1.80 Limiting the surge current

The value of the surge limiting resistor must be small compared to the load resistance R_L. This is because such R_S reduces the d.c. output voltage.

Once the diodes are selected having maximum surge current rating as I_{FSM}, provided in the diode datasheet, the surge limiting resistor value can be,

$$\boxed{\begin{aligned} R_S &= \frac{E_{sm}-1.4}{I_{FSM}} \\ R_S &= \frac{E_{sm}-0.7}{I_{FSM}} \end{aligned}}$$

... For bridge rectifier

... For other circuits

where I_{FSM} = Maximum forward surge current rating of diode

1.30.9 Advantages

The advantages of capacitor input filter are,

1. Less number of components.
2. Low ripple factor hence low ripple voltage.
3. Suitable for high voltage at small load currents.

1.30.10 Disadvantages

The disadvantages of capacitor input filter are,

1. Ripple factor depends on load resistance.
2. Not suitable for variable loads as ripple content increases as R_L decreases.
3. Regulation is poor.
4. Diodes are subjected to high surge currents hence must be selected accordingly.

➠ **Example 1.16 :** *Determine the peak to peak ripple voltage and the ripple factor for a bridge rectifier using capacitor input filter. The load resistance is* 2 kΩ *while the d.c. voltage across the load is 12 V. Assume supply frequency to be 50 Hz and ideal diodes. The capacitor of* 100 μF *is used in the filter circuit.*

Solution : $R_L = 2\ k\Omega$, $E_{DC} = 12$ V, f = 50 Hz, C = 100 μF

$$V_r = \frac{E_{DC}}{2\,f\,C\,R_L} = \text{peak to peak ripple voltage}$$

... eq. (4) of section 1.30.3

$$= \frac{12}{2\times 50\times 100\times 10^{-6}\times 2\times 10^{3}} = \mathbf{0.6\ V}$$

The ripple factor is ,

$$\gamma = \frac{1}{4\sqrt{3}\,f\,C\,R_L} = \frac{1}{4\sqrt{3}\times 50\times 100\times 10^{-6}\times 2\times 10^{3}}$$

$$= \mathbf{0.0144\ i.e.\ 1.44\ \%}$$

➠ **Example 1.17 :** *A full wave rectifier is operated from 50 Hz supply with 120 V (rms). It is connected to a load drawing 50 mA and using 100 μF filter capacitor. Calculate the d.c. output voltage and the r.m.s. value of ripple voltage. Also calculate the ripple factor.*

Solution : $E_{s(rms)} = 120$ V, f = 50 Hz, $I_{DC} = 50$ mA, C = 100 μF

$$E_{sm} = \sqrt{2}\,E_{s(rms)} = \sqrt{2}\times 120 = 169.7056\text{ V}$$

For full wave rectifier,

$$E_{DC} = E_{sm} - I_{DC}\left[\frac{1}{4\,fC}\right]$$

$$= 169.7056 - \frac{50\times 10^{-3}}{4\times 50\times 100\times 10^{-6}} = \mathbf{167.2056\ V}$$

$$V_{r(rms)} = \frac{I_{DC}}{4\sqrt{3}\,fC} = \frac{50\times 10^{-3}}{4\times\sqrt{3}\times 50\times 100\times 10^{-6}} = \mathbf{1.4433\ V}$$

The ripple factor is given by,

$$\gamma = \frac{V_{r(rms)}}{E_{DC}} = \frac{1.4433}{167.2056} = 8.63\times 10^{-3}$$

➠ **Example 1.18 :** *A full wave rectifier uses a centre-tap transformer whose turns ratio to half secondary is 10 : 1 and is supplied with 230 V at 50 Hz. The load resistance is 50 Ω. Calculate the load voltage and the ripple voltage. If now a capacitor of 470 μF is used as a filter, recalculate the load voltage and the ripple voltage, assuming same load current.*

Solution : $E_{p(rms)} = 230$ V, f = 50 Hz, $N_1 : N_2 = 10 : 1$, $R_L = 50\ \Omega$

Case 1 : $$\frac{E_{p(rms)}}{E_{s(rms)}} = \frac{N_1}{N_2} = \frac{10}{1}$$

$$\therefore \quad E_{s(rms)} = \frac{E_{p(rms)}}{10} = \frac{230}{10} = 23\text{ V}$$

$$\therefore \quad E_{sm} = \sqrt{2}\,E_{s(rms)} = 32.5269\text{ V}$$

$$\therefore \quad I_m = \frac{E_{sm}}{R_L} = \frac{32.5269}{50} = 0.6505\text{ A}$$

$$\therefore \quad I_{DC} = \frac{2I_m}{\pi} = \frac{2\times 0.6505}{\pi} = 0.4141\text{ A}$$

$$\therefore \quad E_{DC} = I_{DC}R_L = 0.4141\times 50 = \mathbf{20.7072\ V}$$

$$\text{Ripple factor} = \mathbf{0.48} \text{ for full wave without filter}$$

$$\therefore \quad \text{Ripple voltage (rms)} = \text{ripple factor} \times E_{DC}$$

$$= 0.48\times 20.7072 = \mathbf{9.9394\ V}$$

Case 2 : Now **capacitor filter** is used.

$$\therefore \quad E_{DC} = E_{sm} - \frac{I_{DC}}{4fC} = 32.5269 - \frac{0.4141}{4\times 50\times 470\times 10^{-6}}$$

$$= \mathbf{28.1215\ V}$$

The ripple voltage can be calculated as,

$$\gamma = \frac{1}{4\sqrt{3}\,fCR_L} = \mathbf{3.256\times 10^{-3}}$$

$$\therefore \quad V_{r(rms)} = \gamma\times E_{DC} = 3.256\times 10^{-3}\times 28.1215 = \mathbf{0.09156\ V}$$

1.31 Circuit Models of a Diode

The diode is required to be replaced by the equivalent circuit in many practical electronic circuits, for the analysis purpose. Such an equivalent circuit of a diode is called **circuit model** of a diode. There are three methods of replacing diode by its circuit model, which are,

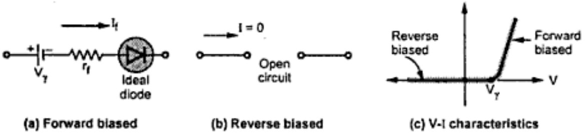
1. Practical diode model
2. Ideal diode model
3. Piecewise linear model

Let us discuss these three circuit models.

1.31.1 Practical Diode Model

It is seen that in forward biased diode, the total voltage drop across the diode is V_f which consists of drop due to barrier potential which is almost equal to cut-in voltage V_γ and the drop across the internal forward dynamic resistance r_f of the diode. While when reverse biased, reverse saturation current is very small and practically neglected. Hence reverse biased diode is practically assumed to be **open circuit.**

Thus the practical diode model consists of a battery equal to cut-in voltage and the forward resistance, in series with an ideal diode, in forward biased condition. The Fig. 1.81 (a) shows this model. In reverse biased, it is open circuited. The Fig. 1.81 (b) shows this model. While the Fig. 1.81 (c) shows the correspondig V-I characteristics.



(a) Forward biased (b) Reverse biased (c) V-I characteristics

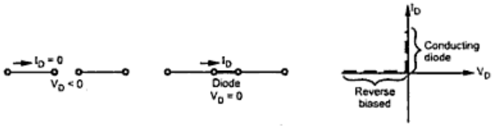
Fig. 1.81 Practical diode model

Key Point: *An external circuit to the diode must be designed properly so as to control the forward current through the diode.*

1.31.2 Ideal Diode Model

In many cases, as the forward resistance of diode is small and cut-in voltage is also small, the diode is assumed to be an **ideal diode**.

In case of ideal diode, it is assumed that it starts conducting instantaneously when applied voltage V_D is just greater than zero and the drop across the conducting diode is zero. So conducting diode can be ideally replaced by a **short circuit**, for the analysis of various diode circuits. The Fig. 1.82 shows the ideal diode characteristics.



(a) Reverse biased (b) Forward biased (c) V - I characteristics

Fig. 1.82 Ideal diode model

1.31.3 Piecewise Linear Model of Diode

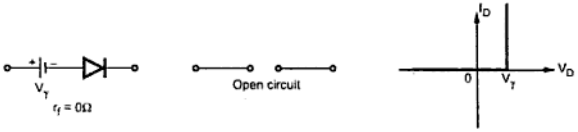
Another way to analyse the diode circuits is to approximate the V-I characteristics of a diode using only straight lines i.e. linear relationships.

In such approximation, the diode forward resistance is neglected and the diode is assumed to conduct instantaneously when applied forward biased voltage V_D is equal to cut-in voltage V_γ. And then it is assumed that current increases instantaneously giving straight line nature of V-I characteristics. While in reverse biased condition when $V_D < 0$, the diode does not conduct at all.

Hence when diode forward resistance is assumed zero, the circuit model of diode is as shown in the Fig. 1.83 (a). In reverse biased, the diode is open circuit as shown in the

Fig. 1.83 (b). As the diode conducts at $V_D = V_\gamma$, the V-I characteristics with straight lines is as shown in the Fig. 1.83 (c).

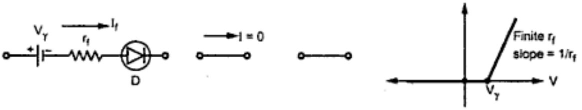
As the method models the diode with the pieces of straight lines, the name given to such approximation is **piecewise-linear method**. The characteristics of diode shown in the Fig. 1.83 (c) are called the piecewise linear diode characteristics.



(a) Forward biased (b) Reverse biased (c) V - I characteristics

Fig. 1.83 Linear piecewise model of diode with $r_f = 0\ \Omega$

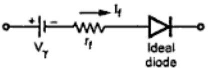
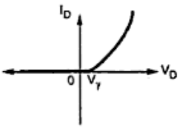
Finite r_f : In the above discussion, r_f is neglected as very small. But if r_f is considered to be finite, then in V-I characteristics, forward biased characteristics is a straight line with a slope equal to reciprocal of r_f. In reverse biased the diode is still assumed to be open circuited. The linear piecewise model with finite r_f is shown in the Fig. 1.84.



(a) Forward biased (b) Reverse biased (c) V-I characteristics

Fig. 1.84 Linear piecewise model of diode with finite r_f

The diode equivalent models are summarized in the Table 1.5.

Type	Model in forward biased	V-I characteristics	Drop across diode
Practical diode			$V_f = V_\gamma + I_f r_f$

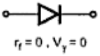
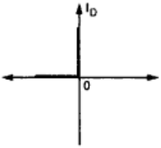
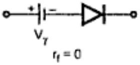
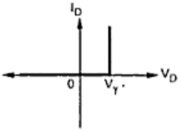
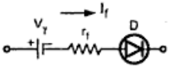
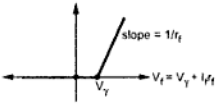
Ideal diode			$V_f = 0$
Piecewise linear with $r_f = 0\,\Omega$			$V_f = V_\gamma$
Piecewise linear with finite r_f			$V_f = V_\gamma + I_f r_f$

Table 1.5 Diode equivalent circuits

In all the above models, the diode is assumed to be open circuit, when reverse biased. The value of $V_\gamma = 0.2$ V for germanium and 0.7 V for silicon diodes.

1.31.4 Analysis of Diode Circuits

Using the appropriate diode model, the circuit consisting of many diodes, resistances and sources can be analysed. The analysis starts by assuming certain diodes ON and other diodes OFF. This assumption is based on circuit inspection and polarities of sources connected in the circuit. Then ON diodes must be replaced by a battery of voltage V_γ and a series resistance r_f. If r_f is not known, it can be assumed zero. The OFF diodes must be replaced by open circuits. Then the circuit becomes linear and can be analysed using Kirchhoff's laws. The assumption of ON diodes can be verified from the directions of currents obtained by Kirchhoff's laws analysis. If the direction of current obtained for a particular diode is reverse i.e. from n to p for a diode, the assumption that diode is ON is incorrect. In such a case, ON diode must be replaced by OFF and entire analysis of the circuit must be done once again. The OFF state assumption of diodes can be verified by calculating voltages across open circuits, used to replace OFF diodes. If we get polarity of any such voltage in forward direction, with magnitude greater than V_γ, the assumption of OFF diode is incorrect. In such a case, that diode must be replaced by ON state model, and once again entire analysis must be done. If the voltages are in reverse direction or in forward direction with magnitudes less than V_γ, the assumptions of OFF diodes get justified. This method is used to analyse various complex diode circuits.

Key Point: *Thus by using model of a diode, the mathematical analysis of the circuit can be done, which helps us to predict the circuit performance before actually building and testing the diode circuit in the laboratory.*

1.32 Clipper Circuits or Limiters

The basic action of clipper circuits is to remove the certain portions of the waveform, above or below the certain levels, as per the requirements.

Key Point: *Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called* ***clipper circuits*** *or* ***clippers.***

The half wave rectifier is the best and simplest type of clipper circuit which clips off the negative portion of the input signal. By changing the orientation of the diode in the circuit, positive or negative portion of the input signal can be clipped off.

The **clipper** circuits are also called **limiters** or **slicers**. The clipper circuits are mainly classified depending upon the orientation of the diode in the circuit.

Key Point: *When the diode is connected in series with the load, such circuit is called* ***Series Clipper.*** *When the diode is connected in a branch which is parallel to the load, it is called* ***Parallel Clipper.***

Let us discuss, these two types of clipper circuits.

1.32.1 Steps to Analyse Clipper Circuits

The various clipper circuits can be analysed using the following steps,

1. Replace the diodes by one of its equivalent models.
2. Identify ON and OFF states of the diodes and the clipping levels of V_{in}.
3. Derive the equation for transfer characteristics of the circuit.
4. Plot the transfer characteristics and input-output waveforms of the circuit.

1.33 Series Clippers

A series clipper can be used to clip off the entire positive or negative half cycles of input waveforms. It also can be used to clip off the portion above the certain reference voltage or below the certain reference voltage. A diode is most important element of any clipper circuit. It acts as a switch. It makes the circuit open, when reverse biased while it makes the circuit closed when forward biased. Let us study the working of some series clipper circuits.

1.33.1 Series Negative Clipper Circuit

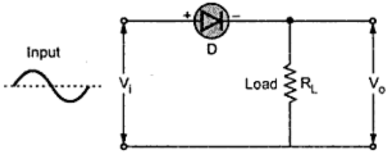


Fig. 1.85 Negative series clipper

Key Point: *A series negative clipper is basically a half wave rectifier circuit.*

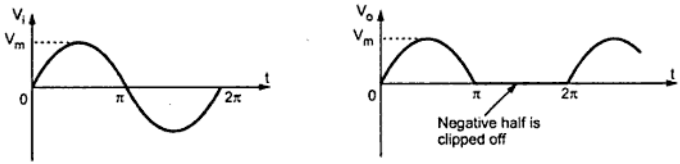
Operation :

Consider a circuit shown in the Fig. 1.85 where diode is connected in series with the load. Let us analyze this circuit. For a positive half cycle, the diode D is forward biased. Hence the voltage waveform across R_L looks like a positive half cycle of the input voltage.

While for a negative half cycle, diode D is reverse biased and hence will not conduct at all. Hence there will not be any voltage available across resistance R_L. Hence the negative half cycle of input voltage gets clipped off. The input waveform and the corresponding output voltage waveform is shown in the Fig. 1.86.

Key Point: *For an ideal diode, the output voltage will reach to the same maximum level as that of input, during positive half cycle.*

As it clips off negative half cycle of the input it is called **series negative clipper.**



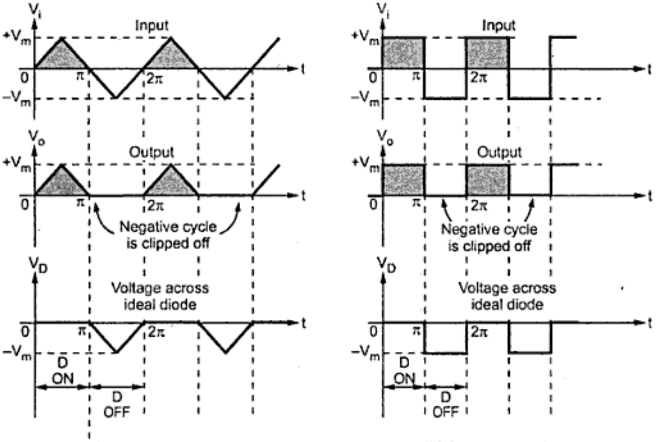
(a) Input voltage (b) Output voltage

Fig. 1.86

Key Point: *It is not necessary that in such circuits the input voltage waveform has to be a sinusoidal one.*

Operation with non-sinusoidal inputs :

The input to the circuit can be of any type as square, triangular etc. The circuit clipps off the negative portion of the input waveform. This is shown in Fig. 1.87(a) and (b).



(a) Triangular input voltage (b) Square wave input

Fig. 1.87 Waveforms of series negative clipper

When diode is reverse biased, the negative peak of input appears across the diode. The diode must be selected so as to withstand this reverse voltage. Its peak inverse voltage (PIV) rating must be higher than the reverse voltage appearing across it.

Transfer characteristics :

The working of the circuit can be easily understood if a graph of output against input is available.

Key Point: *The graph of output variable against input variable of the circuit is called transfer characteristics of the circuit.*

Thus for the negative series clipper, the graph of V_o against V_i is its transfer characteristics. The mathematical equation for such a graph, **assuming ideal diode** is given by,

$$\boxed{\begin{array}{ll} V_o = V_i & \text{... for } V_i \geq 0 \\ V_o = 0, & \text{... for } V_i < 0 \end{array}}$$

The graph showing above mathematical relationship is shown in the Fig. 1.88.

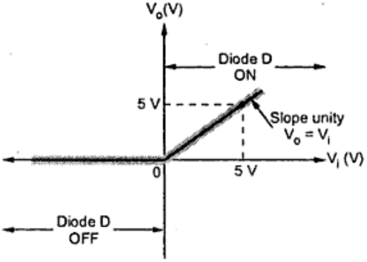


Fig. 1.88 Transfer characteristics with ideal diode

Effect of cut-in voltage of diode :

It is known that diode does not conduct till the forward voltage becomes greater than cut-in voltage V_γ of the diode. Hence in series negative clipper, the diode D conducts when $V_i > V_\gamma$, where V_γ is generally 0.7 V for silicon diodes. While for $V_i \le V_\gamma$, the diode D is OFF and $V_o = 0$ V.

Thus due to cut-in voltage of diode,

1. Only negative half cycle does not get clipped off but part of positive half cycle till V_i becomes more than V_γ of diode also gets clipped off.
2. The maximum output voltage V_o available is less than maximum input voltage V_m by the amount equal to V_γ.

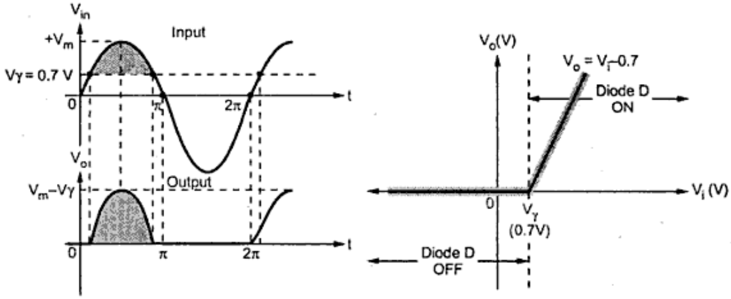
The mathematical equation for transfer characteristics now becomes,

$$\boxed{\begin{array}{ll} V_o = V_i - 0.7 & \text{... for } V_i > 0.7 \text{ V} \\ V_o = 0, & \text{... for } V_i \le 0.7 \text{ V} \end{array}}$$

The effect of cut-in voltage i.e. barrier potential is shown in the Fig. 1.89(a) and 1.89(b).

(See Fig. 1.89 (a) and (b) on next page.)

Key Point: *The region for which diode is ON is called* ***transmitting region*** *while the region for which diode is OFF is called* ***clipping or limiting region.***



(a) Input-output wave forms

(b) Transfer characteristics with non-ideal diode

Fig. 1.89 Effect of V_γ on negative clipper circuit

1.33.2 Series Positive Clipper Circuit

Similar to series negative clipper, a circuit which clipps off positive part of the input can be obtained. It is called series positive clipper.

> **Key Point**: *The positive series clipper can be obtained by changing the direction of diode in negative clipper circuit.*

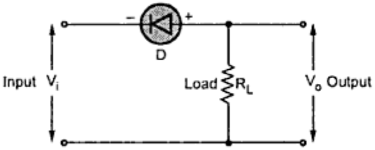


Fig. 1.90 Positive series clipper

The Fig. 1.90 shows positive series clipper circuit in which diode direction is opposite to that in negative series clipper circuit.

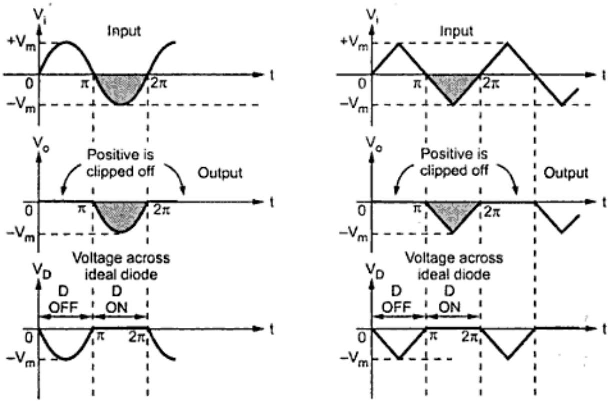
Operation :

For positive half cycle of input, $V_i > 0\,V$ and diode is reverse biased. Hence it acts as open circuit and $V_o = 0\,V$.

For negative half cycle, when $V_i < 0$, the diode conducts. Assuming ideal diode, the output voltage V_o available is same as input voltage. Thus entire negative half cycle of input is available at the output

> **Key Point**: *Thus positive series clipper clips off the positive part of the input waveform.*

The output waveforms for sinusoidal and triangular input waveforms are shown in the Fig. 1.91.



(a) Sinusoidal input (b) Triangular input

Fig. 1.91 Waveforms of series postive clipper

Transfer characteristics :

With **ideal diode**, the equation for transfer characteristics is,

$$V_o = 0 \quad \text{... for } V_i > 0 \text{ V}$$
$$V_o = V_i, \quad \text{... for } V_i \leq 0 \text{ V}$$

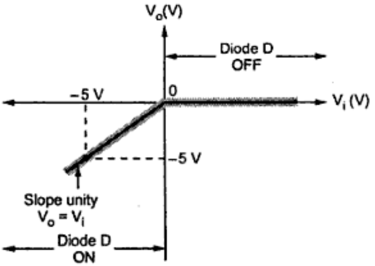


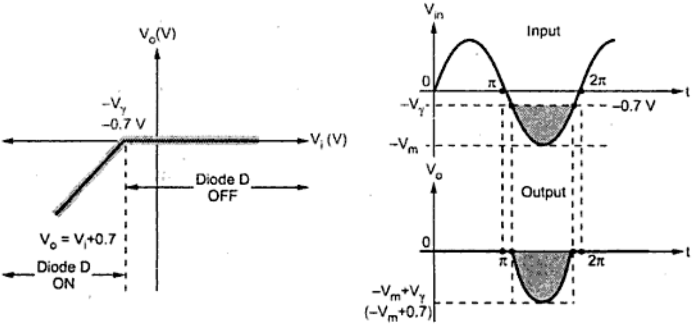
Fig. 1.92 Transfer characteristics with ideal diode

The transfer characteristics are shown in the Fig. 1.92. If the diode is not ideal then as long as V_i is less than $-V_\gamma$ i.e. − 0.7 V, the diode can not conduct.

Hence mathematical equation for transfer characteristics with practical diode having cut-in voltage V_γ is

$$V_o = 0 \quad \text{... for } V_i \geq -0.7 \text{ V}$$
$$V_o = V_i + 0.7 \quad \text{... for } V_i \leq -0.7 \text{ V}$$

The transfer characteristics are shown in the Fig. 1.93(a) while the waveforms with non-ideal diode are shown in the Fig. 1.93(b).


V_o(V)
$-V_\gamma$
-0.7 V
V_i (V)
Diode D OFF
$V_o = V_i + 0.7$
Diode D ON
V_{in}
Input
0
π
2π
t
$-V_\gamma$
-0.7 V
$-V_m$
V_o
Output
0
π
2π
t
$-V_m + V_\gamma$
$(-V_m + 0.7)$

(a) Transfer characteristics **(b) wave forms**

Fig. 1.93 Effect of V_γ on positive clipper circuit

Key Point: *Thus due to V_γ, the part of negative half cycle also gets clipped off alongwith a positive half cycle of the input, in a positive series clipper circuit.*

1.33.3 Clipping Above Reference Voltage V_R

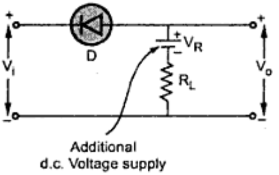

+
+
D
V_R
V_i
V_o
R_L
−
−
Additional
d.c. Voltage supply

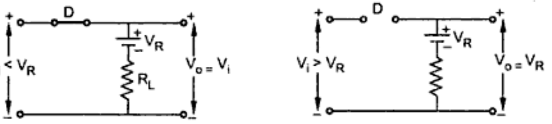
Fig. 1.94 Clipping above V_R

The output of the clipper can be adjusted as per the requirement by adding an additional voltage source in series with the load resistance as shown in the Fig. 1.94.

The diode D is an ideal diode and hence there is no drop across it when it is forward biased. Thus when forward biased, it acts as a short circuit while when reverse biased it acts as open circuit.

Operation :

When V_i is less than V_R , the diode becomes forward biased and the circuit can be reduced to as shown in the Fig. 1.95 (a). In this case the output voltage V_o is equal to input voltage V_i. When V_i is greater than V_R, the diode is reverse biased and circuit gets reduced to, as shown in the Fig. 1.95 (b). No current can flow in the circuit as circuit is open and hence output voltage V_o is equal to V_R.


D
+
V_i < V_R
V_R
R_L
V_o = V_i
-
D
V_i > V_R
V_R
V_o = V_R

(a) $V_i < V_R$ (b) $V_i > V_R$

Fig. 1.95

The input and output waveforms for such a clipper are shown in the Fig. 1.96.

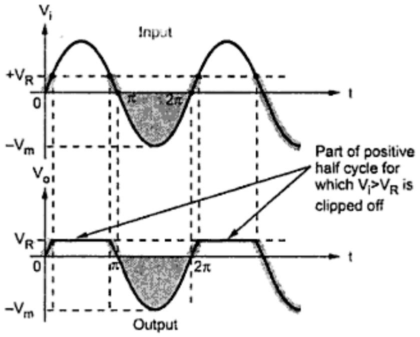

V_i
Input
+V_R
0
π
2π
t
-V_m
V_o
V_R
0
π
2π
t
-V_m
Output
Part of positive half cycle for which V_i>V_R is clipped off

Fig. 1.96 Waveforms for clipping above V_R

Key Point: *It can be seen that the portion of the input waveform above V_R gets clipped off. The level of V_R can be adjusted as per the requirement by selecting proper battery voltage.*

Mathematically this can be expressed as,

$$\boxed{\begin{array}{ll} V_o = V_i, & \text{... for } V_i < V_R \\ V_o = V_R, & \text{... for } V_i > V_R \end{array}}$$

This mathematical representation helps us to sketch the transfer characteristics of the clipper circuit. The transfer characteristics is the graph of output voltage V_o against input voltage V_i. The above equations are called the **transfer characteristic equations.** The transfer characteristics is shown in the Fig. 1.97.

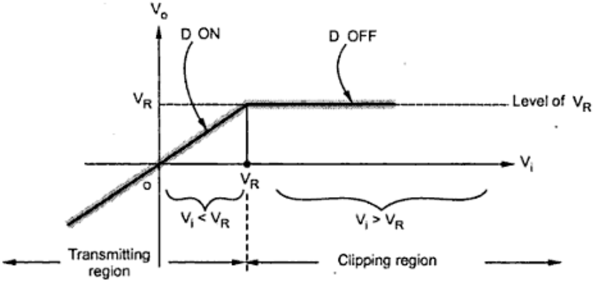


Fig. 1.97 Transfer characteristics

For the portion till $V_i < V_R$, the graph is straight line. This region is called the **transmission region** as it transmits V_i at the output as it is. While the portion for $V_i > V_R$, the output is constant. This region is called **clipping region.**

1.33.4 Clipping Below Reference Voltage V_R

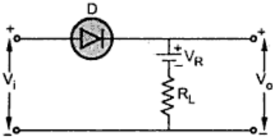


Fig. 1.98 Clipping below V_R

By changing the orientation of the diode in the circuit discussed above, we get the clipping circuit which clips the portion of waveform, below the reference voltage V_R.

The circuit is shown in the Fig. 1.98.

The diode D is an ideal diode which acts like a switch.

Operation

When V_i is less than V_R, the diode is reversed biased and circuit becomes open. The output voltage is equal to V_R as no current flows in the circuit. The circuit is shown in the Fig. 1.99 (a). When V_i is greater than V_R, the diode D becomes forward biased and circuit becomes as shown in the Fig. 1.99 (b). The output voltage V_o is equal to the input voltage V_i.

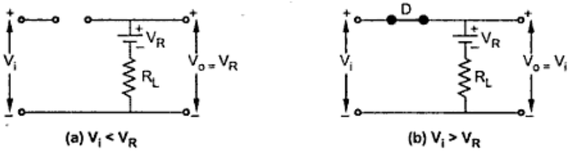


Fig. 1.99

The transfer characteristic equations are,

$$\boxed{\begin{array}{ll} V_o = V_R, & \ldots \text{for } V_i < V_R \\ V_o = V_i, & \ldots \text{for } V_i > V_R \end{array}}$$

The transfer characteristics is shown in the Fig. 1.100.

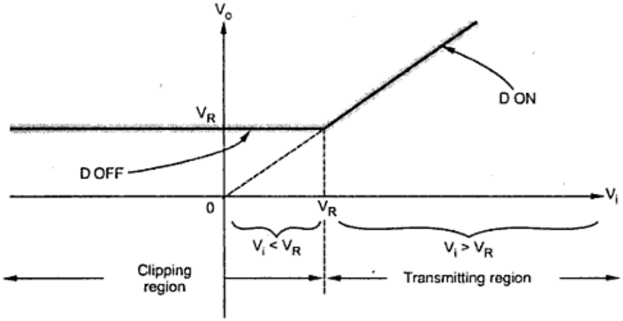
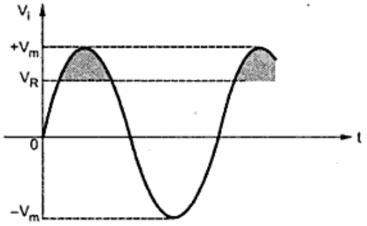


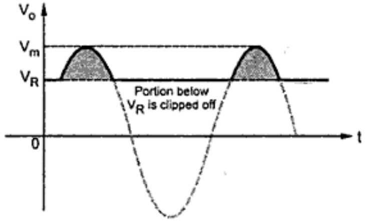
Fig. 1.100 Transfer characteristics

The region for $V_i < V_R$ is the clipping region while the region for $V_i > V_R$ is the transmitting region.

The Fig. 1.101 (a) shows the sinusoidal input voltage V_i and the Fig. 1.101 (b) shows the corresponding output waveform.



(a) Input



(b) Output

Fig. 1.101 Clipping below V_R

Key Point: *It can be seen that the portion of the output waveform below* V_R *is clipped off.*

1.33.5 Additional D.C. Supply in Series with Diode

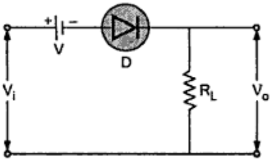


Fig.1.102 Additional d.c. supply in series with diode

The output of the clipper can be adjusted as per the requirement by adding an additional voltage source in series with the diode as shown in the Fig 1.102.

Operation :

In such a case, as long as the voltage V_i is not greater than additional battery voltage V, the diode will not start conduction, during positive half cycle. And applying KVL to the circuit we can write,

$$V_o = V_i - V$$

Hence when input voltage V_i is at its maximum V_m, the output will achieve its peak and will be equal to $V_m - V$. During negative half cycle, diode will be reverse biased and will not conduct at all. Hence negative portion of the input will be clipped off. The output voltage $V_o = 0$ V Hence the output voltage waveform will be as shown in the Fig. 1.103.

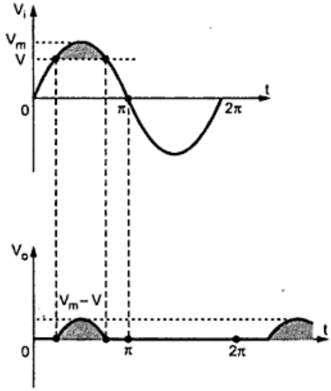


Fig. 1.103 Additional d.c. supply

Transfer characteristics :

Mathematically relation between input and output can be expressed as,

$$\boxed{\begin{aligned} V_o &= V_i - V, && \text{... for } V_i > V \\ V_o &= 0, && \text{... for } V_i \le V \end{aligned}}$$

The transfer characteristics are shown in the Fig. 1.104.

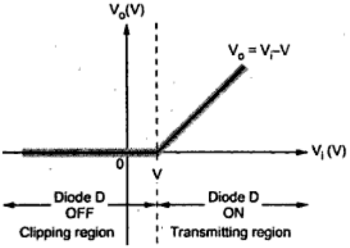


Fig. 1.104 Transfer characteristics for d.c. supply in series with diode

Key Point: *By adjusting the value of V as well as polarities of V, any part of the input as per the requirement can be clipped off.*

➡ **Example 1.19 :** *Show the output waveform for the network shown in the Fig. 1.105, if the peak value of a.c. input is 15 V. Show all the voltage levels in the output.*

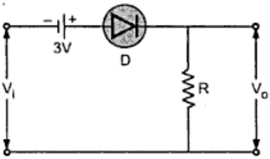


Fig. 1.105

Solution : As V = +3 V when V_i = 0, the diode is forward biased and V_o = +3 V, assuming ideal diode.

Applying KVL to the circuit we get,

$$V_i - (-V) = V_o$$

$$\therefore \quad V_i + V = V_o$$

Thus $$V_o = V_i + V, \quad \text{... for D ON}$$

$$V_o = 0, \quad \text{... for D OFF}$$

Now at t = 0, V_i = 0 but V = + 3 hence V_o = + 3. This is because at V = +3 V, diode is forward biased. When V_m = +15 V will be reached by V_i the output will reach to + 15 + 3 = + 18 V level and will start decreasing.

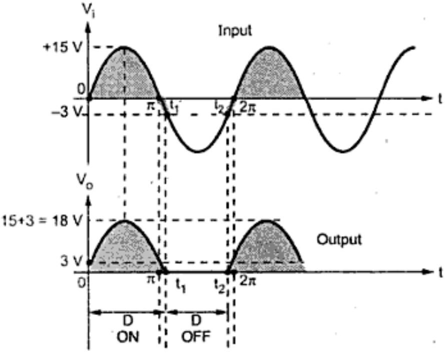


Fig. 1.106 Input and output waveforms

At $\omega t = \pi$, V_i will be zero, but output will be still +3 V. The output continues its decreasing nature in the negative half cycle of the input V_i till V_i reaches upto – 3 V at the instant t_1. At this instant, diode becomes reverse biased and output becomes zero.

When input starts increasing, at the instant t_2 when V_i crosses the limit of – 3 V, diode becomes forward biased and output starts increasing. At $\omega t = 2\pi$, it is again + 3 V and so on. The nature of the input and output voltage waveforms is shown in the Fig.1.106.

> **Key Point:** *The part of the input waveform between the instants t_1 and t_2 is clipped off. By selecting proper value of V, the instants t_1 and t_2 can be adjusted as per the requirement to obtain any desired waveform.*

The transfer characteristics are shown in the Fig. 1.107 according to the equation of V_o obtained.

Thus $V_o = V_i + V$, ... for $V_i > -3$

$V_o = 0$, ... for $V_i \leq -3$

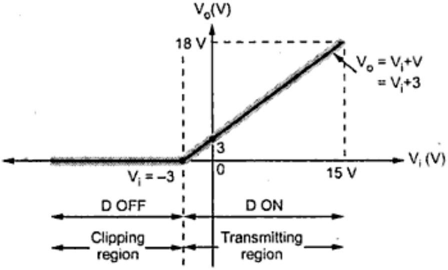


Fig. 1.107 Transfer characteristics

This example illustrates the use of additional supply voltage source to control transition state of diode, to get the required waveform of the clamped output.

1.34 Parallel Clippers

In a parallel clipper circuit, the diode is connected across the load terminals. It can be used to clip or limit the positive or negative part of the input signal, as per the requirement.

1.34.1 Basic Parallel Clipper with Positive Clipping

The Fig. 1.108 shows the basic parallel clipper circuit in which diode D is connected across the load resistance R_L. The resistance R_1 is current controlling resistance.

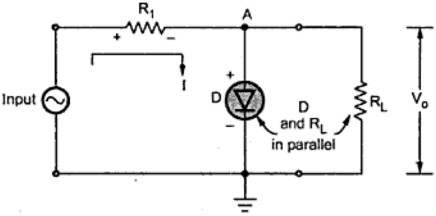


Fig. 1.108 Basic parallel clipper

Operation :

Assume ideal diode. During **positive half cycle** of the input V_i, the diode D becomes **forward biased** and remains forward biased for the entire half cycle of the input.

> **Key Point**: *As ideal diode acts as short circuit when forward biased, the current I flows entirely through diode D. The drop across short circuit diode is zero.*

As R_L is in parallel with diode no current flows through it and output voltage $V_o = 0$ V as shown in the Fig. 1.109.

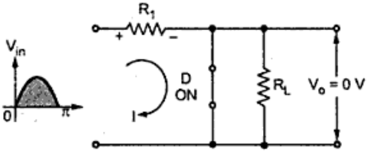


Fig. 1.109 Operation during positive half cycle

> **Key Point**: *This condition remains for entire positive half cycle of the input. Thus positive half cycle gets clipped off.*

During **negative half cycle** of input, the diode is **reverse biased** and acts as open circuit. The entire current flows through R_L as shown in the Fig. 1.110.

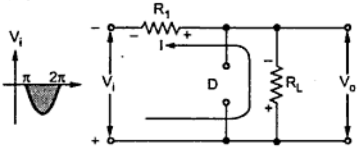


Fig. 1.110 Operation during negative half cycle

Hence $V_o = \frac{V_i R_L}{R_L + R_1}$ using potential divider rule. Thus $V_o \propto V_i$ and there exists straight line relationship between the input and output voltage.

Key Point: *As* $V_o \propto V_i$ *during negative half cycle of the input, proportionate negative half cycle is available at the output.*

The waveforms are shown in the Fig. 1.111.

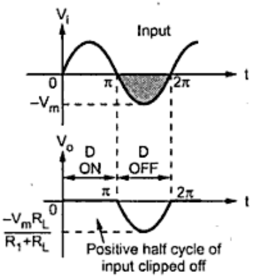


Fig. 1.111 Waveforms for parallel clipper

Transfer characteristics :

The mathematical equations for the transfer characteristics are,

$$V_o = 0, \quad \ldots \text{ for } V_i \geq 0$$

$$V_o = \frac{V_i R_L}{R_1 + R_L}, \quad \ldots \text{ for } V_i < 0$$

The transfer characteristics are shown in the Fig. 1.112.

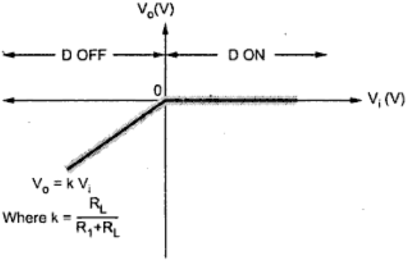


Fig. 1.112 Transfer characteristics of positive parallel clipper

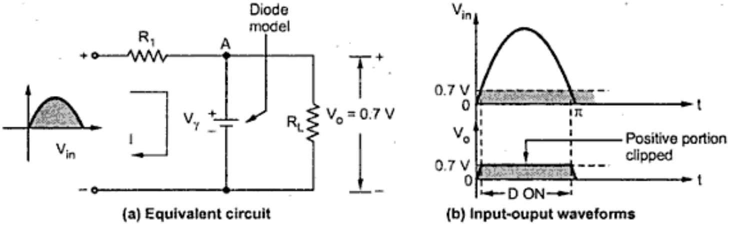
Key Point: *Making* $R_1 << R_L$, $V_o = V_{in}$ *can be obtained.*

1.34.2 Effect of Cut-in Voltage of Diode

Let us use linear piecewise model of diode, in which diode conducts when potential of node A becomes just equal to cut-in voltage of the diode. And once diode starts conducting, it acts as a voltage source of value 0.7 V for silicon, neglecting internal resistance r_f of diode. Hence V_A = 0.7 V for the conducting diode.

Key Point: *As* $V_o = V_A$, *the output voltage is 0.7 V till* $V_{in} > 0.7$ *V.*

This is shown in the Fig. 1.113.



(a) Equivalent circuit (b) Input-ouput waveforms

Fig. 1.113 Basic parallel clipper (Positive half cycle)

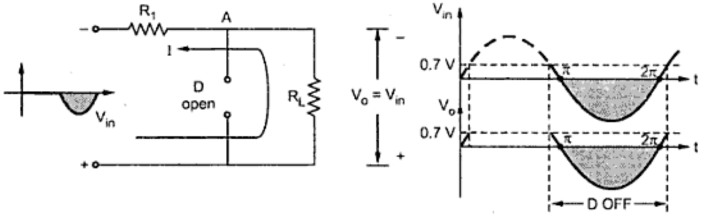
Thus almost entire positive half cycle gets clipped off.

In the negative half cycle of the input voltage V_{in}, when V_{in} is less than 0.7 V, the diode becomes reverse biased and acts as an open circuit. Hence current I flows through R_1 and R_L. The output voltage is negative part of the input voltage whose magnitude is given by,

$$V_o = \frac{V_{in} R_L}{R_1 + R_L} = V_{in} \qquad \ldots R_1 << R_L$$

Key Point: *Thus output follows the input and negative cycle of V_{in} gets reproduced at the output.*

This is shown in the Fig. 1.114.

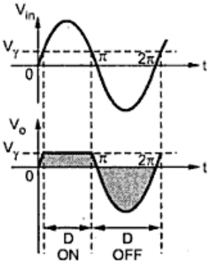


R1
A
I
D
open
RL
Vin
Vo = Vin
Vin
0.7 V
π
2π
t
Vo
0.7 V
D OFF

(a) Equivalent circuit (b) Input-output waveforms

Fig. 1.114 Basic parallel clipper (Negative half cycle)

The overall input-output waveforms can be shown as in the Fig. 1.115 using linear piecewise diode model.



Vin
Vγ
0
π
2π
t
Vo
Vγ
0
π
2π
t
D
ON
D
OFF

Fig. 1.115 Piecewise model

Transfer characteristics :

It is known that the **transfer characteristics** is the graph of output voltage against input voltage with time t as an implicit variable.

For the basic parallel clipper circuit we can write,

$$\boxed{\begin{array}{lll} & V_o = V_\gamma & V_{in} \geq V_\gamma \\ \text{and} & V_o = V_{in} & V_{in} < V_\gamma \end{array}}$$

... (1)

... (2)

Using the equations the transfer characteristics can be obtained as shown in the Fig. 1.116.

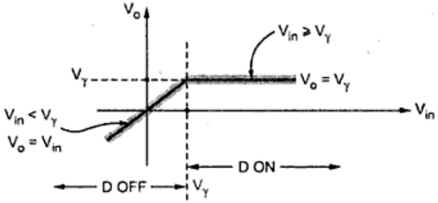


Fig. 1.116 Transfer characteristics

Key Point: *The portion for which* $V_{in} < V_\gamma$ *is called the* ***transmitting region*** *while the portion for which* $V_{in} > V_\gamma$ *is called* ***limiting region or clipping region.***

1.34.3 Basic Parallel Clipper with Negative Limiting

Key Point: *The negative clipping with basic parallel clipper can be achieved by reversing the direction of diode.*

When V_{in} is positive then the diode is reversed biased and acts as an open circuit. Thus the output voltage V_o is same as V_{in}, for $R_1 << R_L$. Hence the positive half cycle of V_{in} gets reproduced at the output. This is shown in the Fig. 1.117.

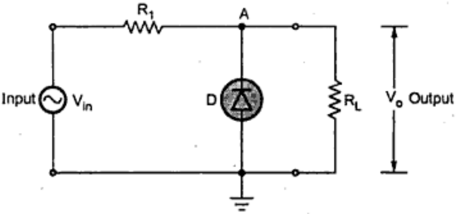
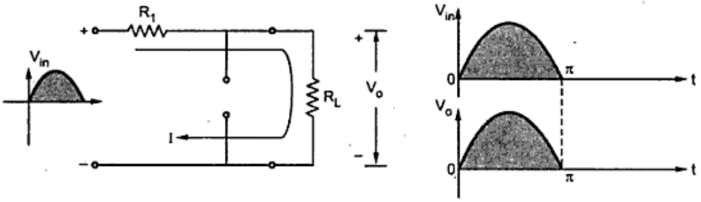


Fig. 1.117 Basic parallel clipper



(a) Equivalent circuit (b) Input-output waveforms

Fig. 1.118 Basic parallel clipper (Negative clipping)

The magnitude of the output voltage is,

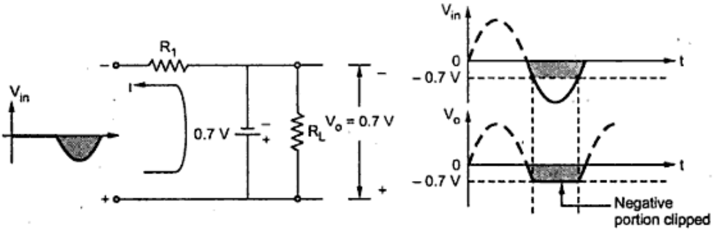
$$V_o = V_{in}\left[\frac{R_L}{R_1 + R_L}\right] = V_{in} \qquad \ldots R_1 << R_L$$

Consider the negative half cycle of V_{in}. As V_{in} decreases below zero and becomes -0.7 V, the diode becomes forward biased and starts conducting. As long as $V_{in} < -0.7$ V, the diode remains ON and drop across it is cut-in voltage $V_{\gamma} = 0.7$ V, with polarities as shown in the Fig. 1.119 (a).

Key Point: *As diode and R_L are in parallel, the output voltage V_o is equal to the drop across diode i.e. 0.7 V in opposite direction.*

$$\therefore \qquad V_o = -0.7 \text{ V} \qquad \ldots \text{for } V_{in} < -0.7 \text{ V}$$

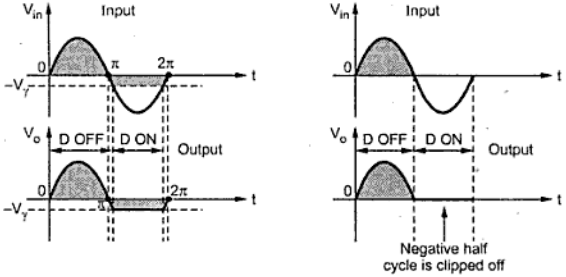
Thus the entire negative half cycle gets clipped off, as shown in the Fig. 1.119 (b).



(a) Equivalent circuit (b) Input-output waveforms

Fig. 1.119 Basic parallel clipper (Negative clipping)

The overall input-output waveforms can be shown as in the Fig. 1.120. The Fig. 1.120 (a) shows the waveforms with piecewise model of diode while the Fig. 1.120 (b) shows the waveforms with an ideal diode approximation with $V_\gamma = 0$ V.


V_{in}
Input
0
π
2π
t
$-V_\gamma$
V_o
D OFF
D ON
Output
0
2π
π
t
$-V_\gamma$
V_{in}
Input
0
t
V_o
D OFF
D ON
Output
0
t
Negative half cycle is clipped off

(a) Piecewise model (b) Ideal diode

Fig. 1.120

Transfer characteristics :

The transfer characteristic equations are,

$$\boxed{\begin{array}{ll} V_o = V_{in}, & V_{in} \geq -V_\gamma \\ V_o = -V_\gamma, & V_{in} < -V_\gamma \end{array}}$$

... (3)

and ... (4)

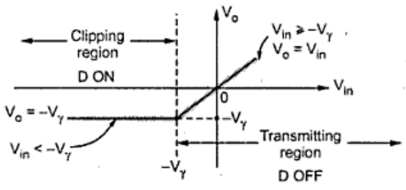


Fig. 1.121 Transfer characteristics

The transfer characteristics are shown in the Fig. 1.121.

➠ **Example 1.20 :** *Sketch the output waveform for a clipper circuit shown in the Fig. 1.122. Also obtain the peak magnitude of the output waveform. Assume silicon diode.*

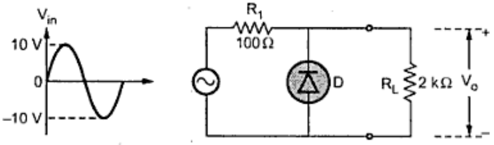


Fig. 1.122

Solution : This is a basic parallel clipper with negative clipping. For positive half cycle of input, the diode D is reverse biased and acts as an open circuit hence $V_o = V_{in}$. But the magnitude of the output voltage is,

$$V_o = V_{in} \times \frac{R_L}{R_1 + R_L} = 10 \times \frac{2 \times 10^3}{[2 \times 10^3 + 100]} = 9.5238 \text{ V}$$

This is peak value of the output voltage.

For negative half cycle of V_{in}, the diode is forward biased when $V_i < -0.7$ V and

$V_o = -V_\gamma = -0.7$ V.

The input-output waveforms are shown in the Fig. 1.123.

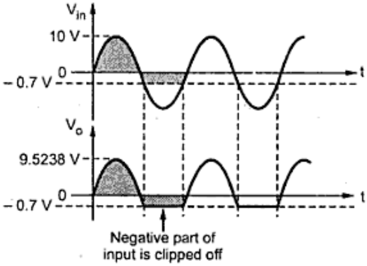


Fig. 1.123

1.35 Parallel Clipper Circuits with Reference Voltage V_R

If it is necessary to have reference voltage level for clipping, other than V_γ then an external battery can be used in the basic circuit.

Key Point: *The introduction of battery in series with the diode is effective in clipping the a.c. voltage waveform above the certain reference voltage called* ***bias voltage or reference voltage.***

Reference voltage is denoted as V_R. The Fig. 1.124 shows the basic parallel positive clipper circuit with reference voltage.

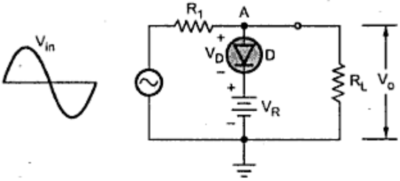


Fig. 1.124 Positive clipper with reference voltage

1.35.1 Operation

The operation for **positive half cycle** of the input can be divided into two cases.

Case 1 : V_i is positive but less than V_R

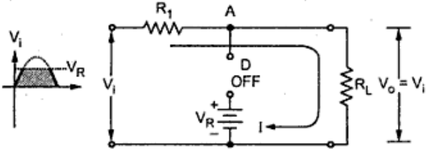


Fig. 1.125 0 V < V_i < V_R

When V_i is positive but less than V_R, the diode D is **reverse biased** and acts as open circuit. The equivalent circuit is as shown in the Fig. 1.125.

Hence the output voltage

$$V_o = V_i \frac{R_L}{R_1 + R_L}$$

But selecting $R_1 << R_L$,

$$V_o \approx V_i \qquad ...(1)$$

Case 2 : V_i positive and greater than V_R

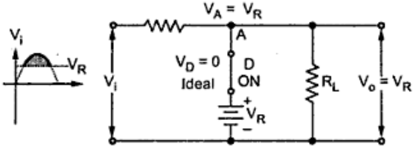


Fig. 1.126 V_i > V_R

Assuming **ideal diode,** when V_i becomes greater than V_R, the diode D becomes **forward biased** and acts as short circuit. This is shown in the Fig. 1.126. The output voltage now is same as voltage of node A which is V_R, as the drop across ideal ON diode is zero.

$$\therefore \qquad V_o = V_R \qquad \text{... for} \quad V_i > V_R \qquad \text{... (2)}$$

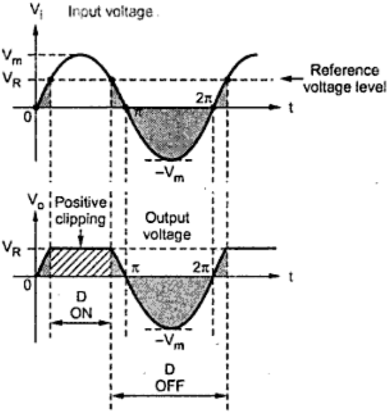
When V_o again becomes less than V_R, the diode D becomes OFF and $V_o \approx V_i$.

For the entire **negative half cycle** of the input, $V_i < V_R$ hence diode D remains reverse biased. It acts as open circuit.

$$\therefore \qquad V_o = \frac{V_i R_L}{R_1 + R_L} \approx V_i \qquad \text{... } R_1 << R_L \qquad \text{... (3)}$$

Key Point: *The entire negative half cycle is reproduced at the output.*

The input and output waveforms are shown in the Fig. 1.127.



V_i
Input voltage
V_m
V_R
Reference voltage level
2π
π
t
0
$-V_m$
V_o
Positive clipping
Output voltage
V_R
π
2π
t
0
D ON
$-V_m$
D OFF

Fig. 1.127 Waveforms for positive parallel clipper with V_R

1.35.2 Transfer Characteristics

The mathematical equations for transfer characteristics are,

$$\boxed{\begin{array}{ll} V_o = V_i & \text{... for } V_i \le V_R \\ V_o = V_R & \text{... for } V_i > V_R \end{array}}$$

The transfer characteristics are shown in the Fig. 1.128.

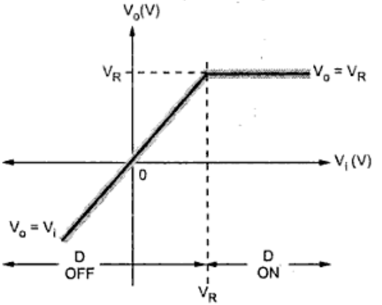


Fig. 1.128 Transfer characteristics

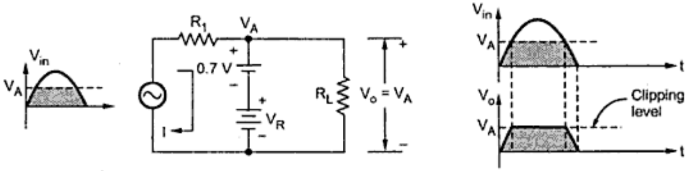
1.35.3 Effect of Cut-in Voltage of Diode

Let the diode is non-deal with cut-in voltage $V_\gamma = 0.7$ V

Key Point: *For diode D to be ON, the potential of node A must be 0.7 V more than V_R.*

So $V_A = 0.7 + V_R$ for diode ON

During the positive half-cycle of the input voltage V_{in} , as long as $V_{in} < V_A$, the diode will not conduct. But when $V_{in} = V_A$ the diode starts conducting and the output voltage $V_o = V_A = 0.7 + V_R$. This is shown in the Fig. 1.129.



(a) $V_{in} > V_A$

(b) Waveforms

Fig. 1.129

But when $V_{in} < V_A$ and throughout negative half cycle the diode is reverse biased and acts as open circuit and hence $V_o = V_{in}$. The magnitude of V_o remains same as obtained before, for clipper without V_R.

$$\therefore \quad V_o = V_{in} \frac{R_L}{R_1 + R_L} = V_{in} \qquad \ldots R_1 << R_L$$

Thus entire negative half cycle is reproduced as it is, at the output. The circuit acts as positive clipper with the clipping level as V_A other than V_γ.

The input-output waveforms are shown in the Fig. 1.130.

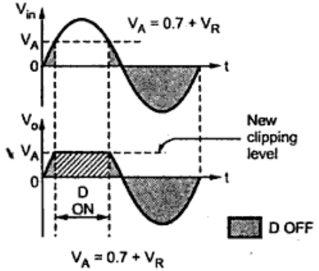


Fig. 1.130 Biased clipper waveforms with non-ideal diode

The dashed portion is the clipping region of the circuit. For ideal diode, $V_\gamma = 0$ and hence clipping level is $V_A = V_R$.

Key Point:*Varying the reference voltage up or down, the clipping level of the circuit can be changed, as per the requirement.*

The transfer characteristics equations are,

$$\boxed{\begin{aligned} V_o &= V_A, & \ldots V_{in} \geq V_A \\ V_o &= V_{in}, & \ldots V_{in} < V_A \end{aligned}}$$

The transfer characteristics are shown in the Fig. 1.131.

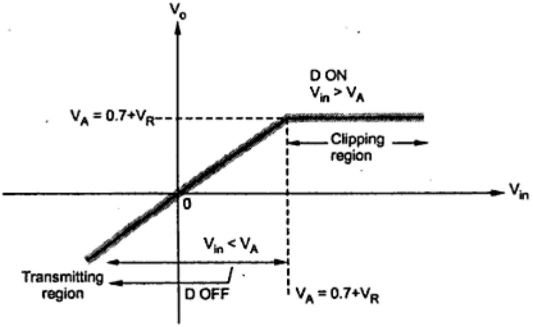


Fig. 1.131 Transfer characteristics

1.35.4 Parallel Negative Clipper with Reference Voltage V_R

The Fig. 1.132 shows parallel negative biased clipper with bias reference voltage V_R. This is obtained by reversing the direction of diode in a parallel positive clipper with reference voltage V_R.

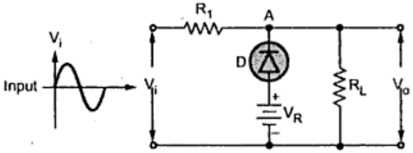


Fig. 1.132 Parallel negative clipper with V_R

Operation : Assume ideal diode

During positive half cycle of the input, when $V_i = 0\,V$, due to V_R diode is forward biased immediately.

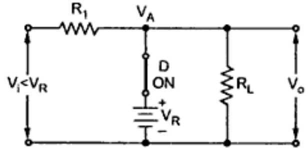


Fig. 1.133 D ON, $V_i < V_R$

The voltage of node A is $V_A = V_R$ when diode is ON as shown in the Fig. 1.133.

$\therefore\ V_o = V_A = V_R$ ... D ON.

The condition exists as long as $V_i < V_R$.

When increasing V_i becomes greater than V_R, the diode D becomes reverse biased. The circuit is as shown in the Fig. 1.134.

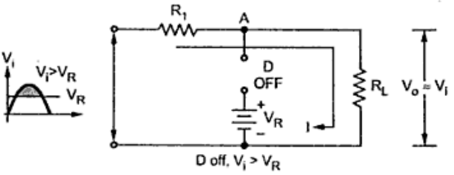


Fig. 1.134 D OFF, $V_i > V_R$

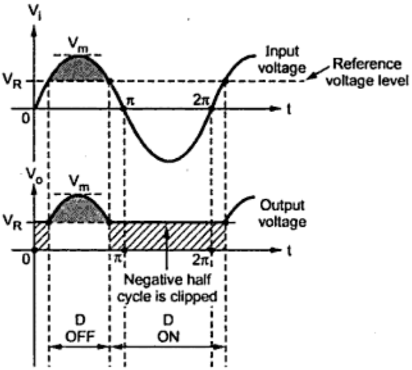
The output voltage follows the input voltage.

$$V_o = \frac{V_i\ R_L}{R_1 + R_L} \approx V_i \ \text{....}\ R_1 << R_L$$

When V_i becomes less than V_R, the diode D again becomes ON and $V_o = V_R$. The diode D remains ON for entire **negative half cycle** of the input and for which $V_o = V_R$.

Key Point: *The entire negative half cycle of the input is clipped off and the circuit acts as parallel negative clipper.*

The input and output waveforms are shown in the Fig. 1.135.



V_i
V_m
V_R
0
π
2π
t
Input voltage
Reference voltage level
V_o
V_m
V_R
0
π
2π
t
Output voltage
Negative half cycle is clipped
D OFF
D ON

Fig. 1.135 Waveforms for negative parallel clipper with V_R

Transfer characteristics : The equations for the transfer characteristics are,

$$V_o = V_i, \quad \ldots \text{ for } V_i > V_R$$

$$V_o = V_R, \quad \ldots \text{ for } V_i \le V_R$$

The transfer characteristics are shown in the Fig. 1.136.

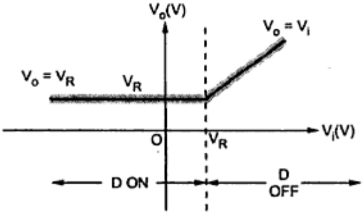


Fig. 1.136 Transfer characteristics for negative clipper with V_R

Example 1.21 : *Draw the output voltage waveforms for the circuit shown if input voltage is square wave of amplitude 5 V. Assume ideal diode. Identify the circuit.*

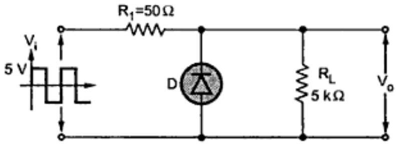


Fig. 1.137

Solution : 1. For **positive half cycle** of the input, $V_i = 5\,V$ hence diode D is **reverse biased** and hence current I flows as shown in the Fig. 1.137(a).

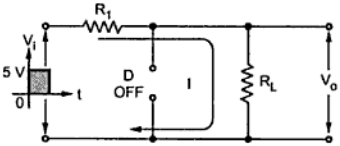


Fig. 1.137(a)

$$V_o = IR_L$$

$$I = \frac{V_i}{R_1 + R_L}$$

$$\therefore\ V_o = \frac{V_i R_L}{R_1 + R_L}$$

$$\therefore\ V_o = V_i \times \frac{5000}{5000+50}$$

$$= 0.99\ V_i \approx V_i$$

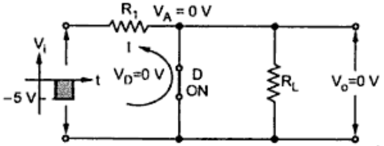


Fig. 1.137 (b)

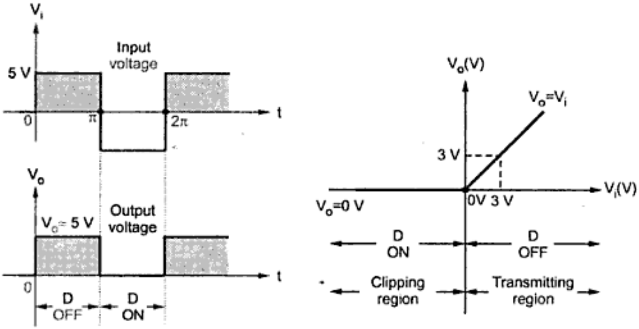
2. For **negative half cycle** of the input, the diode D is **forward biased** and becomes ON. The drop across it is 0 V as it is ideal. Hence R_L gets bypassed through short provided by diode.

$\therefore\ V_o = 0\,V$ as shown in the Fig. 1.137 (b).

$$\text{Thus,}\quad V_o = V_i \qquad \text{....}\ V_i > 0\,V$$

$$V_o = 0 \qquad \text{...}\ V_i < 0\,V$$

The input-output waveforms are shown in the Fig. 1.138 (a) while transfer characteristics are shown in the Fig. 1.138 (b).



(a) Waveforms

(b) Transfer characteristic

Fig. 1.138

Key Point : *As the negative half cycle of the input is clipped and diode D is in parallel with load* R_L, *the circuit is* ***parallel negative clipper.***

1.36 Two Way Parallel Clipper Circuit

In this circuit it is required to clip off the portions of both positive and negative half cycles of the input. For this clipping at two different levels is required.

Key Point: *Combining positive and negative clipper circuits with* V_R, *a two way parallel clipper can be obtained.*

The circuit diagram of two way paralle clipper is shown in the Fig. 1.139.

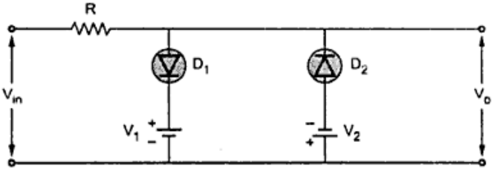


Fig. 1.139 Two way parallel clipper

Assume that the input is purely sinusoidal in nature.

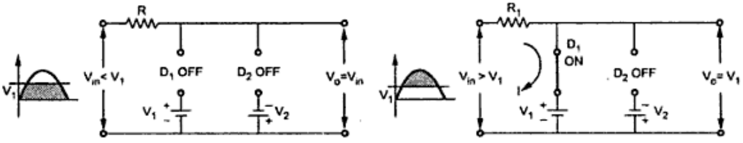
$$V_{in} = V_m \sin \omega t$$

The diodes D_1 and D_2 are ideal diodes.

1.36.1 Operation

Positive half cycle of the input : When V_{in} goes positive till it becomes more than V_1, D_1 and D_2, both the diodes are reverse biased. And $V_o = V_{in}$

When $V_{in} > V_1$, then D_1 becomes forward biased and conducts. While D_2 remains reverse biased for the entire positive half cycle of the input. This shown in the Fig. 1.140 (a) and (b).


R
V1
Vin< V1
D1 OFF
D2 OFF
Vo=Vin
V1
V2
R1
V1
Vin > V1
I
D1 ON
D2 OFF
Vo= V1
V1
V2

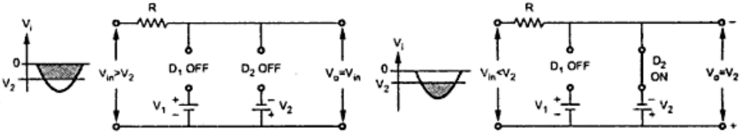
(a) $V_{in} < V_1$ (b) $V_{in} > V_1$

Fig. 1.140 Positive half cycle of input

Thus when $V_{in} < V_1$, D_1 and D_2 are OFF and $V_o = V_{in}$

While when $V_{in} > V_1$, D_1 is ON D_2 is OFF and $V_o = V_1$

Negative half cycle of the input : In the negative half cycle, as long as V_{in} is greater than V_2, the diode D_2 remains reverse biased. The D_1 remains OFF for the entire negative half cycle of the input. This is shown in the Fig. 1.141 (a). The $V_o = V_{in}$

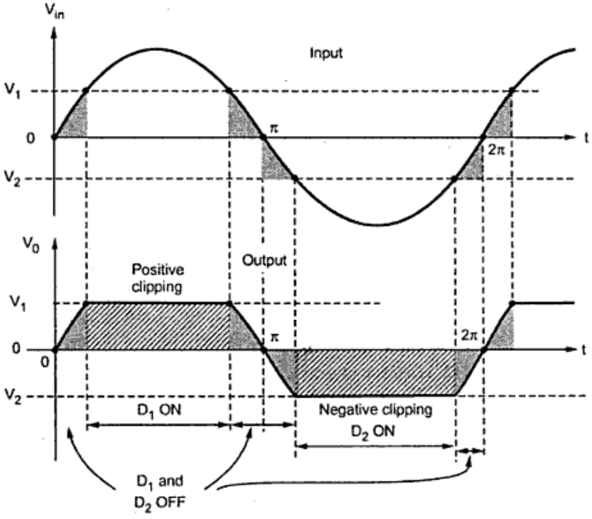

R
Vi
0
V2
Vin>V2
D1 OFF
D2 OFF
Vo=Vin
V1
V2
R
Vi
0
V2
Vin<V2
D1 OFF
D2 ON
Vo=V2
V1
V2
-
+

(a) $V_{in} > V_2$ (b) $V_{in} < V_2$

Fig. 1.141 Negative half cycle of input

When V_{in} becomes less than V_2, the diode D_2 becomes forward biased and conducts. The diode D_1 is still OFF. This is shown in the Fig. 1.141 (b) where $V_o = V_2$. The output V_o is negative as the polarities of V_2 are opposite to that of V_1.

The input and output waveforms for the two way clipper are shown in the Fig. 1.142.



V_{in}
Input
V_1
0
V_2
π
2π
t
V_0
Positive clipping
Output
V_1
0
0
V_2
π
2π
t
D_1 ON
Negative clipping
D_2 ON
D_1 and D_2 OFF

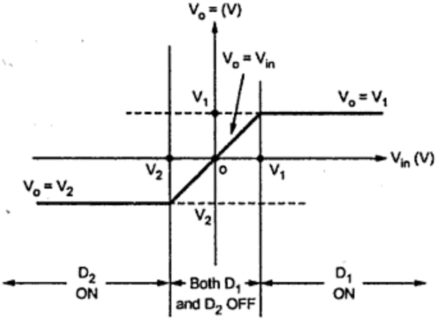
Fig. 1.142 Waveforms for two way parallel clipper

1.36.2 Transfer Characteristics

The mathematical equations for the two way clipper are,

$$\therefore \boxed{\begin{array}{ll} \left.\begin{array}{ll} V_o = V_{in} & \ldots\text{for } V_{in} < V_1 \\ V_o = V_1 & \ldots\text{for } V_{in} > V_1 \end{array}\right\} & \text{Positive half cycle} \\ \left.\begin{array}{ll} V_o = V_{in} & \ldots\text{for } V_{in} > V_2 \\ V_o = V_2 & \ldots\text{for } V_{in} < V_2 \end{array}\right\} & \text{Negative half cycle} \end{array}}$$

The transfer characteristics are shown in the Fig. 1.143.



V_o = (V)
V_o = V_{in}
V₁
V_o = V₁
V_{in} (V)
V₂
o
V₁
V_o = V₂
V₂
D₂ ON
Both D₁ and D₂ OFF
D₁ ON

Fig. 1.143 Transfer characteristics for two way clipper

Key Point: *Thus the circuit clips the input for both positive as well as negative half cycles and hence called two way parallel clipper circuit.*

1.37 Clamper Circuits

Sometimes it is necessary to add a d.c. level to the a.c. output signal.

Key Point: *The circuits which are used to add a d.c. level as per the requirements to the a.c. output signal are called* ***clamper circuits.***

The capacitor, diode and resistance are the three basic elements of a clamper circuit. The clamper circuits are also called **d.c. restorer** or **d.c. inserter circuits.**

Depending upon whether the positive d.c. or negative d.c. shift is introduced in the output waveform, the clampers are classified as,

a) Negative clampers

b) Positive clampers

Let us study these two circuits.

1.37.1 Negative Clamper

A simple negative clamper which adds a negative level to the a.c. output is shown in the Fig. 1.144. It consists of a capacitor C, the ideal diode D and the load resistance R_L.

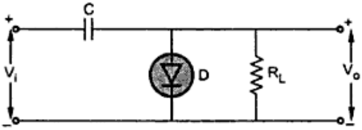


Fig. 1.144 Negative clamper

The following **assumptions** are made while analysing the clamper circuit;

1. The diode is ideal in behaviour.
2. The time constant τ = RC is designed to be very large by selecting large values of R and C.

Operation :

During the first quarter of **positive cycle** of the input voltage V_i, the capacitor gets charged through **forward biased diode** D upto the maximum value V_m of the input signal V_i. The capacitor charging is almost instantaneous, which is possible by selecting proper values of C and R_L in the circuit. The capacitor once charged to V_m, acts as a battery of voltage V_m as shown in the Fig. 1.145.

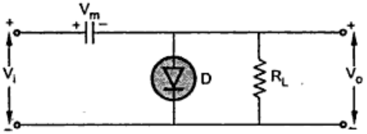


Fig. 1.145

Thus when D is ON, the output voltage V_o is zero. As input voltage decreases after attaining its maximum value V_m, the capacitor remains charged to V_m and the diode D becomes reverse biased.

Due to large RC time constant the capacitor holds its entire charge and capacitor voltage remains as $V_C = V_m$ as shown in the Fig. 1.146.

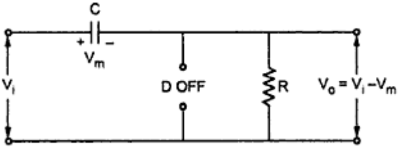


Fig. 1.146

And the output voltage V_o is now given by,

$$V_o = V_i - V_C = V_i - V_m \quad \text{... (1)}$$

Key Point: *This is as good as adding a negative d.c. level equal to* $-V_m$ *to the output.*

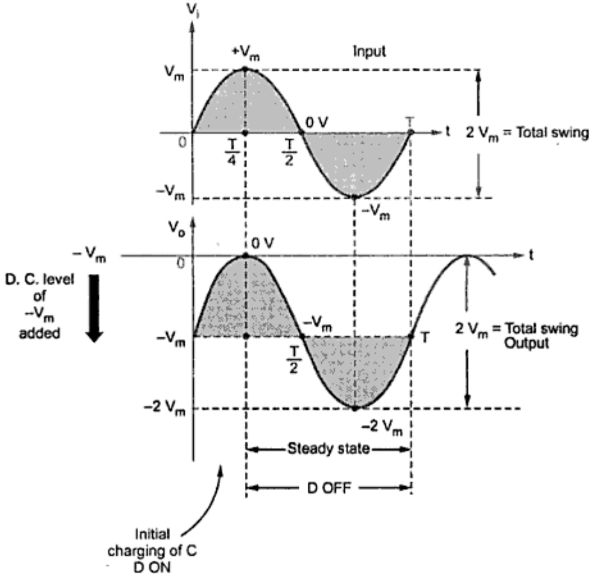
In the negative half cycle of V_i, the diode will remains reverse biased. The capacitor starts discharging through the resistance R_L. As the time constant R_LC is very large, it can be approximated that the capacitor holds all its charge and remains charged to V_m, during this period also. Hence we can write again that,

$$V_o = V_i - V_C = V_i - V_m \quad \text{.... for negative half cycle} \qquad \text{... (2)}$$

$$\boxed{\begin{array}{ll} V_o = -V_m, & \text{for } V_i = 0 \\ V_o = 0, & \text{for } V_i = V_m \\ V_o = -2V_m, & \text{for } V_i = -V_m \end{array}}$$

Waveforms :

Assuming ideal diode, the input and output waveforms are shown in the Fig. 1.147.



V_i
$+V_m$
Input
V_m
0 V
T
t
$2 V_m$ = Total swing
0
$\frac{T}{4}$
$\frac{T}{2}$
$-V_m$
$-V_m$
V_o
0 V
$-V_m$
t
0
D. C. level of $-V_m$ added
$-V_m$
$-V_m$
$\frac{T}{2}$
T
$2 V_m$ = Total swing Output
$-2 V_m$
$-2 V_m$
Steady state
D OFF
Initial charging of C D ON

Fig. 1.147 Negative clamper waveforms

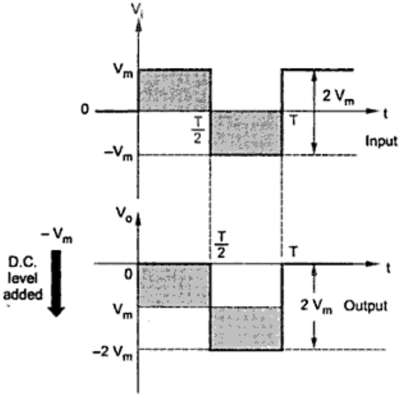


Fig. 1.148 Waveforms for square wave input

The peak to peak amplitude of the input is 2 V_m, similarly the peak to peak amplitude of the output is also 2 V_m. **Thus the total swing of the output is always same as the total swing of the input, for a clamper circuit.**

Square wave input :

If the same clamper circuit is subjected to square wave type input, capacitor charges to peak value of input voltage almost instantaneously and net output in positive half cycle remains zero. In negative half cycle, the output swings to twice the peak value of the voltage and remains constant during negative half cycle of the input voltage V_i.

Key Point: *The total swing of the output is same as the total swing of the input.*

The Fig. 1.148 shows the input and output waveforms for square wave input.

1.37.2 Positive Clamper

The circuit is shown in the Fig. 1.149.

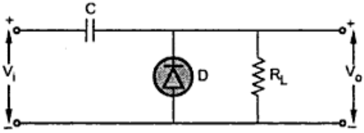


Fig. 1.149 Positive clamper

Key Point: *By changing the orientation of the diode in the negative clamper, the positive clamper circuit can be achieved.*

Operation :

During the first quarter of **negative half cycle** of the input voltage V_i, diode D gets forward biased and almost instantaneously capacitor gets charged equal to the maximum value V_m of the input signal V_i, with the polarities as shown in the Fig. 1.150.

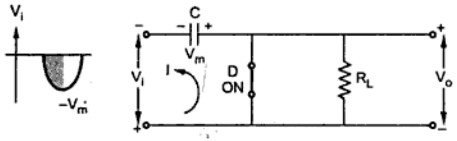


Fig. 1.150

The capacitor once charged to V_m, acts as a battery of voltage V_m with the polarities as shown in the Fig. 1.150.

This is because RC time constant is very large hence capacitor holds its entire charge all the time.

Thus when $V_i = V_m$, the output voltage V_o is 2 V_m. Under steady state conditions we can write,

$$V_o = V_i + V_m$$

In the **positive half cycle**, the diode D is reverse biased. The capacitor starts discharging through R_L. But due to large time constant, it hardly gets discharged during positive half cycle of V_i. This is shown in the Fig. 1.151.

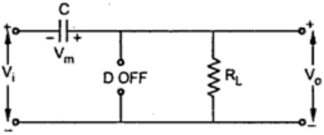


Fig. 1.151 Positive half cycle

Key Point: *The capacitor holds its entire charge, all the time.*

Hence, $V_o = V_i + V_m$

$V_o = V_m$,	for $V_i = 0$
$V_o = 2\ V_m$,	for $V_i = V_m$
$V_o = 0$,	for $V_i = -V_m$

Waveforms :

Assuming ideal diode, the input and output waveforms are shown in the Fig. 1.152.

(See Fig. 1.152 on next page.)

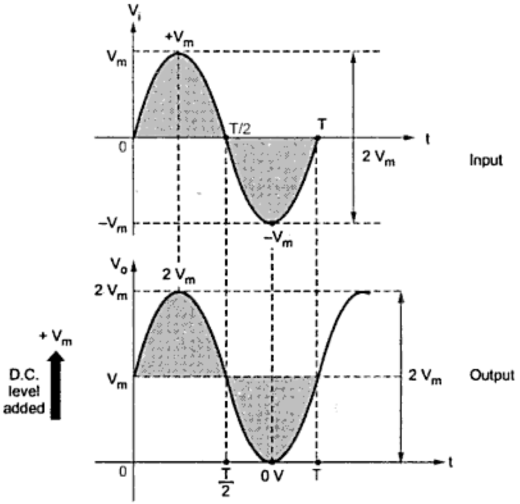


Fig. 1.152 Positive clamper waveforms

1.37.3 Steps to Analyze Clamping Network

The following steps are useful in analyzing the clamping networks :

1) Start the analysis of the clamping network by considering that part of the input which will forward bias the diode.
2) When the diode is conducting, assume that the capacitor charges instantaneously to a voltage level determined by the input.
3) Assume that when the diode is not conducting, due to the large time constant, capacitor maintains its established voltage level.
4) Analyse the output, taking care of its polarities. Sketch the output waveform.

Key Point : *As a crosscheck it can be remembered that the total output swing is always equal to the total input swing.*

1.37.4 Addition of Battery in Clamper

The addition of d.c. level and shape of the output can be controlled by adding additional voltage supply in series with the diode with the polarity, as per the requirement. One such clamping network is shown in the Fig. 1.153.

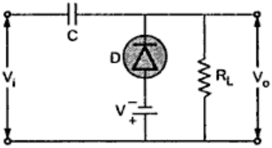


Fig. 1.153

Operation :

During **first quarter of negative half cycle,** When V_i becomes less than V, the diode D becomes forward biased. The capacitor gets charged instantaneously to $V_m - V$ as shown in the Fig. 1.154.

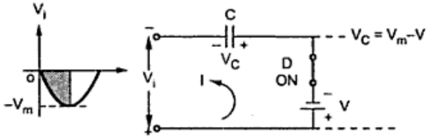


Fig. 1.154 Charging of capacitor

There after capacitor retains its charge all the time and its voltage remains at $V_C = V_m - V$

Due to this, the diode D now remains reverse biased. During positive half cycle, the circuit behaves as shown in the Fig. 1.155.

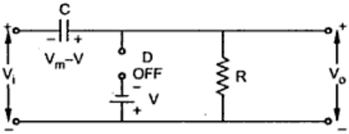


Fig. 1.155 Positive half cycle

Applying KVL to the circuit,

$$+V_C - V_o + V_i = 0$$

$$\therefore \quad V_o = V_i + V_C = V_i + (V_m - V) \qquad ...(1)$$

Key Point: *Thus the d.c. shift of* V_m - V *gets added to the input to produce the output.*

From the equation 1,

$$\therefore \quad V_o = 2V_m - V \qquad ... V_i = +V_m$$

$$V_o = V_m - V \qquad ... V_i = 0$$

$$V_o = -V \qquad ... V_i = -V_m$$

The input and output waveforms are shown in the Fig. 1.156.

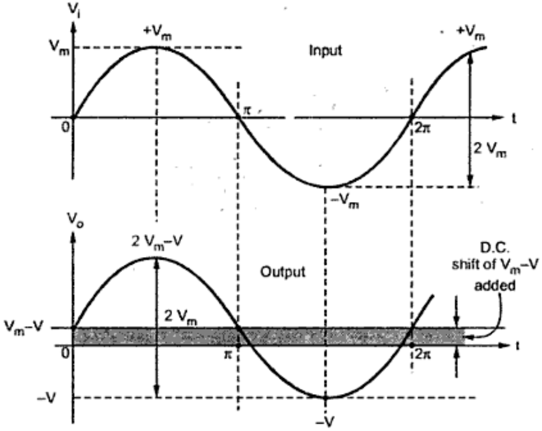

V_i
+V_m
+V_m
V_m
Input
0
π
2π
t
2 V_m
-V_m
V_o
2 V_m-V
Output
D.C. shift of V_m-V added
2 V_m
V_m-V
0
π
2π
t
-V
-V

Fig. 1.156 Waveforms for clamper with d.c. source

1.37.5 Clamper Application

The clamper circuits are often used in the television receivers as d.c. restorer. The video signal in television is processed through capacitively coupled amplifiers hence the

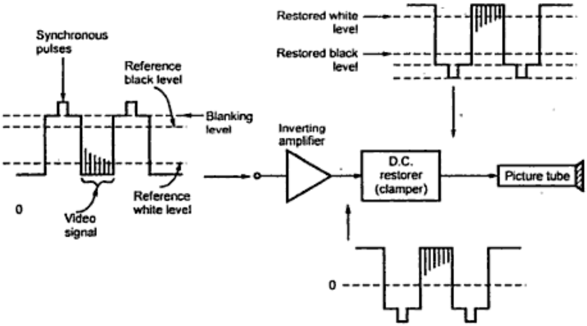

Synchronous pulses
Reference black level
Blanking level
Reference white level
Video signal
0
Inverting amplifier
Restored white level
Restored black level
D.C. restorer (clamper)
Picture tube
0

Fig. 1.157 Use of clamper circuit in television receiver

signal losts its d.c. component which effectively loses black and white reference levels and the blanking level. Hence it is necessary to restore these levels back before applying signal to the picture tube. This is done by a clamper circuit acting as a d.c. restorer. This is shown in the Fig. 1.157.

1.38 Voltage Multipliers

The voltage multipliers are used to step up the output voltage level to two, three or more times the peak voltage of the input. Such circuits use clamping action. Such circuits can be used in bridge rectifiers to increase the level of output d.c. voltage. The various voltage multiplier circuits are,

1. Voltage doubler.
2. Voltage tripler
3. Voltage quadrapler

Each circuit is further classified as,

a. Half wave multiplier and b. Full wave multiplier.

1.38.1 Half Wave Voltage Doubler

The Fig. 1.158 shows the circuit diagram of a **half wave voltage doubler** which gives d.c. voltage output equal to 2 V_m where V_m is the maximum value of the input a.c. voltage.

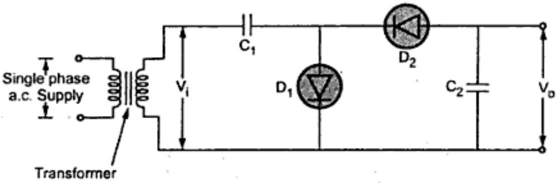


Fig. 1.158 Half wave voltage doubler

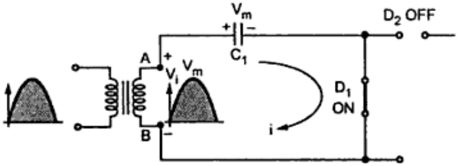


Fig. 1.159

Operation :

Let us see the operation of the circuit assuming ideal diodes.

Positive half cycle of input :

During positive half cycle of V_i, D_1 will be forward biased and the diode D_2 will be reverse biased. The capacitor C_1 will get charged equal to V_m as shown in the Fig 1.159.

The charging of capacitor C_1 is very fast. As D_2 is reverse biased, next part of the circuit remains disconnected from the circuit.

Negative half cycle of input :

During negative half cycle, the diode D_1 will be reverse biased and the diode D_2 will be forward biased. So capacitor C_2 will get charged equal to 2 V_m with the polarities as shown in Fig. 1.160. The capacitor C_2 charges equal to 2 V_m as the voltage V_m on C_1 adds to the input voltage. The capacitor C_1 retains its voltage V_m all the time, once charged. The peak value of input is V_m with polarities such that point A is negative and B is positive.

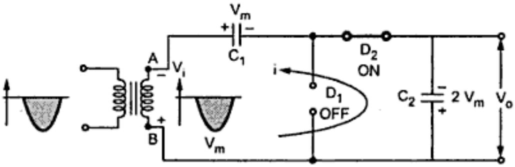


Fig. 1.160

Applying KVL to the loop,

$$+V_m - V_{C2} + V_{C1} = 0$$

Where V_m = Peak value of V_i

V_{C1} = Voltage of capacitor C_1

V_{C2} = Voltage of capacitor C_2

But $V_{C1} = V_m$

$$\therefore \quad V_{C2} = V_m + V_{C1} = V_m + V_m$$

$$= 2V_m$$

This proves that the capacitor C_2 charges to $2V_m$ with the polarities as shown. It retains this voltage as long as load is connected to the circuit.

Action when load is connected :

If load is connected to the circuit, the voltage across C_2 drops during positive half cycle and is again recharged to $2V_m$ in the next negative half cycle. As capacitor charges in alternate half cycle, the circuit is called **half wave doubler circuit.** The output waveform will be similar to the half wave signal filtered by capacitor input filter.

Key Point: *The P.I.V. rating of each diode is* $2V_m$.

1.38.2 Full Wave Voltage Doubler

The Fig. 1.161 (a) shows a full wave voltage doubler.

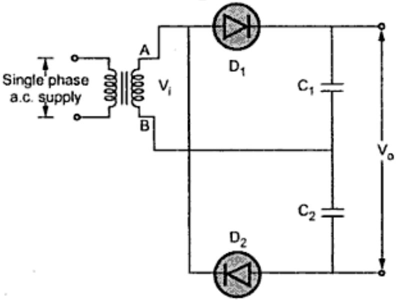


Fig. 1.161 (a) Full wave voltage doubler

Positive half cycle of input :

In the positive half cycle of the secondary voltage of transformer, the diode D_1 is forward biased and the capacitor C_1 charges equal to V_m, the peak of secondary transformer voltage, assuming ideal diodes. This is shown in the Fig. 1.161 (b).

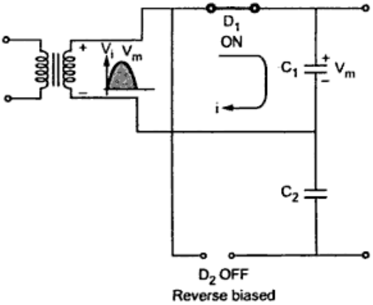


Fig. 1.161 (b) Positive half cycle of input

Negative half cycle of input :

In the negative half cycle of the secondary voltage of transformer, the diode D_2 is forward biased while the diode D_1 is reverse biased. The capacitor C_2 gets charged equal to V_m with the polarity as shown in the Fig. 1.162.

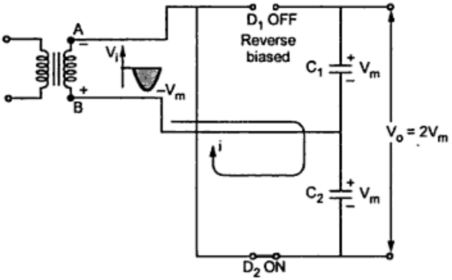


Fig. 1.162 Negative half cycle of input

The output is taken across 2 capacitors in series.

$$\therefore V_o = V_{C1} + V_{C2} = V_m + V_m = 2V_m$$

On no load, the output voltage V_o is almost 2 V_m. But if load resistance R_L is connected across output terminals, the charge on capacitors continuously decreases and capacitor voltages will start decreasing. Hence voltage regulation of such circuit is poor.

The voltage rating of the capacitors C_1 and C_2 is V_m volts each while the P.I.V. rating of the diodes D_1 and D_2 is 2 V_m.

> **Key Point**: *Both full wave and half wave doubler circuits provide twice the peak voltage of the transformer secondary, without the necessity of centre tap.*

Why regulation is poor ?

When load is connected, capacitors start discharging through the load and capacitor voltages start decreasing.

Similarly the series combination of C_1 and C_2 supplies the load current. Thus C_1 and C_2 appears to be in series from the load point of view. The equivalent capacitance as experienced by load circuit from filtering point of view now becomes,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \quad \text{... } C_1 \text{ and } C_2 \text{ in series.}$$

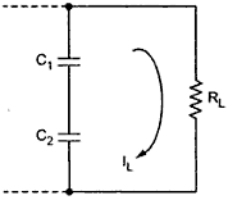


Fig. 1.163 C_1 and C_2 in series from load point of view

This value is less than individual value of C_1 and C_2. The **ripple factor** is inversely proportional to the value of filtering capacitor.

Thus ripple facor increases which indicates that ripple content in the output increases as filtering action is poor. Due to this, the voltage regulation is poor. For higher load current, the capacitors discharge more and not able to provide constant voltage. Hence regulation is poor at higher load current.

Key Point: *PIV rating of each diode D_1 and D_2 is $2V_m$.*

➡ **Example 1.22 :** *A certain voltage doubler has 25 V rms as its input voltage. What is the output voltage? What is the PIV rating of the diode ?*

Solution :

$$V_i = \text{input voltage} = 25 \text{ V rms}$$

$$\therefore \quad V_m = \sqrt{2}\ V_i(\text{rms}) = \sqrt{2}\times 25 = 35.3553 \text{ V}$$

For voltage doubler circuit,

$$V_o = 2V_m = 2\times 35.3553 = 70.7106 \text{ V}$$

The PIV rating of diodes is,

$$\text{PIV} = 2V_m = 70.7106 \text{ V}$$

The same idea can be extended to have the output three times or four times, the peak of the transformer secondary.

Key Point: *The diodes and capacitors get connected in ladder fashion to obtain higher voltage multipliers. Hence the circuits are also called **ladder type multipliers.***

1.38.3 Voltage Tripler

The voltage tripler can be obtained by adding one more diode-capacitor section to the half wave doubler circuit. The circuit is shown in the Fig. 1.164.

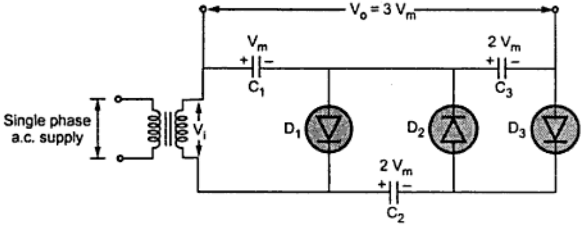

$V_o = 3V_m$
V_m
+ −
C_1
$2V_m$
+ −
C_3
Single phase a.c. supply
V_i
D_1
D_2
D_3
$2V_m$
+ −
C_2

Fig. 1.164 Voltage tripler

Operation :

During **first positive half cycle** of the input, the diode D_1 becomes forward biased while D_2 and D_3 are reverse biased. The capacitor C_1 charges to V_m with the polarities as shown in the Fig. 1.165.

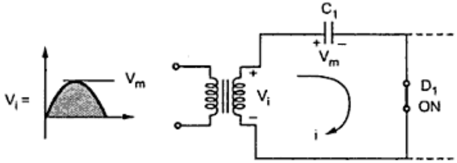

C_1
+ −
V_m
$V_i =$
V_m
+
V_i
−
i
D_1
ON

Fig. 1.165

During **next negative half cycle** of the input, the diode D_2 is forward biased. The capacitor C_1 holds its entire charge and its voltge remains at V_m. Hence the capacitor C_2 charges to $2V_m$ with the polarities as shown in the Fig. 1.166.

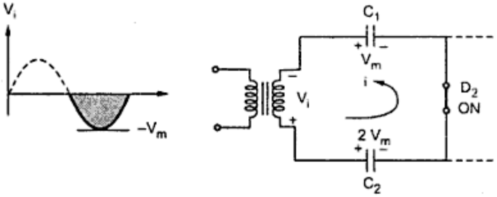

V_i
$-V_m$
C_1
+ −
V_m
−
V_i
+
i
D_2
ON
$2V_m$
+ −
C_2

Fig. 1.166

The diodes D_1 and D_3 are reverse biased.

Applying KVL,

$$+V_m - V_{C2} + V_{C1} = 0$$

$$\therefore \quad V_{C2} = V_m + V_{C1} = 2V_m$$

In the **next positive half cycle** of the input, the diode D_3 is forward biased as C_2 retains its charge and voltage to $2V_m$ while C_1 retains its voltage to V_m. The diodes D_1 and D_2 are reverse biased. Thus the capacitor C_3 charses to $2V_m$ through forward biased D_3 with the polarities as shown in the Fig. 1.167.

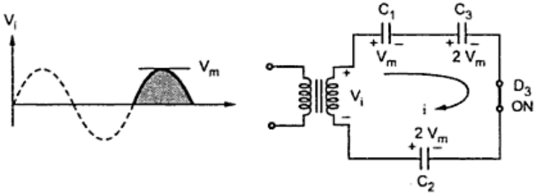


Fig. 1.167

Applying KVL,

$$+V_m - V_m - V_{C3} + V_{C2} = 0$$

$$\therefore \quad V_{C3} = V_{C2} = 2V_m$$

The output V_o is taken across the capacitors C_1 and C_3.

$$\therefore \quad V_o = V_{C1} + V_{C3} = V_m + 2V_m$$

$$= 3V_m$$

Key Point: *Thus the output is three times the peak of the input voltage and circuit works as **voltage tripler**.*

Key Point: *PIV rating of each diode D_1, D_2 and D_3 is $2V_m$.*

The limitations of poor regulation and filtering due to higher lood current and two capacitors C_1 and C_3 in series suplying the load continue for this circuit as well.

1.38.4 Voltage Quadrupler

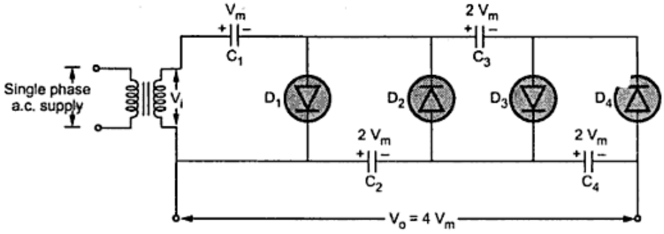


Fig. 1.168 Voltage quadrupler

The addition of another diode and capacitor section to the voltage tripler gives a voltage quadrupler. The circuit is shown in the Fig. 1.168.

The capacitor C_4 charges to $2V_m$, with the polarity shown in a negative half cycle, through D_4 which is $4V_m$.

Key Point: *The P.I.V. of each diode is* $2V_m$.

1.38.5 Advantages, Applications and Limitations

The important advantage of multipliers is the use of clamping action to increase peak rectified voltage without increasing the rating of the input transformer. This is economical. The centre tap transformer is also not required in the multiplier circuit.

Due to poor regulation at higher load currents, the multipliers are used in the high voltage low current applications. The multipliers are used in applications like television receivers and cathode ray tube (CRT) anode voltages.

One important disadvantage of such circuits is, as more and more stages of diode and capacitor are added to a chain, the output voltage keeps on falling substantially.

Key Point : *The ripple also increases according to the increased load current. The voltage regulation becomes more poor and poor. Hence these circuits are useful in very low current applications only.*

Examples with Solutions

Example 1.23 : *A p-n junction diode has at a temperature of 125°C a reverse saturation current of 30 μA. At a temperature of 125 °C find the dynamic resistance for 0.2 V bias in forward and reverse direction.*

Solution : The given values are,

$T = 125\ ^\circ C,\ V = \pm 0.2\ V,\quad I_0 = 30\ \mu A$

Now $V_T = kT$ at temperature T in °K

$\therefore\quad T = 125 + 273 = 398\ ^\circ K$

and $k = 8.62\times 10^{-5}$ = Boltzmann's constant

$\therefore\quad V_T = 398\times 8.62\times 10^{-5} = 0.034307\ V = 34.3076\ mV$

The dynamic resistance is given by,

$$r = \frac{\eta V_T}{I_0\ e^{V/\eta V_T}}$$

Assume germanium diode, $\eta = 1$

For forward bias, $V = +\ 0.2\ V$

$$\therefore\quad r_f = \frac{1\times 0.0343076}{30\times 10^{-6}\times e^{0.2/0.0343076}} = \mathbf{3.3612\ \Omega}$$

For reverse bias, $V = -\ 0.2\ V$

$$\therefore\quad r_r = \frac{1\times 0.0343076}{30\times 10^{-6}\times e^{-0.2/0.0343076}} = \mathbf{389.078\ k\Omega}$$

Example 1.24 : *For a silicon p-n junction diode*
(i) For what value of reverse voltage will the reverse current reach 90% of its saturation value at room temperature. (ii) Find the ratio of current for a forward bias of 0.2 V to the reverse saturation current for the same magnitude of reverse bias voltage.

Solution : For silicon $\eta = 2$ and $V_T = 26$ mV at 300 °K

(i) Let I_0 be the reverse saturation current at room temperature.

The new current is $-\ 0.9\ I_0$ due to new voltage applied.

So $I = -\ 0.9 I_0$, negative as it is reverse current.

The current equation of diode is,

$$I = I_0\ (e^{V/\eta V_T} - 1)$$

$$\therefore\quad -\ 0.9\ I_0 = I_0\ (\ e^{V/2\times 26\times 10^{-3}} - 1)$$

$$\therefore\quad -\ 0.9 = e^{V/52\times 10^{-3}} - 1$$

$$\therefore\quad e^{V/52\times 10^{-3}} = 0.1$$

$$\therefore \quad \frac{V}{52\times10^{-3}} = ln\ (0.1) = -2.3025$$

$$\therefore \quad \mathbf{V = -0.1198\ V}$$

The negative sign indicates it is reverse biased voltage.

Note : The current equation of diode is applicable for both forward and reverse biased condition of a diode.

(ii) Now forward voltage V = 0.2 V

$$\therefore \quad I = I_0\ [\ e^{0.2/\ 2\times26\times10^{-3}} - 1\ ]$$

$$I = 45.812\ I_0$$

While for reverse bias V = – 0.2 V

$$\therefore \quad I = I_0\ [\ e^{-0.2/\ 2\times26\times10^{-3}} - 1\ ]$$

$$\therefore \quad I = -0.9786\ I_0$$

So the ratio of currents for a 0.2 V of forward and reverse biased conditions is

$$\frac{\text{I when forward biased}}{\text{I when reverse biased}} = \frac{45.812\, I_0}{-0.9786\, I_0} = \mathbf{-46.811}$$

So the ratio is 46.811 while negative sign indicates that the two current directions are opposite to each other.

Example 1.25 : *If the reverse saturation current in a PN junction silicon diode is 1 nA, find the applied voltage for a forward current 0.5 μA.*

Solution : $I_0 = 1$ nA, $I = 0.5\ \mu A$, $\eta = 2$ for silicon

$$I = I_0\left[e^{V/\eta V_T} - 1\right]$$

Assume $V_T = 26$ mV at room temperature

$$\therefore \quad 0.5\times10^{-6} = 1\times10^{-9}\left[e^{V/2\times26\times10^{-3}} - 1\right]$$

$$\therefore \quad \frac{V}{52\times0^{-3}} = ln\ (501)$$

$$\therefore \quad \mathbf{V = 0.3232\ V}$$

Example 1.26 : *Calculate the silicon diode current for the forward bias voltage of 0.6 V at 25° C, if the reverse saturation current is 10 μA.*

Solution : V = 0.6 V, T = 25 °C = 298 °K, $I_0 = 10\ \mu A$, $\eta = 2$

$$\therefore \quad V_T = kT = 8.62\times10^{-5}\times298 = 0.02568\ V$$

$$\therefore \qquad I = I_0\left[e^{V/\eta V_T}-1\right] = 10\times10^{-6}\left[e^{0.6/2\times 0.02568}-1\right]$$

$$= \mathbf{1.18\ A}$$

Example 1.27 : *A germanium diode carriers a current of 1 mA at room temperature when a forward bias of 0.15 V is applied. Estimate the reverse saturation current at room temperature.* **(UPTU, May-2006)**

Solution : $I = 1$ mA, $T = 27\ ^\circ C = 300\ ^\circ K$, $V = 0.15$ V.

For germanium, $\eta = 1$

$$I = I_0\left[e^{V/\eta V_T}-1\right] \quad \text{where } V_T = 26 \text{ mV at } 300\ ^\circ K$$

$$\therefore \qquad 1\times10^{-3} = I_0\left[e^{0.15/26\times10^{-3}}-1\right]$$

$$\therefore \qquad I_0 = \mathbf{3.1319\ \mu A} \qquad \text{... Reverse saturation current}$$

Example 1.28 : *Determine the currents I_1, I_2 and I_{D2} for the network shown in the Fig. 1.169.*

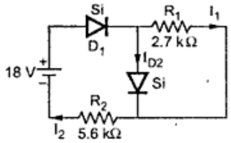


Fig. 1.169

Solution : Due to 18 V supply, both D_1 and D_2 are forward biased and conducting. The drops across D_1 and D_2 are 0.7 V with polarities as shown in the Fig. 1.170.

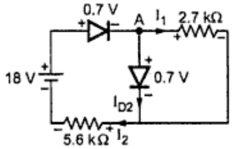


Fig. 1.170

Now $\qquad V_A = 0.7$ V

This is same across R_1.

$$\therefore \qquad I_1 = \frac{V_A}{R_1} = \frac{0.7}{2.7\times10^3}$$

$$= 0.259 \text{ mA}$$

Applying KVL to the loop,

$$-0.7 - 0.7 - I_2\,(5.6\times10^3) + 18 = 0$$

$$\therefore \qquad I_2 = 2.96 \text{ mA}$$

Now $$I_{D2} = I_2 - I_1 = 2.96 - 0.259$$

$$= \mathbf{2.701\ mA}$$

Example 1.29 : *Sketch the output for the given circuit,*

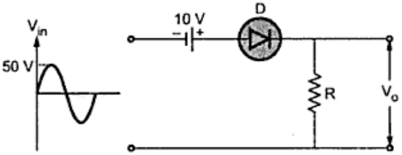


Fig. 1.171

Solution : It can be seen that the diode is forward biased due to 10 V battery.

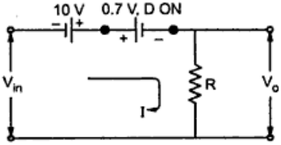


Fig. 1.172

So we can write,

$$V_o = V_{in} + 10 - 0.7 = V_{in} + 9.3 \text{ V}$$

The output is $V_{in} + 9.3$ till the V_{in} value reduces to -9.3 V. So when V_{in} is maximum, output V_o will be at its maximum i.e. $50 + 9.3 = 59.3$ V.

But when V_{in} becomes more negative than -9.3 V then diode is reverse biased and it acts as an open circuit, thus the output is zero till V_{in} becomes more than -9.3 V.

The input-output waveforms are shown in the Fig. 1.173.

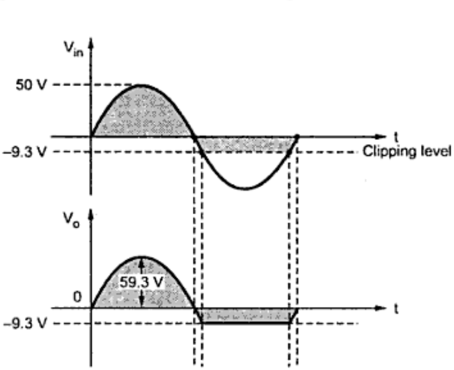


Fig. 1.173

Thus circuit acts as a negative clipper.

Example 1.30 : *Determine V_0 for the network shown,*

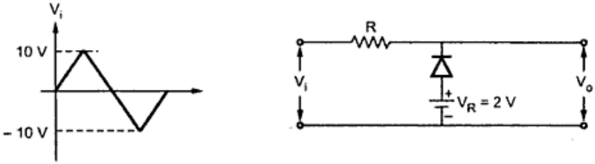


Fig. 1.174

(UPTU, Dec.-2002)

Solution : Assume that the diode is ideal.

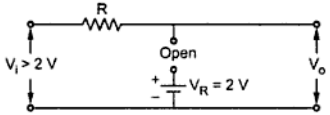


Fig. 1.174(a)

When $V_i > 2$ V, the diode is reverse biased and the circuit becomes as shown in the Fig. 1.174(a).

$$\therefore \qquad V_o = V_i \qquad \ldots V_i > 2 \text{ V}$$

The output is equal to input voltage.

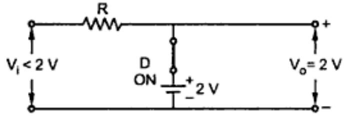


Fig. 1.174 (b)

When V_i becomes 2 V and is less than 2 V, the diode becomes forward biased due to battery of 2 V. The circuit becomes as shown in the Fig. 1.174 (b).

$$\therefore \qquad V_o = 2 \text{ V constant} \qquad \ldots V_i < 2 \text{ V}$$

Thus the overall output voltage is as shown in the Fig. 1.174 (c).

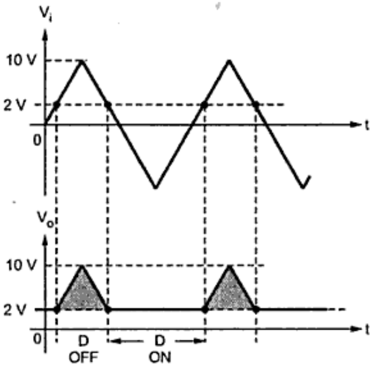


Fig. 1.174 (c)

Example 1.31 : *A symmetrical 5 kHz squarewave varying between +10 V and –10 V is impressed upon the clipping circuit shown. Assuming* $R_f = 0\ \Omega$, $R_r = 2\ M\Omega$ *and* $V_\gamma = 0$ *V. Sketch the steady state output waveform.*

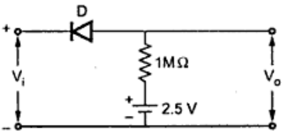


Fig. 1.175

(UPTU, May-2003)

Solution : When V_i is greater than 2.5 V, the diode D is reverse biased with reverse resistance $R_r = 2\ M\Omega$. The circuit is as shown in the Fig. 1.175 (a).

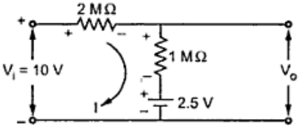


Fig. 1.175(a)

Applying KVL to the loop,

$$-I\times 2\times 10^6 - 1\times 10^6 I - 2.5 + V_i = 0$$

As V_i is square wave, V_i = 10 V instantaneously.

$$\therefore \qquad I = \frac{10-2.5}{3\times 10^6} = 2.5\ \mu A$$

$$\therefore \qquad V_o = I\times 1\times 10^6 + 2.5 = 5\ \textbf{V} \qquad \dots V_i = 10\ V$$

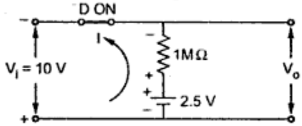


Fig. 1.175 (b)

When V_i becomes − 10 V i.e. less than 2.5 V, the diode becomes forward biased. The circuit becomes as shown in the Fig. 1.175 (b).

Applying KVL,

$$-I\times 1\times 10^6 + V_i + 2.5 = 0$$

$$\therefore \qquad I = \frac{10+2.5}{1\times 10^6} = 12.5\ \mu A$$

$$\therefore \qquad V_o = 2.5 - I\times 1\times 10^6 = 2.5 - 12.5 = -\ \textbf{10 V} \qquad \dots V_i = -10\ V$$

The output voltage is as shown in the Fig. 1.175 (c).

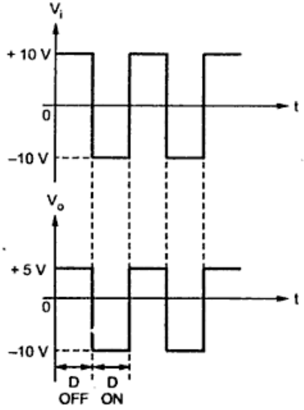


Fig. 1.175 (c)

Example 1.32 : *Sketch the output voltage V_o for the circuit shown. Assume ideal diodes.*

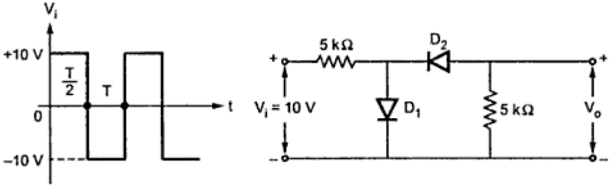

V_i
+10 V
T/2
T
0
t
–10 V
5 kΩ
D₂
+
V_i = 10 V
D₁
5 kΩ
V_o
–

Fig. 1.176

(UPTU, Dec.-2004)

Solution : When $V_i = +10$ V for the period $\left(T/2\right)$ then diode D_1 is forward biased and D_2 is reverse biased. The circuit is as shown in the Fig. 1.176 (a).

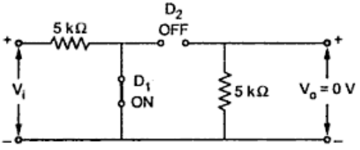

5 kΩ
D₂
OFF
+
V_i
D₁
ON
5 kΩ
V_o = 0 V
–

Fig. 1.176 (a)

Thus no current cam flow through other 5 kΩ resistance as D_2 is open.

$\therefore V_o = $ **0 V** ... $V_i = +10$ V

When $V_i = -10$ V, the diode D_2 is forward biased while the diode D_1 is reverse biased. The circuit is as shown in the Fig. 1.176 (b).

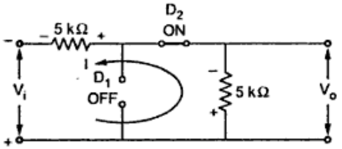

5 kΩ
–
+
D₂
ON
I
D₁
OFF
V_i
5 kΩ
V_o

Fig. 1.176 (b)

Applying KVL to the loop,

$$I = \frac{V_i}{(5+5)\times 10^3} = \frac{10}{10\times 10^3}$$

$$= 1 \text{ mA}$$

$$\therefore \quad V_o = -5\times 10^3 \times I = -5 \text{ V} \qquad \ldots V_i = -10 \text{ V.}$$

Thus the overall output voltage is as shown in the Fig. 1.176 (c).

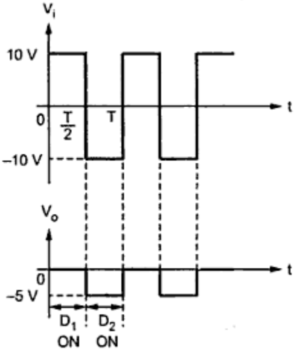


Fig. 1.176(c)

Example 1.33: *Determine the output waveform for the network shown and calculate d.c. output level and PIV of each diode.* **(UPTU, Dec.-2002, May-2005)**

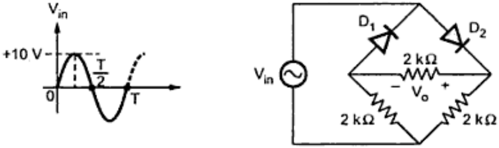

V_{in}
+10 V
$\frac{T}{2}$
0
T
V_{in}
D_1
D_2
2 kΩ
– V_o +
2 kΩ
2 kΩ

Fig. 1.177

Solution : For the positive half cycle, the diode D_2 is forward biased and circuit becomes as shown in the Fig. 1.177(a).

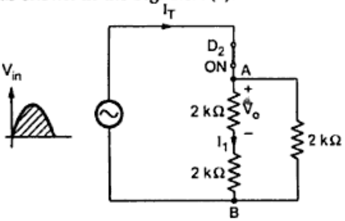

I_T
V_{in}
D_2 ON
A
+
2 kΩ
V_o
–
I_1
2 kΩ
2 kΩ
B

Fig. 1.177 (a)

For $V_{in} = V_m = 10$ V

$$I_T = \frac{V_m}{(4\,k\Omega \| 2\,k\Omega)} = \frac{10}{1333.33}$$

$$= 7.5 \text{ mA}$$

$$\therefore \quad I_1 = I_T \times \frac{2}{(2+4)} = 2.5 \text{ mA}$$

... Current division rule

$$\therefore \qquad V_o = I_1 \times 2\,\text{k}\Omega = \mathbf{5\ V}$$

with A positive

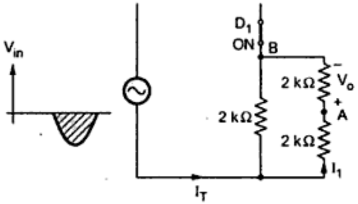


Fig. 1.177 (b)

For the negative half cycle, the diode D_1 is forward biased and circuit becomes as shown in the Fig. 1.177 (b).

Again current through 2 kΩ in branch AB flows from A to B i.e. in the same direction as it flows for positive half cycle. Thus circuit acts as a **full wave rectifier.**

For $\qquad V_{in} = V_m = 10\ \text{V}$

$$I_T = \frac{V_m}{\left(4\,\text{k}\Omega \,\|\, 2\,\text{k}\Omega\right)} = 7.5\ \text{mA}$$

$$I_1 = I_T \times \frac{2}{(2+4)} = 2.5\ \text{mA}$$

$$\therefore \qquad V_0 = I_1 \times 2\ \text{k}\Omega = \mathbf{5\ V}$$

with A positive

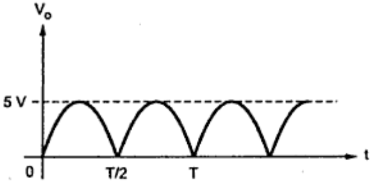


Fig. 1.177 (c)

The output waveform is shown in the Fig. 1.177 (c).

$$V_{DC} = \frac{2V_m}{\pi} = \frac{2\times 5}{\pi}$$

$$= \mathbf{3.183\ V}$$

$$\text{PIV} = V_m$$

$$= \mathbf{5\ V}$$

➡ **Example 1.34 :** *Draw the output waveform for the circuit shown.*

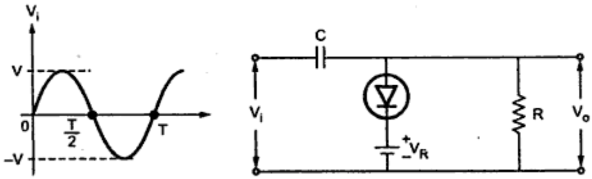


Fig. 1.178

Assume RC ≥ 10 T. **(UPTU, May-2005)**

Solution : Assuming ideal diode, during first quarter of the input cycle, when $V_i > V_R$, the diode is forward biased and C gets charged to $(V - V_R)$ volts as shown in the Fig. 1.178(a).

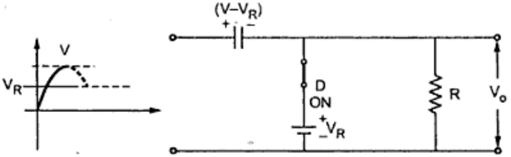


Fig. 1.178 (a)

When V_{in} drops below V, the capacitor remains charged to $(V - V_R)$ with same polarities and diode becomes reverse biased.

$$\therefore \quad V_o = V_i - V_C = V_R \qquad \text{... for } V_i = V$$

$$= -V_C = -(V - V_R) \qquad \text{... for } V_i = 0$$

In the negative half cycle, the capacitor hardly discharges through R as RC >> 10 T. Thus it remains charged at $(V - V_R)$ with same polarities as shown in the Fig. 1.178 (b), for entire negative half cycle.

$$\therefore \quad V_o = -V_i - (V - V_R)$$

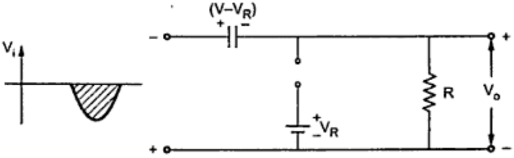


Fig. 1.178 (b)

$$\therefore \quad V_o = -V - V + V_R = -2V + V_R \qquad \text{... for } V_i = -V$$

$$\therefore \quad V_o = -(V - V_R) \qquad \text{... for } V_i = 0$$

Thus the output waveform is as shown in the Fig. 1.178 (c).

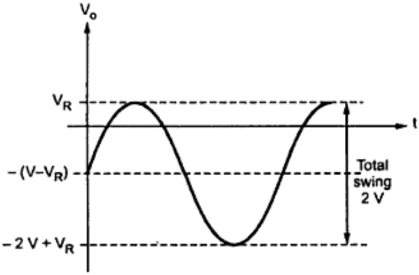


Fig. 1.178 (c)

Example 1.35 : *A 220 V, 50 Hz a.c. voltage is applied to the primary of 4:1 step down transformer which is used in a bridge rectifier, having $R_L = 1\ k\Omega$. Assuming ideal diodes, calculate :*

i) D.C output voltage *ii) D.C. power delivered to load*

iii) PIV of each diode *iv) Output frequency* **(UPTU, May-2006)**

Solution : E_p (rms) = 220 V, $R_L = 1\ k\Omega$

$$\frac{E_p(\text{rms})}{E_s(\text{rms})} = \frac{4}{1} \quad \text{i.e. } E_s(\text{rms}) = \frac{E_p(\text{rms})}{4} = \frac{220}{4} = 55\ V$$

$$\therefore \quad E_{sm} = \sqrt{2} \times E_s(\text{rms}) = 77.7817\ V$$

$$\therefore \quad I_m = \frac{E_{sm}}{R_L} = \frac{77.7817}{1 \times 10^3} = 77.7817\ mA$$

$$\therefore \quad I_{DC} = \frac{2I_m}{\pi} = 49.5174\ mA$$

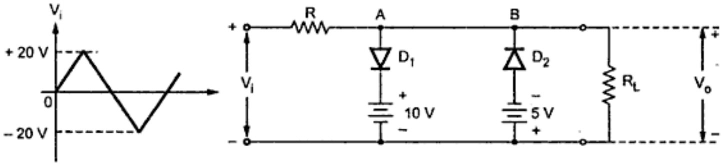
i) $\therefore \quad E_{DC} = I_{DC} R_L = \mathbf{49.5174\ V}$

ii) $P_{DC} = I_{DC}^2 R_L = (49.5174 \times 10^{-3})^2 \times 1 \times 10^3 = \mathbf{2.4519\ W}$

iii) $PIV = E_{sm} = \mathbf{77.7817\ V}$

iv) Output frequency = $2 \times f = 2 \times 50 = \mathbf{100\ Hz}$

Example 1.36 : *Draw the output waveform for the circuit shown.*

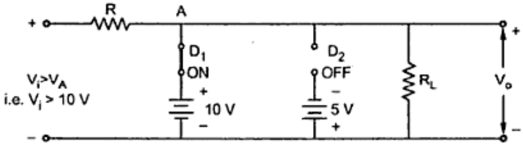


V_i
+ 20 V
0
– 20 V
R
A
B
+
–
V_i
D_1
+
10 V
–
D_2
–
5 V
+
R_L
V_o
+
–

Fig. 1.179

(UPTU, May.-2006)

Solution : When V_i is greater than V_A the diode D_1 conducts while D_2 remains OFF. So circuit reduces as shown in the Fig. 1.179 (a).

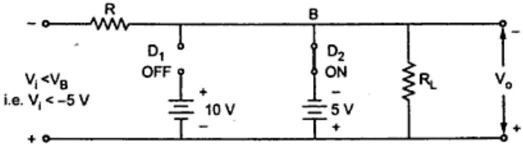


R
A
+
–
D_1
ON
D_2
OFF
V_i>V_A
i.e. V_i > 10 V
+
10 V
–
–
5 V
+
R_L
V_o
+
–

Fig. 1.179(a)

Thus $V_o = V_A = 10$ **V**

When V_i is less than V_B, the diode D_2 conducts while D_1 remains OFF. So circuit reduces as shown in the Fig. 1.179 (b).



R
B
–
+
D_1
OFF
D_2
ON
V_i <V_B
i.e. V_i < –5 V
+
10 V
–
–
5 V
+
R_L
V_o
–
+

Fig. 1.179 (b)

Thus $V_o = V_B = -5$ **V**

While when $V_i < 10$ V and $V_i > -5$ V, the output follows the input as both the diodes remain reverse biased. The input and output waveforms are shown in the Fig. 1.179 (c).

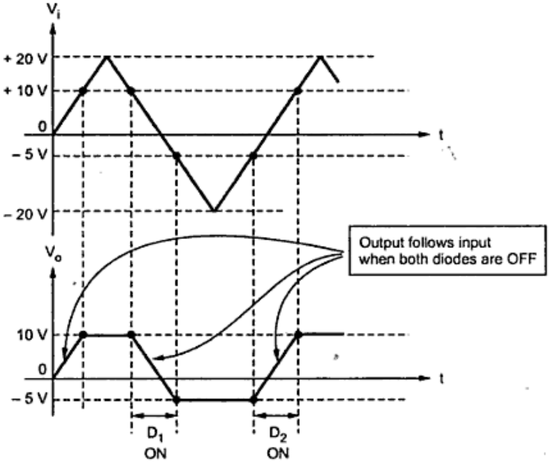


Fig. 1.179(c)

Example 1.37 : *Determine the d.c. resistance level for the diode shown in the following Fig. 1.180 at,*

(i) $I_D = 2\ mA$

(ii) $I_D = 20\ mA$

(iii) $V_D = -10\ V$ **(UPTU, May-2007)**

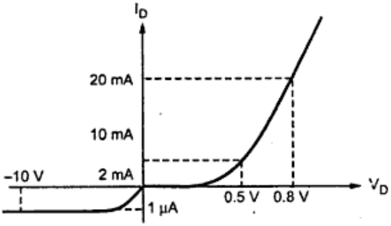


Fig. 1.180

Solution : For a diode,

$$\text{D.C. resistance} = \left.\frac{\text{Diode voltage}}{\text{Diode current}}\right|_{\text{At a point}}$$

(i) For $I_D = 2$ mA, $V_D = 0.5$ V from graph

$$\therefore \quad R = \frac{V_D}{I_D} = \frac{0.5}{2\times10^{-3}} = \mathbf{250\ \Omega}$$

(ii) For $I_D = 20$ mA, $V_D = 0.8$ V from graph

$$\therefore \quad R = \frac{0.8}{20\times10^{-3}} = \mathbf{40\ \Omega}$$

(ii) For $V_D = -10$ V, $I_D = -1$ μA from graph

$$\therefore \quad R = \frac{-10}{-1\times10^{-6}} = \mathbf{10\ M\Omega}$$

Example 1.38 : *Determine I, V_1, V_2 and V_o for the series d.c. configuration of the following Fig. 1.181.* **(UPTU, May-2007)**

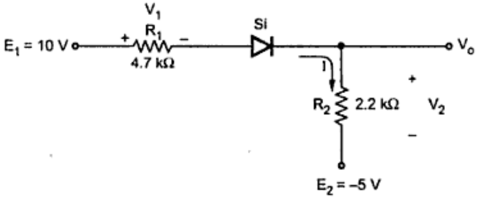

V1
R1
+
–
E1 = 10 V
4.7 kΩ
Si
Vo
I
+
R2
2.2 kΩ
V2
–
E2 = –5 V

Fig. 1.181

Solution : Assume ideal diode hence in forward biased condition, it acts as a closed switch.

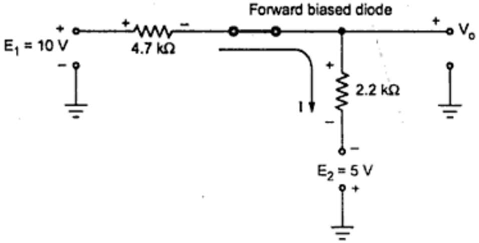

Forward biased diode
+
E1 = 10 V
–
+
–
4.7 kΩ
+
Vo
I
+
2.2 kΩ
–
–
E2 = 5 V
+

Fig. 1.182

Applying KVL to the loop,

$$-4.7\times10^{3}I-2.2\times10^{3}I+5+10 = 0$$

$$\therefore \quad I = \frac{15}{6.9\times10^{3}} = \mathbf{2.1739\ mA}$$

$$\therefore \quad V_1 = IR_1 = 2.1739\times10^{-3}\times4.7\times10^{+3} = \mathbf{10.2173\ V}$$

$$\therefore \quad V_2 = IR_2 = 2.1739\times10^{-3}\times2.2\times10^{+3} = \mathbf{4.7825\ V}$$

$$\therefore \quad V_o = V_2 - E_2 = 4.7825 - 5 = \mathbf{-0.2174\ V}$$

Example 1.39 : *Sketch V_o for network in the Fig. 1.183.* **(UPTU, May-2007)**

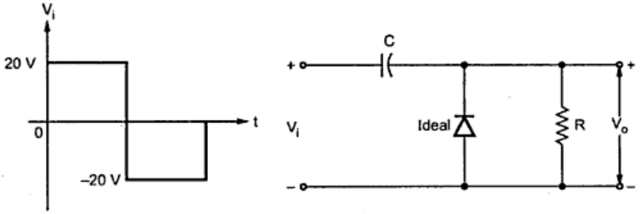


Fig. 1.183

Solution : During the negative half cycle, the diode will be forward biased as shown in the Fig. 1.184.

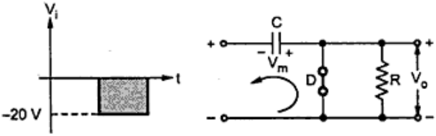


Fig. 1.184

The capacitor gets charged to V_m = 20 V with the polarities as shown.

$$V_o = -V_i + V_m$$

$$= -20 + 20 = 0\ V$$

Thus during negative half cycle, V_o = 0 V.

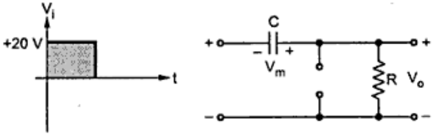


Fig. 1.185

In the positive half cycle, the diode is reverse biased and acts as an open switch as shown in the Fig. 1.185 The capacitors tries to discharge through R but due to large time constant it hardly discharges and retains its full charge during positive half cycle. Hence voltage across C remains same as $V_m = 20$ V.

$$\therefore \quad V_o = V_i + V_m = 20 + 20 = 40 \text{ V}$$

Thus during positive half cycle, $V_o = 40$ V.

Hence the waveforms are as shown in the Fig. 1.186.

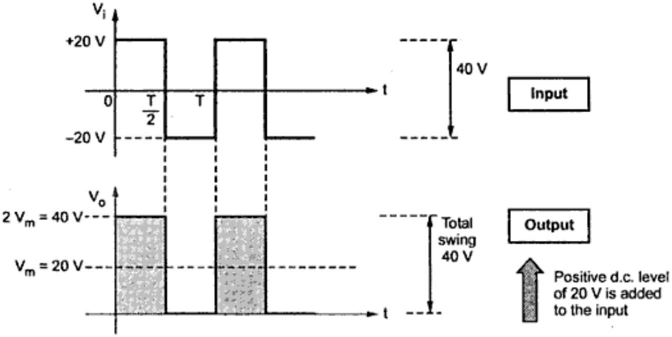


Fig. 1.186

Example 1.40 : *Sketch the output waveform.* **(UPTU, May-20007)**

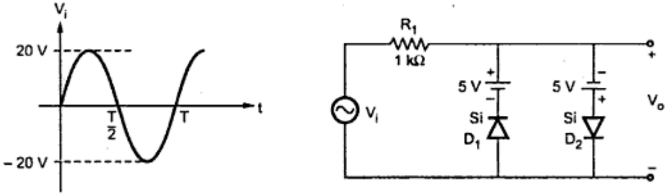
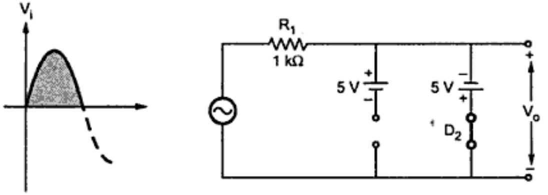


Fig. 1.187

Solution : Assume that the diodes are ideal.

Positive half cycle of input

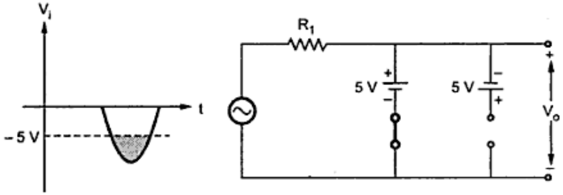
The diode D_2 is forward biased for the entire positive half cycle and circuit reduces as shown in the Fig. 1.188, with diode D_1 is reverse biased.



Thus $V_o = -5$ V for the entire positive half cycle of the input.

Fig. 1.188

Negative half cycle of input : As long as magnitude of V_i is less than 5 V, the diode D_1 is still reverse biased and the diode D_2 forward biased. Thus $V_o = -5$ V. When V_i becomes less than -5 V, then the diode D_1 becomes forward biased and the diode D_2 becomes reverse biased. Thus the circuit becomes as shown in the Fig. 1.189.



Thus the output voltage is,
$V_o = +5$ V

Fig. 1.189

The waveforms are shown in the Fig. 1.190.

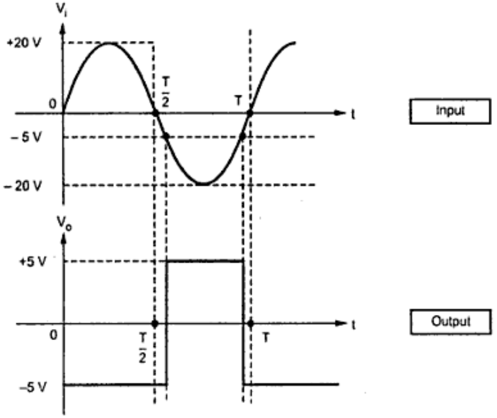


Fig. 1.190

Review Questions

1. *Explain the behaviour of unbiased p-n junction.*
2. *What is depletion layer and junction potential in an unbiased p-n junction ?*
3. *Explain the behaviour of forward biased diode.*
4. *Draw and explain the forward characteristics of a diode.*
5. *Explain the behaviour of reverse biased diode.*
6. *Draw and explain the reverse characteristics of a diode.*
7. *What is reverse breakdown ? Explain the two breakdown mechanisms in a diode.*
8. *Describe the two different break-down mechanisms in a diode.*
9. *Write the diode equation and explain the significance of various terms.*
10. *Write the diode current equation and explain the V-I characteristics from it.*
11. *Draw the V-I characteristics of Ge and Si diodes. Give reasons for variations in the characteristics, if any.*
12. *Explain the effect of termperature on a p-n juntion diode.*
13. *Explain the V-I characteristics of a diode.*
14. *Define forward static and dynamic resistances of diode.*
15. *The current of germanium diode is 100 μA at a voltage of – 1V, at room temperature. Determine the magnitude of the current for the voltages of ± 0.2 V at room temperature.*
    (Ans. : 291 mA, 99.95 μA)
16. *A silicon diode has a reverse saturation current of 60 nA. Calculate the voltage at which 1% of the rated current will flow through the diode, at room temperature if diode is rated for 1A.*
    (Ans. : 0.6252 V)
17. *How does the reverse saturation current of diode varies with temperature? Explain.*
18. *For a germanium diode carrying 10 mA the required forward bias is about 0.2 V. Estimate the reverse saturation current and the bias voltage required for currents of 1 mA and 100 mA.*
    (Ans. : 4.56 μA, 0.14 V, 0.26 V)
19. *Give the relation between voltage and current for a p-n junction diode.*
20. *Derive the expression for the dynamic resistance of a diode.*
21. *For a silicon diode with reverse saturation current of 0.2 μA, calculate the dynamic forward and reverse resistance at a voltage of 0.72 V and – 0.72 V respectively, applied across the diode, at room temperature of 27 °C.* **(Ans. : 0.252 Ω, 2680.9 G Ω)**
22. *Write in detail about the two types of capacitances associated with a diode.*
23. *What is practical significance of a transition capacitance ? Explain.*
24. *What is diffusion capacitance ? State its practical significance.*
25. *What is rectifier ?*
26. *Which are the important characteristics of a rectifier circuit ?*
27. *Explain why diode can be used as a rectifier ?*
28. *Draw the circuit diagram of half wave rectifier and explain its operation with the help of waveforms.*

29. *Derive the expressions for the following parameters of the half wave rectifier circuit :*

    a. Average d.c. current (I_{DC}) *b. Average d.c. voltage* (E_{DC})

    c. R.M.S. value of current (I_{RMS}) *d. D.C. power output* (P_{DC})

    e. A.C. power input (P_{AC}) *f. Rectifier efficiency* (η)

    g. Ripple factor (γ)

30. *What is ripple factor ? What is the requirement of a rectifier in terms of ripple factor ? How is it achieved ?*

31. *A half wave rectifier circuit feeds a resistive load of 10 kΩ through a power transformer having a step-down turns ratio of 8 : 1 and operated from 230 V, 50 Hz A.C. mains supply. Assume the forward resistance of diode to be 40 Ω and transformer secondary winding resistance as 12 Ω. Calculate the maximum, RMS, and average values of current, DC output voltage and power, efficiency of rectification, and ripple factor.*

    (Ans. : I_m = 4.045 mA, I_{rms} = 2.024 mA, I_{DC} = 1.2875 mA,)
    E_{DC} = 12.875 V, P_{DC} = 16.58 mW, P_{AC} = 41.179 mW,
    Rectifier efficiency = 40.26 %, Ripple factor = 1.21)

32. *Prove that the voltage regulation for a half wave rectifier is* $[(R_s + R_f)/R_L] \times 100$.

33. *Derive the expressions for the following parameters of the full wave rectifier.*

    a) Average d.c. current (I_{DC}) *b) Average d.c. output voltage* (E_{DC})

    c) R.M.S. value of current (I_{RMS}) *d) D.C. power output* (P_{DC})

    e) A.C. power input (P_{AC}) *f) Rectifier efficiency* (η)

34. *Prove that the ripple factor for the full-wave rectifier circuit is 0.48.*

35. *Compare the full wave rectifier with half-wave rectifier circuit.*

36. *Define ripple factor and rectifier efficiency. State their values for full-wave rectifier circuit.*

37. *A full-wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from either end of secondary to center tap is 20 V. If the diode forward resistance is 3 Ω and that of the half secondary is 5 Ω, for a load of 1 kΩ, calculate*

    a) Power delivered to load, *b) % Regulation at full load,*

    c) Efficiency at full load, *d) T.U.F. of secondary.*

    (Ans. : 1) P_{dc} = 0.3191 W, b) % Regulation = 0.7469 %,
    c) Efficiency of full load = 0.8041, d) T.U.F. = 0.804)

38. *Draw a full wave rectifier circuit with centre-tapped transformer. Explain its working with waveforms across secondary winding, diodes and load.*

39. *Define the terms rectification efficiency and peak inverse voltage. State standard values of rectification efficiency for a half-wave and a full wave rectifier.*

40. *Give four advantages that a full wave rectifier has over a half wave rectifier .*

41. *Which are different full wave rectifiers used in electronic circuits ? With diagrams explain working and compare the parameters measured.*

42. *Draw the circuit diagram of bridge rectifier.*

43. *Describe its operation.*

44. *How will you use 'ON'/OFF indicator for the bridge rectifier circuit ?*

Solution : The 'ON/OFF' indicator is required to indicate whether the bridge rectifier is working or not and d.c. output voltage is available or not. For this, LED with a current limiting high resistance in series with it, is connected across the load resistance. Hence when bridge rectifier is working, LED will be ON inspite of whether load is present or not. The OFF LED indicates that bridge rectifier is not working and d.c. output voltage is not available.

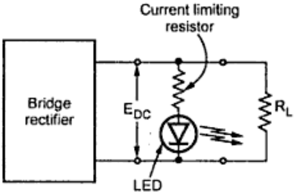


Fig. 1.191

45. *Draw the circuit diagram of capacitor filter used in rectifier and explain its operation.*

46. *Draw the circuit diagram of bridge rectifier with capacitor filter and explain its operation with relevant waveforms.*

47. *Justify the statement.*

    'The capacitor filter provides poor voltage regulation.'

48. *Explain the operation of capacitor filter with the help of waveforms.*

49. *Explain the various circuit models of a diode.*

50. *Explain the basic series clipper circuit.*

51. *Explain the basic series clipper above reference voltage.*

52. *Explain the basic series clipper below reference voltage.*

53. *Explain the basic parallel clipper circuit.*

54. *Explain the clipping above and below the reference voltage in a basic parallel clipper.*

55. *Explain the two way parallel clipper circuit.*

56. *Explain the negative clamper circuit.*

57. *Explain the positive clamper circuit.*

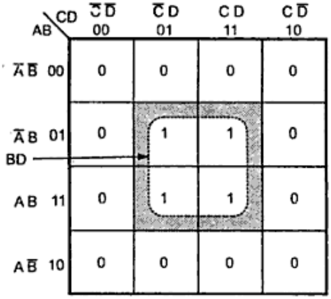
58. *Explain one application of clamper.*

59. *Explain with neat circuit diagram the operation of the following circuits*

    i) Half wave voltage doubler, *ii) Full wave voltage doubler,*

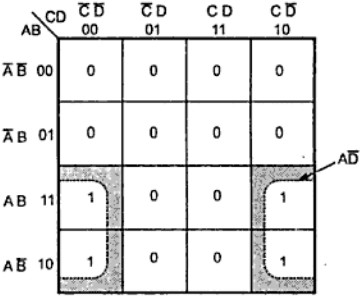
    iii) Voltage tripler, *iv) Voltage quadrupler.*

❑❑❑



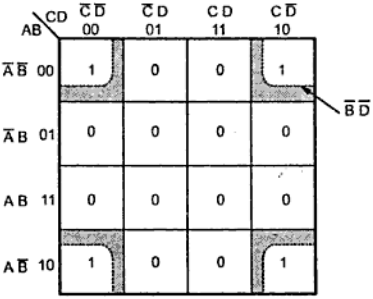
AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0	0	0	0
$\bar{A}B$ 01	0	1	1	0
AB 11	0	1	1	0
$A\bar{B}$ 10	0	0	0	0

Fig. 7.47 (c) $Y = BD$



AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0	0	0	0
$\bar{A}B$ 01	0	0	0	0
AB 11	1	0	0	1
$A\bar{B}$ 10	1	0	0	1

Fig. 7.47 (d) $Y = A\bar{D}$



AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1	0	0	1
$\bar{A}B$ 01	0	0	0	0
AB 11	0	0	0	0
$A\bar{B}$ 10	1	0	0	1

Fig. 7.47 (e) $Y = \bar{B}\bar{D}$

From the above Karnaugh maps we can easily notice that when a quad is combined two variables are eliminated. For example, in Fig. 7.47 (c) we have following terms with 4 variables :

$$
\begin{aligned}
Y &= \bar{A}B\bar{C}D + \bar{A}BCD + AB\bar{C}D + ABCD \\
&= \bar{A}BD(\bar{C} + C) + ABD(\bar{C} + C) \\
&= \bar{A}BD + ABD \\
&= BD(\bar{A} + A) \\
&= BD
\end{aligned}
$$

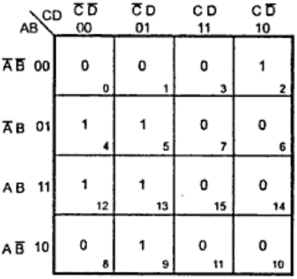
(only two variables in the result, variables A and C are eliminated)

Example 7.76 : *Minimize the expression*

$$Y = \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + AB\overline{C}\overline{D} + AB\overline{C}D + A\overline{B}\overline{C}D + \overline{A}\,\overline{B}\,C\overline{D}.$$

Solution :

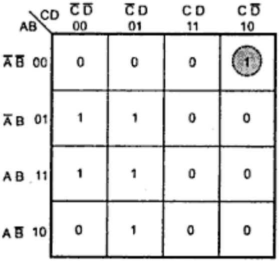
Step 1 : Fig. 7.50 (a) shows the K-map for four variables and it is plotted according to the given expression.



AB \ CD	$\overline{C}\overline{D}$ 00	$\overline{C}D$ 01	CD 11	$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00	0 0	0 1	0 3	1 2
$\overline{A}B$ 01	1 4	1 5	0 7	0 6
AB 11	1 12	1 13	0 15	0 14
$A\overline{B}$ 10	0 8	1 9	0 11	0 10

Fig. 7.50 (a)

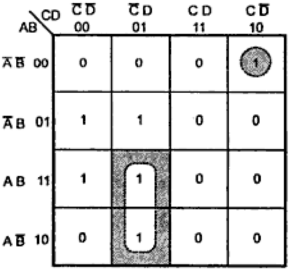
Step 2 : Cell 2 is the only cell containing a 1 that is not adjacent to any other 1. It is referred to separately as group 1.



AB \ CD	$\overline{C}\overline{D}$ 00	$\overline{C}D$ 01	CD 11	$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00	0	0	0	1
$\overline{A}B$ 01	1	1	0	0
AB 11	1	1	0	0
$A\overline{B}$ 10	0	1	0	0

Fig. 7.50 (b)

Step 3 : 1 in the cell 9 is adjacent only to 1 in the cell 13. This pair is combined and referred to as group 2.



AB \ CD	$\overline{C}\overline{D}$ 00	$\overline{C}D$ 01	CD 11	$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00	0	0	0	1
$\overline{A}B$ 01	1	1	0	0
AB 11	1	1	0	0
$A\overline{B}$ 10	0	1	0	0

Fig. 7.50 (c)

Step 4 : There is no octet, but there is quad cells 4, 5, 12 and 13 form a quad. This quad is combined and referred to as group 3.

Step 5 : All 1s have already grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1 variable is not eliminated. In group 2 variable B is eliminated and in group 3 variables A and D are eliminated and we get,

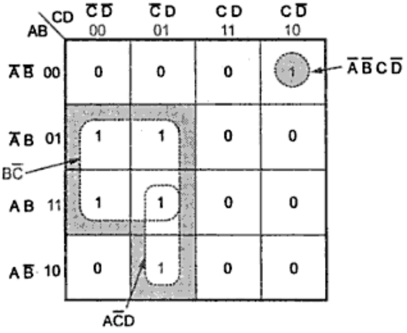

CD
AB
$\bar{C}\bar{D}$ 00
$\bar{C}D$ 01
CD 11
$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00
$\bar{A}B$ 01
AB 11
$A\bar{B}$ 10
0
0
0
1
1
1
0
0
1
1
0
0
0
1
0
0
$\bar{A}\bar{B}C\bar{D}$
$B\bar{C}$
$A\bar{C}D$

Fig. 7.50 (d)

$$Y = \bar{A}\bar{B}C\bar{D} + A\bar{C}D + B\bar{C}$$

Example 7.77 : *Reduce the following four variable function to its minimum sum of products form :*

$$Y = \bar{A}\bar{B}C\bar{D} + ABC\bar{D} + A\bar{B}C\bar{D} + A\bar{B}CD + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}\bar{D}.$$

Solution :

Step 1 : Fig. 7.51 (a) shows the K-map for four variables and it is plotted according to the given expression.

Step 2 : There are no isolated 1s.

Step 3 : There are no such 1s which are adjacent to only one other 1.

Step 4 : There are three quads formed by cells 0, 2, 8, 10, cells 8, 10,

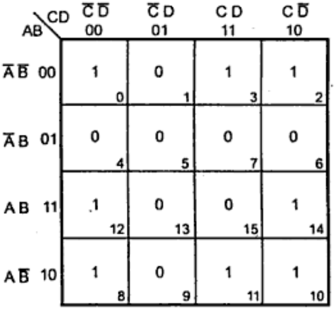

CD
AB
$\bar{C}\bar{D}$ 00
$\bar{C}D$ 01
CD 11
$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00
$\bar{A}B$ 01
AB 11
$A\bar{B}$ 10
1 0
0 1
1 3
1 2
0 4
0 5
0 7
0 6
1 12
0 13
0 15
1 14
1 8
0 9
1 11
1 10

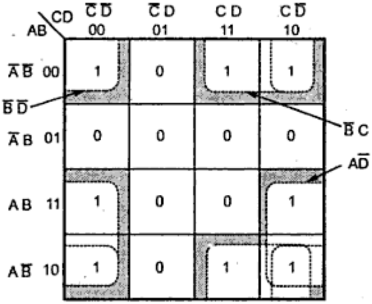
Fig. 7.51 (a)

12, 14 and cells 2, 3, 10, 11. These quads are combined and referred to as group 1, group 2 and group 3 respectively.

Step 5 : All 1s have already been grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1 variables A and C are eliminated, in group 2 variables B and C are eliminated and in group 3 variables A and D are eliminated and we get

$$Y = \bar{B}\,\bar{D} + A\bar{D} + \bar{B}C$$



AB \ CD	$\bar{C}\,\bar{D}$ 00	$\bar{C}\,D$ 01	$C\,D$ 11	$C\,\bar{D}$ 10
$\bar{A}\,\bar{B}$ 00	1	0	1	1
$\bar{A}\,B$ 01	0	0	0	0
$A\,B$ 11	1	0	0	1
$A\,\bar{B}$ 10	1	0	1	1

Fig. 7.51 (b)

Example 7.78 : *Reduce the following function to its minimum sum of products form :*

$$Y = \bar{A}\,\bar{B}\,\bar{C}D + \bar{A}B\bar{C}D + \bar{A}BCD + \bar{A}BC\bar{D} + AB\bar{C}\,\bar{D} + AB\bar{C}D + ABCD + A\bar{B}\,CD.$$

Solution :

Step 1 : Fig. 7.52 (a) shows the K-map for four variables and it is plotted according to the given expression.

Step 2 : There are no isolated 1s.

AB \ CD	$\bar{C}\,\bar{D}$ 00	$\bar{C}\,D$ 01	$C\,D$ 11	$C\,\bar{D}$ 10
$\bar{A}\,\bar{B}$ 00	0 0	1 1	0 3	0 2
$\bar{A}\,B$ 01	0 4	1 5	1 7	1 6
$A\,B$ 11	1 12	1 13	1 15	0 14
$A\,\bar{B}$ 10	0 8	0 9	1 11	0 10

Fig. 7.52 (a)

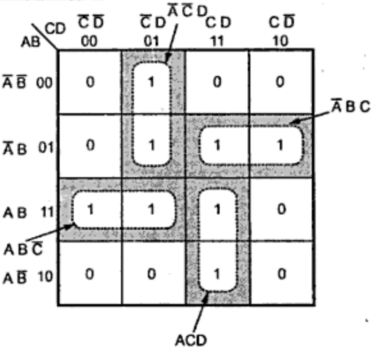

$\bar{A}\bar{C}D$
CD
AB
$\bar{C}\bar{D}$ 00
$\bar{C}D$ 01
CD 11
$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00
$\bar{A}B$ 01
AB 11
$A\bar{B}$ 10
0 1 0 0
0 1 1 1
1 1 1 0
0 0 1 0
$\bar{A}BC$
$AB\bar{C}$
ACD

Fig. 7.52 (b)

Step 3 : The 1 in the cell 1 is adjacent only to 1 in the cell 5, the 1 in the cell 6 is adjacent only to the 1 in the cell 7, the 1 in the cell 12 is adjacent only to the 1 in the cell 13 and the 1 in the cell 11 is adjacent only to the 1 in the cell 15. These pairs are combined and referred to as group 1-4 respectively.

Step 4 : There is no octet, but there is a quad. However, all 1s in the quad have already been grouped. Therefore this quad is ignored.

Step 5 : All 1s have already been grouped.

Step 6 : Each group generates a term in the expression for Y. In group 1 variable B is eliminated. Similarly, in group 2-4 variables D, D and B are eliminated one in each group. We finally get minimum sum of products form as

$$Y = \bar{A}\bar{C}D + \bar{A}BC + AB\bar{C} + ACD$$

➡ Example 7.79 : *Simplify the logic function specified by the truth table 7.40 using the Karnaugh map method. Y is the output variable, and A, B, and C are the input variables.*

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 7.40

Solution :

Step 1 : Fig. 7.53 (a) shows the K-map for three variables and it is plotted according to given truth table.

Step 2 : There are no isolated 1s.

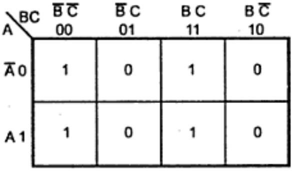

BC
A
$\bar{B}\bar{C}$
00
$\bar{B}C$
01
BC
11
$B\bar{C}$
10
$\bar{A}$ 0
A 1
1
0
1
0
1
0
1
0

Fig. 7.53 (a)

Step 3 : The 1 in the cell 0 is adjacent only to 1 in the cell 4 and the 1 in the cell 3 is adjacent only to 1 in the cell 7. These two pairs are grouped and referred to as group 1 and group 2.

Step 4 : There is no octet and quad.

Step 5 : All 1s have already been grouped.

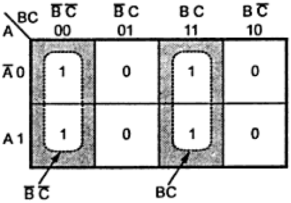

BC
A
$\bar{B}\bar{C}$
00
$\bar{B}C$
01
BC
11
$B\bar{C}$
10
$\bar{A}$ 0
A 1
1
0
1
0
1
0
1
0
$\bar{B}\bar{C}$
BC

Fig. 7.53 (b)

Step 6 : In group 1 and group 2 variable A is eliminated and we get.

$$Y = \bar{B}\,\bar{C} + BC$$

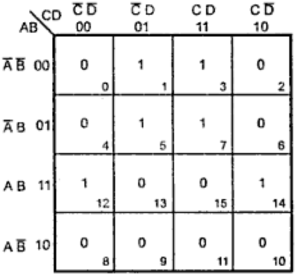
Example 7.80 : *Reduce the following function using Karnaugh map technique and implement using basic gates*

$$f(A, B, C, D) = \bar{A}\bar{B}D + AB\bar{C}\bar{D} + \bar{A}BD + ABC\bar{D}.$$

Solution : The given function is not in the standard sum of products form. It is converted into standard SOP form as given below.

$$\begin{aligned} f(A, B, C, D) &= \bar{A}\bar{B}D + AB\bar{C}\bar{D} + \bar{A}BD + ABC\bar{D} \\ &= \bar{A}\bar{B}D(C+\bar{C}) + AB\bar{C}\bar{D} + \bar{A}BD(C+\bar{C}) + ABC\bar{D} \\ &= \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D + AB\bar{C}\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + ABC\bar{D} \end{aligned}$$

Step 1 : Fig. 7.54 (a) shows the K-map for four variables and it is plotted according to expression in standard SOP form.

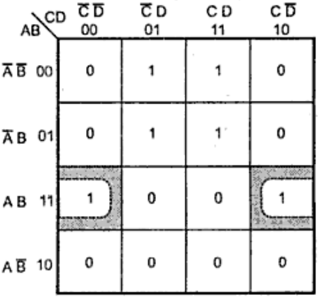


AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0 0	1 1	1 3	0 2
$\bar{A}B$ 01	0 4	1 5	1 7	0 6
AB 11	1 12	0 13	0 15	1 14
$A\bar{B}$ 10	0 8	0 9	0 11	0 10

Fig. 7.54 (a)

Step 2 : There are no isolated 1s.

Step 3 : The 1 in the cell 12 is adjacent only to the 1 in the cell 14. This pair is combined and referred to as group 1.



AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0	1	1	0
$\bar{A}B$ 01	0	1	1	0
AB 11	1	0	0	1
$A\bar{B}$ 10	0	0	0	0

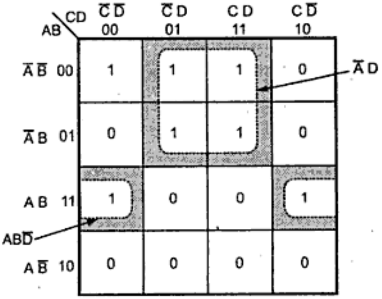
Fig. 7.54 (b)

Step 4 : There is a quad. Cells 1, 3, 5 and 7 form a quad. This quad is referred to as group 2.

Step 5 : All 1s have already been grouped.

Step 6 : In group 1 variable C is eliminated and in group 2 variables B and C are eliminated. We get simplified equation as

$$Y = AB\bar{D} + \bar{A}D$$



AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1	1	1	0
$\bar{A}B$ 01	0	1	1	0
AB 11	1	0	0	1
$A\bar{B}$ 10	0	0	0	0

Fig. 7.54 (c)

7.17.5 Essential Prime Implicants

After grouping the cells, the sum terms which appear in the K-map are called prime implicant groups. It is observed that some cells may appear in only one prime implicant group; while other cells may appear in more than one prime implicant group. In Fig. 7.55 (c), cells 1, 4, 9 and 10 appear in only one prime implicant group. These cells are called **essential cells** and corresponding prime implicants are called **essential prime implicants.**

7.17.6 Simplification of Product of Sums Expressions (Minimal Products)

In the above discussion, we have considered the Boolean expression in sum of products form and grouped 2, 4, and 8 adjacent ones to get the simplified Boolean expression in the same form. In practice, the designer should examine both the sum of products and product of sums reductions to ascertain which is more simplified. We have already seen the representation of product of sums on the Karnaugh map. Once the expression is plotted on the K-map instead of making the groups of ones, we have to make groups of zeros. Each group of zero results a sum term and it is nothing but the **prime implicate**. The technique for using maps for POS reductions is a simple step by step process and it is similar to the one used earlier.

1. Plot the K-map and place 0s in those cells corresponding to the 0s in the truth table or maxterms in the products of sum expression.
2. Check the K-map for adjacent 0s and encircle those 0s which are not adjacent to any other 0s. These are called isolated 0s.
3. Check for those 0s which are adjacent to only one other 0 and encircle such pairs.
4. Check for quads and octets of adjacent 0s even if it contains some 0s that have already been encircled. While doing this make sure that there are minimum number of groups.
5. Combine any pairs necessary to include any 0s that have not yet been grouped.
6. Form the simplified SOP expression for $\bar{F}$ by summing product terms of all the groups.

(Note : The simplified expression is in the complemented form because we have grouped 0s to simplify the expression.)

7. Use DeMorgan's theorem on $\bar{F}$ to produce the simplified expression in POS form.

To get familiar with these steps we will solve some examples.

➠ **Example 7.82 :** *Minimize the expression*

$$Y = (A + B + \bar{C})(A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + \bar{C})(\bar{A} + B + C)(A + B + C)$$

Solution : $(A + B + \bar{C}) = M_1$, $(A + \bar{B} + \bar{C}) = M_3$, $(\bar{A} + \bar{B} + \bar{C}) = M_7$,

$(\bar{A} + B + C) = M_4$, $(A + B + C) = M_0$

Step 1 : Fig. 7.56 (a) shows the K-map for three variable and it is plotted according to given maxterms.

Step 2 : There are no isolated 0s.

Step 3 : 0 in the cell 4 is adjacent only to 0 in the cell 0 and 0 in the cell 7 is adjacent only to 0 in the cell 3. These two pairs are combined and referred to as group 1 and group 2 respectively.

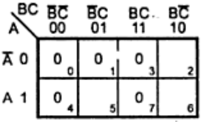


Fig. 7.56 (a)

Step 4 : There are no quads and octets.

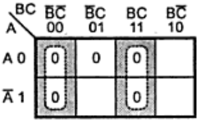


Fig. 7.56 (b)

Step 5 : The 0 in the cell 1 can be combined with 0 in the cell 3 to form a pair. This pair is referred to as group 3.

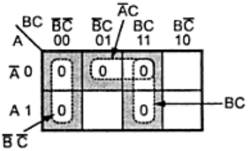


Fig. 7.56 (c)

Step 6 : In group 1 and in group 2, A is eliminated, where as in group 3 variable B is eliminated and we get

$$\overline{Y} = \overline{B}\,\overline{C} + BC + \overline{A}C$$

Step 7 :

$$Y = \overline{\overline{Y}} = \overline{\overline{B}\,\overline{C} + BC + \overline{A}C}$$

$$= \left(\overline{\overline{B}\,\overline{C}}\right)\left(\overline{BC}\right)\left(\overline{\overline{A}C}\right)$$

$$= \left(\overline{\overline{B}} + \overline{\overline{C}}\right)\ \left(\overline{B} + \overline{C}\right)\left(\overline{\overline{A}} + \overline{C}\right)$$

$$= (B + C)\ \left(\overline{B} + \overline{C}\right)\ \left(A + \overline{C}\right)$$

It is possible to directly write the expression for Y by using DeMorgans theorem for each minterm as follows :

$$\overline{Y} = \overline{B}\,\overline{C} + BC + \overline{A}C \rightarrow Y = (B + C)\left(\overline{B} + \overline{C}\right)\left(A + \overline{C}\right)$$

Example 7.83 : *Minimize the following expression in the POS form*

$$Y = (\overline{A} + \overline{B} + C + D)(\overline{A} + \overline{B} + \overline{C} + D)(\overline{A} + \overline{B} + \overline{C} + \overline{D})$$
$$(\overline{A} + B + C + D)(A + \overline{B} + \overline{C} + D)(A + \overline{B} + \overline{C} + \overline{D})(A + B + C + D)$$
$$(\overline{A} + \overline{B} + C + \overline{D})$$

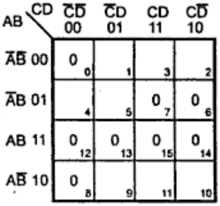
Solution :

$$(\overline{A} + \overline{B} + C + D) = M_{12},\ (\overline{A} + \overline{B} + \overline{C} + D) = M_{14},\ (\overline{A} + \overline{B} + \overline{C} + \overline{D}) = M_{15}$$

$$(\overline{A} + B + C + D) = M_8,\ (A + \overline{B} + \overline{C} + D) = M_6,\ (A + \overline{B} + \overline{C} + \overline{D}) = M_7$$

$$(A + B + C + D) = M_0 \text{ and } (\overline{A} + \overline{B} + C + \overline{D}) = M_{13}$$

Step 1 : Fig. 7.57 (a) shows the K-map for four variable and it is plotted according to given maxterms.

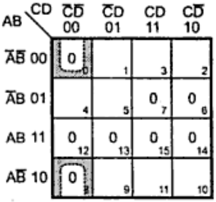


AB
CD
$\overline{C}\overline{D}$ 00
$\overline{C}D$ 01
CD 11
$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00
$\overline{A}B$ 01
AB 11
$A\overline{B}$ 10
0 0
1
3
2
4
5
0 7
0 6
0 12
0 13
0 15
0 14
0 8
9
11
10

Fig. 7.57 (a)

Step 2 : There are no isolated 0s.

Step 3 : 0 in the cell 0 is adjacent only to 0 in the cell 8. This pair is combined and referred to as group 1.

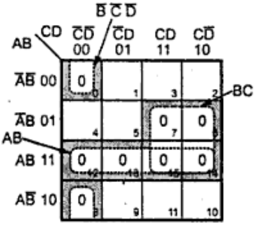


AB
CD
$\overline{C}\overline{D}$ 00
$\overline{C}D$ 01
CD 11
$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00
$\overline{A}B$ 01
AB 11
$A\overline{B}$ 10
0 0
1
3
2
4
5
0 7
0 6
0 12
0 13
0 15
0 14
0 8
9
11
10

Fig. 7.57 (b)

Step 4 : There are two quads. Cells 12, 13, 14 and 15 forms a quad 1 and cells 6, 7, 14, 15 forms a quad 2. These two quads are referred to as group 2 and group 3, respectively.

Step 5 : All 0s have already been grouped.



$\overline{B}\,\overline{C}\,\overline{D}$
AB
CD
$\overline{C}\overline{D}$ 00
$\overline{C}D$ 01
CD 11
$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00
$\overline{A}B$ 01
AB 11
$A\overline{B}$ 10
BC
AB
0 0
1
3
2
4
5
0 7
0 6
0 12
0 13
0 15
0 14
0 8
9
11
10

Fig. 7.57 (c)

Step 6 : In group 1, variable A is eliminated. In group 2, variable C and D are eliminated and in group 3 variables A and D are eliminated. Therefore we get simplified SOP expression as

$$\overline{Y} = \overline{B}\,\overline{C}\,\overline{D} + AB + BC$$

Step 7 :

$$Y = \overline{\overline{Y}} = \overline{\overline{B}\overline{C}\overline{D} + AB + BC}$$

$$= (\overline{\overline{B}\,\overline{C}\,\overline{D}})\,(\overline{AB})\,(\overline{BC})$$

$$= (\overline{\overline{B}} + \overline{\overline{C}} + \overline{\overline{D}})\ (\overline{A} + \overline{B})\,(\overline{B} + \overline{C})$$

$$= (B + C + D)\,(\overline{A} + \overline{B})\,(\overline{B} + \overline{C})$$

It is possible to directly write the expression for Y by using DeMorgans theorem for each minterm as follows :

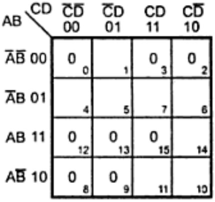
$$Y = \overline{B}\,\overline{C}\,\overline{D} + AB + BC \rightarrow Y = (B + C + D)\,(\overline{A} + \overline{B})\,(\overline{B} + \overline{C})$$

Example 7.84 : *Reduce the following function using K-map technique*

$$f(A, B, C, D) = \pi M(0, 2, 3, 8, 9, 12, 13, 15).$$

Solution :

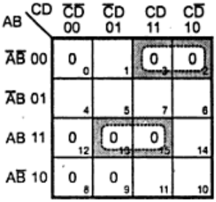
Step 1 : Fig. 7.58 (a) shows the K-map for four variables and it is plotted according to given maxterms.



AB \ CD	$\overline{C}\overline{D}$ 00	$\overline{C}D$ 01	CD 11	$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00	0 0	1	0 3	0 2
$\overline{A}B$ 01	4	5	7	6
AB 11	0 12	0 13	0 15	14
$A\overline{B}$ 10	0 8	0 9	11	10

Fig. 7.58 (a)

Step 2 : There are no isolated 0s.



AB \ CD	$\overline{C}\overline{D}$ 00	$\overline{C}D$ 01	CD 11	$C\overline{D}$ 10
$\overline{A}\overline{B}$ 00	0 0	1	0 3	0 2
$\overline{A}B$ 01	4	5	7	6
AB 11	0 12	0 13	0 15	14
$A\overline{B}$ 10	0 8	0 9	11	10

Fig. 7.58 (b)

Step 3 : The 0 in the cell 15 is adjacent only to 0 in the cell 13 and 0 in the cell 3 is adjacent only to 0 in the cell 7. These two pairs are combined and referred to as group 1 and group 2, respectively.

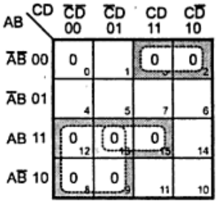

AB
CD
$\bar{C}\bar{D}$ 00
$\bar{C}D$ 01
CD 11
$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00
$\bar{A}B$ 01
AB 11
$A\bar{B}$ 10
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Fig. 7.58 (c)

Step 4 : The cells 8, 9, 12 and 13 form a quad which is referred to as group 3.

Step 5 : The remaining 0 in the cell 0 is combined with the 0 in the cell 2 to form a pair, which is referred to as group 4.

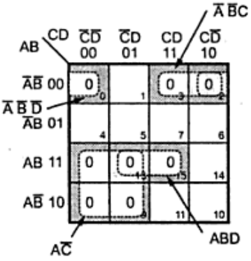

$\bar{A}\bar{B}C$
AB
CD
$\bar{C}\bar{D}$ 00
$\bar{C}D$ 01
CD 11
$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00
$\bar{A}\bar{B}\bar{D}$
$\bar{A}B$ 01
AB 11
$A\bar{B}$ 10
$A\bar{C}$
ABD

Fig. 7.58 (d)

Step 6 : In group 1 and in group 4 variable C is eliminated. In group 2 variable D is eliminated and in group 3 variables B and D are eliminated. Therefore, we get simplified expression in SOP form as

$$\bar{f} = A B D + \bar{A} \bar{B} C + A \bar{C} + \bar{A} \bar{B} \bar{D}$$

Step 7 :

$$f = \bar{\bar{f}} = \overline{ABD + \bar{A} \bar{B} C + A \bar{C} + \bar{A} \bar{B} \bar{D}}$$

$$= \left(\overline{ABD}\right)\left(\overline{\bar{A} \bar{B} C}\right)\left(\overline{A \bar{C}}\right)\left(\overline{\bar{A} \bar{B} \bar{D}}\right)$$

$$= \left(\bar{A} + \bar{B} + \bar{D}\right)\left(\bar{\bar{A}} + \bar{\bar{B}} + \bar{C}\right)\left(\bar{A} + \bar{\bar{C}}\right)\left(\bar{\bar{A}} + \bar{\bar{B}} + \bar{\bar{D}}\right)$$

$$= \left(\bar{A} + \bar{B} + \bar{D}\right)\left(A + B + \bar{C}\right)\left(\bar{A} + C\right)(A + B + D)$$

It is possible to directly the expression for Y by using DeMorgans theorem for each minterm as follows :

$$\bar{f} = A B D + \bar{A} \bar{B} \bar{C} + A\bar{C} + \bar{A} \bar{B} \bar{D} \rightarrow = \left(\bar{A} + \bar{B} + \bar{D}\right)\left(A + B + \bar{C}\right)\left(\bar{A} + C\right)(A + B + D)$$

see the output levels in the truth table as shown in the Table 7.41. Here outputs are defined for input conditions from 0 0 0 to 1 0 1. For remaining two conditions of input, output is not defined, hence these are called don't care conditions for this truth table.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	X

Table 7.41

A circuit designer is free to make the output for any "don't care" condition either a '0' or a '1' in order to produce the simplest output expression.

7.18.1 Describing Incomplete Boolean Function

We describe the Boolean function using either a minterm canonical formula or a maxterm canonical formula. In order to obtain similar-type expressions for imcomplete Boolean functions we use additional term to specify don't care conditions in the original expression. This is illustrated in the following examples.

In expression,

$$f(A, B, C) = \Sigma m (0, 2, 4) + d (1, 5)$$

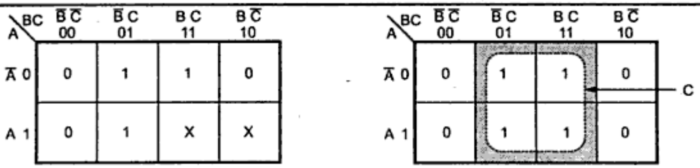
minterms are 0, 2 and 4. The additional term d(1, 5) is introduced to specify the don't care conditions. This terms specifies that outputs for minterms 1 and 5 are not specified and hence these are don't care conditions. Letter d is used to indicate don't care conditions in the expression.

The above expression indicates how to represent don't care conditions in the minterm canonical formula. In the similar manner, we can specify the don't care conditions in the maxterm canonical formula. For example,

$$f(A, B, C) = \Sigma \pi M (2, 5, 7) + d(1, 3)$$

7.18.2 Don't Care Conditions in Logic Design

In this section, we see the example of incompletely specified Boolean function. Let us see the logic circuit for an even parity generator for 4-bit BCD number. The Table 7.42 shows the truth table for even-parity generator. The truth table shows that the output for last six input conditions cannot be specified, because such input conditions does not occur when input is in the BCD form.



A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	1	0
A 1	0	1	X	X

(a)

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	1	0
A 1	0	1	1	0

(b)

Fig. 7.60 Use of don't care conditions

It is not always advisable to put don't cares as 1s. This is illustrated in Fig. 7.60 (b). Here, the don't care output for cell ABC is taken as 1 to form a quad, and don't care output for cell $AB\bar{C}$ is taken as 0, since it is not helping any way to reduce an expression. Using don't care conditions in this way we get the simplified boolean expression as

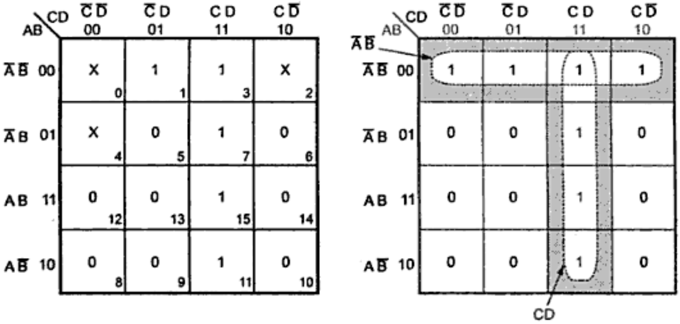
$$Y = C$$

From the above discussion we can realize that it is important to decide which don't cares to change to 0 and which to 1 to produce the best K-map grouping (i.e. the simplest expression). Now, we will see more examples to provide practice in dealing with "don't care" conditions.

Example 7.86 : *Find the reduced SOP form of the following function.*

$$f(A, B, C, D) = \sum m\,(1, 3, 7, 11, 15) + \sum d\,(0, 2, 4).$$

Solution :



AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	X (0)	1 (1)	1 (3)	X (2)
$\bar{A}B$ 01	X (4)	0 (5)	1 (7)	0 (6)
AB 11	0 (12)	0 (13)	1 (15)	0 (14)
$A\bar{B}$ 10	0 (8)	0 (9)	1 (11)	0 (10)

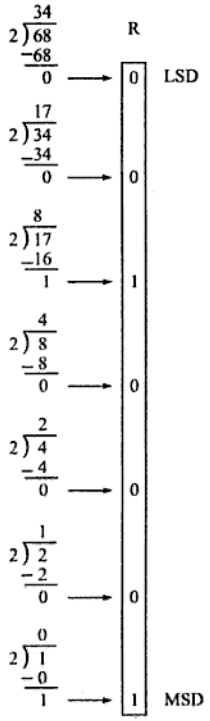
(a)

AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1	1	1	1
$\bar{A}B$ 01	0	0	1	0
AB 11	0	0	1	0
$A\bar{B}$ 10	0	0	1	0

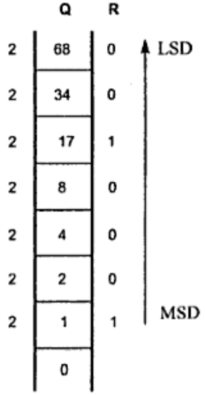
(b)

Fig. 7.61

Step 2 : Convert 68_{10} to its binary equivalent.



≡



Note : Q : Quotient
R : Remainder

Step 3 :

Find 2's complement of 68

$$\begin{array}{rcccccccccl} 68_{10} & = & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & \\ & & & & & & & 1 & 1 & & \leftarrow \text{Carry} \\ & & 1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & \text{1's complement} \\ & + & & & & & & & & 1 & \\ \hline & & 1 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & \text{2's complement} \end{array}$$

Solution : i) $(193)_x = (623)_8$

Converting octal into decimal

$$6 \times 8^2 + 2 \times 8 + 3 = (403)$$

$$(623)_8 = (403)_{10}$$

$$\therefore \quad (193)_x = (403)_{10}$$

$$1 \times x^2 + 9 \times x + 3 \times x^0 = 403$$

$$x^2 + 9x + 3 = 403$$

$$\therefore \quad x = 16 \text{ or } x = -25$$

Negative is not applicable

$$\therefore \quad x = 16$$

$$\therefore \quad (193)_{16} = (623)_8$$

ii) $(225)_x = (341)_8$

Converting octal into decimal

$$3 \times 8^2 + 4 \times 8^1 + 1 \times 8^0 = 225_{10}$$

$$\therefore \quad x = 10$$

iii) $(211)_x = (152)_8$

Converting octal into decimal

$$2x^2 + x + 1 = 8^2 \times 1 + 5 \times 8 + 2$$

$$2x^2 + x + 1 = 106$$

$$\therefore \quad 2x^2 + x - 105 = 0$$

$$(x - 7)(2x + 15) = 0$$

$$x = 7$$

$$\therefore \quad (211)_7 = (152)_8$$

Example 7.98 : *Convert the following binary code to Gray code* $(110110)_2$.

Solution :

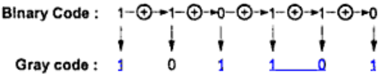


Fig. 7.65

Example 7.103 : *Simplify each of the following using DeMorgan's theorem*

a) $\overline{\left(A+\overline{B}\right)\left(\overline{A}+B\right)}$ b) $\overline{\overline{\overline{\overline{A}\,\overline{B}}\,C}\,D}$.

Solution :

a) $\overline{\left(A+\overline{B}\right)\left(\overline{A}+B\right)}$

$= \overline{A+\overline{B}}+\overline{\overline{A}+B}$ DeMorgan's theorem 1

$= \overline{A}\cdot\overline{\overline{B}}+\overline{\overline{A}}\cdot\overline{B}$ DeMorgan's theorem 2

$= \overline{A}\cdot B+A\cdot\overline{B}$ $\left[\overline{\overline{A}}=A\right]$

$= A\oplus B$

b) $\overline{\overline{\overline{\overline{A}\,\overline{B}}\,C}\,D}$ $= \overline{\overline{\overline{\overline{A}\,\overline{B}}\,C}}+\overline{D}$ DeMorgan's theorem 1

$= \overline{\overline{A}\,\overline{B}}\,C+\overline{D}$ $\left[\overline{\overline{A}}=A\right]$

$= \left(\overline{A}+\overline{B}\right)C+\overline{D}$ DeMorgan's theorem 1

Example 7.104 : *Verify the following Boolean algebraic manipulation. Justify each step with a reference to a postulate or theorem :*

i) $(X+\overline{Y}+XY)\,(X+\overline{Y})\overline{X}Y=0$

ii) $(AB+C+D)\,(\overline{C}+D)\,(\overline{C}+D+E)=AB\overline{C}+D$

Solution : i) $(X+\overline{Y}+XY)\ (X+\overline{Y})\,(\overline{X}Y)$

$= (X+\overline{Y}+X)\ (X+\overline{Y})\,(\overline{X}Y)$ $\because\ A+\overline{A}B=A+B$

$= (X+\overline{Y})\ (X+\overline{Y})\,(\overline{X}Y)$ $\because\ A+A=A$

$= (X+\overline{Y})\,(\overline{X}Y)$ $\because\ A\cdot A=A$

$= X\overline{X}+\overline{Y}\,\overline{X}Y$ $\because\ A\cdot\overline{A}=0$

$= 0$ .... Proved

ii) $(AB+C+D)\ (\overline{C}+D)\ (\overline{C}+D+E)$

$= (AB+C+D)\ (\overline{C}\,\overline{C}+\overline{C}D+\overline{C}E+\overline{C}D+DD+DE)$

$= (AB+C+D)\ (\overline{C}+\overline{C}D+\overline{C}E+\overline{C}D+D+DE)$ $\because\ A\cdot A=0$

$= (AB+C+D)\ [\overline{C}+D\,(\overline{C}+\overline{C}+1+E)+\overline{C}E\,]$

$= (AB+C+D)\ (\overline{C}+D+\overline{C}E\,)$ $\because\ A+1=A$

$= (AB+C+D)\ [\overline{C}+(1+E)+D]$

$= (AB+C+D)(\overline{C}+D)$ $\quad \because A+1 = A$

$= AB\overline{C}+ABD+C\overline{C}+CD+\overline{C}D+D$

$= AB\overline{C}+ABD+CD+\overline{C}D+D$ $\quad \because A\overline{A} = 0$

$= AB\overline{C}+D(AB+C+\overline{C}+1)$

$= AB\overline{C}+D$ ..... Proved $\quad \because A+1 = A$

Example 7.105 : *Simplify the following expression*
$a+a\,\overline{b}+a\,\overline{b}\,\overline{c}+a\,\overline{b}\,\overline{c}\,\overline{d}+......$

Solution : $a+a\,\overline{b}+a\,\overline{b}\,\overline{c}+a\,\overline{b}\,\overline{c}\,\overline{d}+......$

$= a\,[1+\overline{b}+\overline{b}\,\overline{c}+\overline{b}\,\overline{c}\,\overline{d}+......]$

$= a$ $\quad \because A+1 = 1$

Example 7.106 : *Prove that*
$(a+b)\,(\overline{a}+c)\,(b+c) = (a+b)\,(\overline{a}+c)$

Solution : $(a+b)\,(\overline{a}+c)\,(b+c)$

$= (a\,\overline{a}+a\,c+\overline{a}\,b+b\,c)\,(b+c)$

$= (a\,c+\overline{a}\,b+b\,c)\,(b+c)$ $\quad \because A\,\overline{A} = 0$

$= a\,b\,c + a\,c\,c + \overline{a}\,b\,b + \overline{a}\,b\,c + b\,b\,c + b\,c\,c$

$= a\,b\,c + a\,c + \overline{a}\,b + \overline{a}\,b\,c + b\,c + b\,c$ $\quad \because A\,A = A$

$= a\,c\,(b+1)+\overline{a}\,b + b\,c\,(\overline{a}+1+1)$

$= a\,c + \overline{a}\,b + b\,c$ $\quad \because A+1 = 1$

$= a\,c + \overline{a}\,b + b\,c+a\,\overline{a}$ $\quad \because a\,\overline{a} = 0$

$= c\,(a+b) + \overline{a}\,(a+b)$

$= (a+b)\,(\overline{a}+c)$ ...... Proved.

Example 7.107 : *Prove from fundamentals the following expressions :*

i) $x\,y+\overline{x}\,z+y\,z = \overline{x}\,z+xy$

ii) $\overline{x}\,\overline{y}\,z+\overline{x}\,y\,z+x\,\overline{y} = x\overline{y} = \overline{x}\,z+x\overline{y}$.

Solution : i) $x\,y+\overline{x}\,z+y\,z$

$= x\,y+\overline{x}\,z+y\,z\,(x+\overline{x})$

$= x\,y+\overline{x}\,z+x\,y\,z+\overline{x}\,y\,z$

$= x\,y\,(1+z)+\overline{x}\,z(1+y)$

$= x\,y+\overline{x}\,z$ ..... Proved.

ii) $\overline{x}\,\overline{y}\,z+\overline{x}\,y\,z+x\,\overline{y}$

$= \overline{x}\,\overline{y}\,z+\overline{x}\,y\,z+x\,\overline{y}$

$$= \overline{x}\,z(\overline{y}+y)+x\overline{y} \qquad \because A+\overline{A}=1$$

$$= \overline{x}\,z+x\overline{y} \qquad \text{.... Proved.}$$

Example 7.108 : *Prove the following using Boolean theorems.*

i) $(x+\overline{x}\,\overline{y})(\overline{x}+\overline{y})+yz=\overline{y}+z$

ii) $\overline{w}\,\overline{y}\,\overline{z}+wz+\overline{y}z+xyz=\overline{w}\,\overline{y}+wz+xz$

Solution : i)

$$(x+\overline{x}\,\overline{y})(\overline{x}+\overline{y})+yz = x\overline{x}+x\overline{y}+\overline{x}\,\overline{y}+\overline{x}\,\overline{y}+yz$$

$$= x\overline{y}+\overline{x}\,\overline{y}+\overline{x}\,\overline{y}+yz \qquad \because A\cdot\overline{A}=0$$

$$= \overline{y}(x+\overline{x}+\overline{x})+yz \qquad \because x+\overline{x}=1$$

$$= \overline{y}+yz \qquad \because A+\overline{A}B=A+B$$

$$= \overline{y}+z$$

ii)

$$\overline{w}\,\overline{y}\,\overline{z}+wz+\overline{y}z+xyz = \overline{w}\,\overline{y}\,\overline{z}+\overline{y}z+wz+z+xyz \qquad \because A+A=A$$

$$= \overline{y}(\overline{w}\,\overline{z}+z)+wz+z(\overline{y}+xy)$$

$$= \overline{y}(\overline{w}+z)+wz+z(\overline{y}+x)$$

$$\because A+\overline{A}B=A+B$$

$$= \overline{w}\,\overline{y}+\overline{y}z+wz+\overline{y}z+xz$$

$$= \overline{w}\,\overline{y}(z+\overline{z})+\overline{y}z+wz+\overline{y}z+xz$$

$$\because z+\overline{z}=1$$

$$= \overline{w}\,\overline{y}\,\overline{z}+\overline{w}\,\overline{y}\,\overline{z}+\overline{w}\,\overline{y}\,z+w\,\overline{y}\,z+wz+xz$$

$$\because A+A=A$$

$$= \overline{w}\,\overline{y}(\overline{z}+z)+wz(\overline{y}+1)+xz$$

$$\because z+\overline{z}=1 \text{ and } \overline{y}+1=1$$

$$= \overline{w}\,\overline{y}+wz+xz$$

Example 7.109 : *Transform each of the following canonical expressions into its other canonical form in decimal notation.*

(i) $f(x, y, z) = \sum m(1,3,5)$

(ii) $f(w, x, y, z) = \pi M(0,2,5,6,7,8,9,11,12)$.

Solution :

(i) $f(x, y, z) = \pi M(0,2,4,6,7)$

(ii) $f(w, x, y, z) = \sum m(1,3,4,10,13,14,15)$

b) Obtain the minimal SOP and POS expressions for H and V.

Inputs			**Outputs**	
P	**T**	**L**	**H**	**V**
LOW	LOW	LOW	OFF	OPEN
LOW	LOW	HIGH	ON	CLOSED
LOW	HIGH	LOW	OFF	OPEN
LOW	HIGH	HIGH	OFF	CLOSED
HIGH	LOW	LOW	ON	OPEN
HIGH	LOW	HIGH	ON	CLOSED
HIGH	HIGH	LOW	OFF	CLOSED
HIGH	HIGH	HIGH	X	X

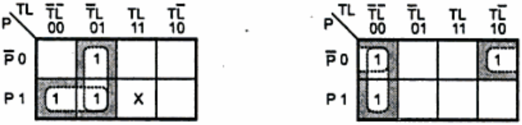
X : System shut down

Solution : a)

Inputs			**Outputs**	
P	**T**	**L**	**H**	**V**
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	X	X

Table 7.44

b) SOP Expressions


P
TL
$\overline{T}\overline{L}$ 00
$\overline{T}L$ 01
TL 11
$T\overline{L}$ 10
$\overline{P}$ 0
P 1
1
1
1
X
1
1
1

Map for H
$H = \overline{T}L + P\overline{T}$

Map for V
$V = \overline{P}\overline{L} + \overline{T}\overline{L}$

Fig. 7.69

Example 7.116 : *Express the switching function $f_{(BA)} = A$ interms of minterms.*

Solution :

$$
\begin{aligned}
f_{(BA)} &= A \\
&= A\ (B+\overline{B}) \\
&= AB + A\overline{B}
\end{aligned}
$$

Example 7.117 : *Simplify the five variable switching function $f_{(EDCBA)} = \Sigma m$ (3, 5, 6, 8, 9, 12, 13, 14, 19, 22, 24, 25, 30).*

Solution :

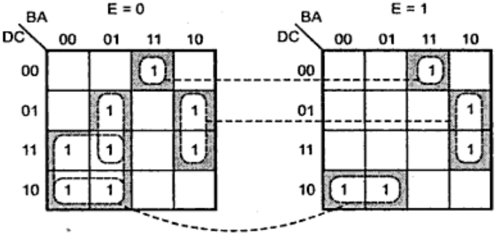


Fig. 7.75

$$
f(E,D,C,B,A) = \overline{D}\,\overline{C}\,B\,A + \overline{E}\,C\,\overline{B}\,A + C\,B\,\overline{A} + \overline{E}\,D\,\overline{B} + D\,\overline{C}\,\overline{B}
$$

Example 7.118 : *Apply DeMorgan's theorem to simplify $\overline{A + B\overline{C}}$.*

Solution :

$$
\begin{aligned}
\overline{A + B\overline{C}} &= \overline{A} \cdot \overline{B\overline{C}} \\
&= \overline{A} \cdot (\overline{B} + C) = \overline{A}\,\overline{B} + \overline{A}\,C
\end{aligned}
$$

Example 7.119 : *Plot the expression on K-map :*
$F(w, x, y) = \Sigma(0, 1, 3, 5, 6) + d(2, 4)$.

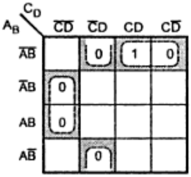
Solution :

W \ XY	00	01	11	10
0	1	1	1	X
1	X	1	0	1

Fig. 7.76

Example 7.120 : *Simplify using K-map to obtain a minimum POS expression :*
$(\overline{A}+\overline{B}+C+D)(A+\overline{B}+C+D)(A+B+C+\overline{D})(A+B+\overline{C}+\overline{D})(\overline{A}+B+C+\overline{D})(A+B+\overline{C}+D)$

Solution : $Y = ((\overline{B}+C+D)(B+C+\overline{D})(A+B+\overline{C})$



$AB \backslash CD$	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$		0	1	0
$\overline{A}B$	0			
AB	0			
$A\overline{B}$		0		

Fig. 7.77

Example 7.121 : *How will you use a 4 input NOR gate as a 2 input NOR gate ?*

Solution : By connecting unused 2 inputs to logic 0 we can use a 4 input NOR gate as a 2 input NOR gate.

Example 7.122 : *Show that the NAND connection is not associative.*

Solution : The NAND connection is not associative says that

$$\overline{\overline{A\cdot B}\cdot C} \neq \overline{A\cdot\overline{B\cdot C}}$$

$$\therefore \quad \overline{\overline{A\cdot B}} + \overline{C} \neq \overline{A} + \overline{\overline{BC}}$$

$$\therefore \quad A\,B+\overline{C} \neq \overline{A}+BC$$

... Proved

Example 7.123 : *For each statement below, draw the appropriate logic-gate representation and indicate the type of gate.*

a) A HIGH output occurs only when all three inputs are LOW

b) A LOW output occurs when any of the four inputs is LOW

c) A LOW output occurs only when all eight inputs are HIGH

Solution :

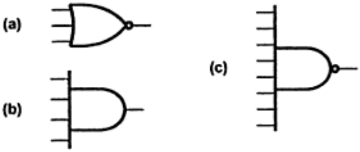


Fig. 7.78

Example 7.127 : *Convert the given circuit to one using only NOR gates.*

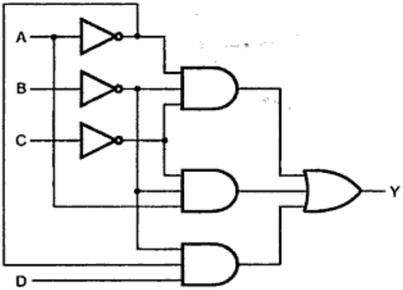


Fig. 7.83

Solution : Adding bubbles on the output of OR gate and on the inputs of AND gate we have

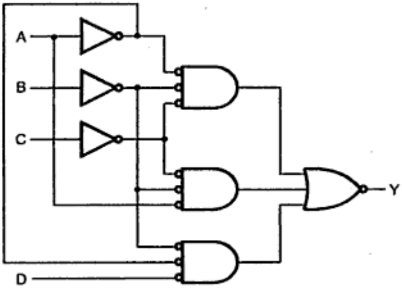


Fig. 7.84

Adding an inverter on each line that received bubble we have,

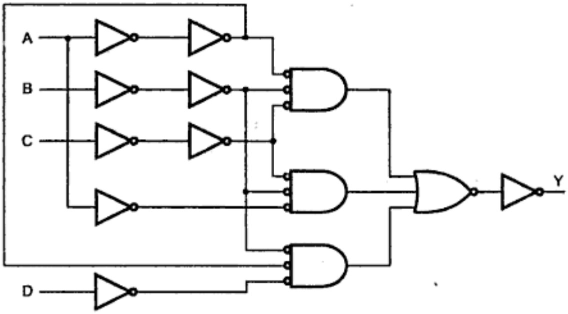


Fig. 7.85

Eliminating double inversion we have,

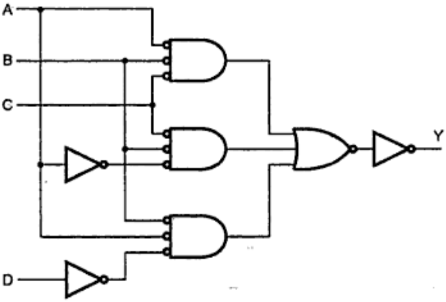


Fig. 7.86

$= \overline{\overline{AB}}\cdot\overline{\overline{CD}}$ **DeMorgan's Theorem 2**

$= \overline{\overline{\overline{AB}}\cdot\overline{\overline{CD}}}$

Therefore the logic circuit is,

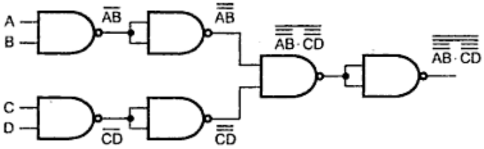

A
B
$\overline{AB}$
$\overline{\overline{AB}}$
$\overline{\overline{AB}}\cdot\overline{\overline{CD}}$
$\overline{\overline{\overline{AB}}\cdot\overline{\overline{CD}}}$
C
D
$\overline{CD}$
$\overline{\overline{CD}}$

Fig. 7.89

Example 7.130 : *Implement AB + $\bar{C}\bar{D}$ = F with three NAND gates. Draw the logic circuit.*

Solution :

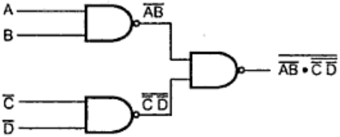

A
B
$\overline{AB}$
$\overline{\overline{AB}\bullet\overline{\bar{C}\bar{D}}}$
$\bar{C}$
$\bar{D}$
$\overline{\bar{C}\bar{D}}$

Fig. 7.90

$$A\,B + \bar{C}\,\bar{D}$$

$$= \overline{\overline{A\,B}} + \overline{\overline{\bar{C}\,\bar{D}}}$$

$$= \overline{\overline{A\,B}\cdot\overline{\bar{C}\,\bar{D}}}$$

Example 7.131 : *Find a minimal sum-of-products representation for*

f(A, B, C, D, E) = Σm (1, 4, 6, 10, 20, 22, 24, 26) + d(0, 11, 16, 27) using Karnaugh map method. Draw the circuit of the minimal expression using only NAND gates.

Solution : The given function has 5 variables. Thus solving it by five variable K-map we get,

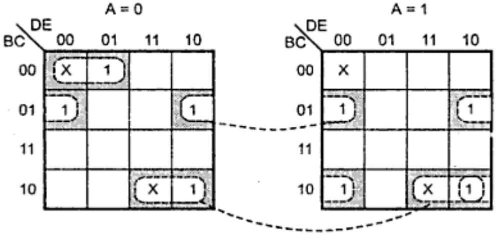
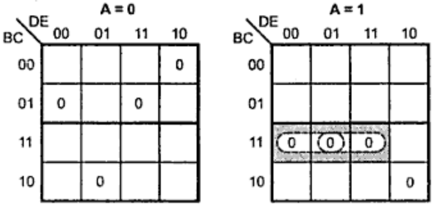

A = 0
A = 1
DE
BC
00
01
11
10
X
1

Fig. 7.91 (a)

Example 7.133 : *Minimize the following using Karnaugh map. Implement the resultant function using NOR gates only.*

$$f(A,B,C,D,E) = \pi M(2,4,7,9,26,28,29,31)$$

Solution :



A = 0

BC \ DE	00	01	11	10
00				0
01	0		0	
11				
10		0		

A = 1

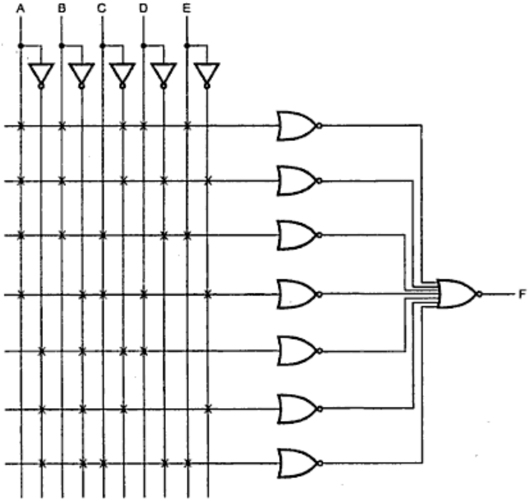
BC \ DE	00	01	11	10
00				
01				
11	0	0	0	
10				0

Fig. 7.93

$$F(A,B,C,D,E) = (A+B+\overline{C}+D+E)\,(A+B+\overline{C}+\overline{D}+\overline{E})\,(A+B+C+\overline{D}+E)\,(A+\overline{B}+C+D+\overline{E})$$
$$(\overline{A}+\overline{B}+\overline{C}+D)\,(\overline{A}+\overline{B}+\overline{C}+\overline{E})\,(\overline{A}+\overline{B}+C+\overline{D}+E)$$

OR-AND implementation can be replaced by NOR-NOR implementation.

Logic diagram using NOR gates



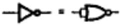
Note : Inverter can be represented by NOR gate 

Fig. 7.94

33. *State and prove the consensus theorem in Boolean algebra.*

34. *State the rules in Boolean algebra.*

35. *Explain the Demorgan's theorems in Boolean algebra.*

36. *Explain the principle of duality with the help of example.*

37. *What do you mean by literals ?*

38. *Name the two basic types of Boolean expressions.*

39. *Convert the given expressions in standard SOP form*

(i) $f(A, B, C) = A + AB + CB$ (ii) $f(P, Q, R) = PQ + R + PR$

40. *Convert the given expression in standard POS form*

(i) $f(A, B, C) = (A + B)(B + C)$ (ii) $f(P, Q, R) = (P + \bar{Q})(P + R)$

41. *Express the following function in standard SOP form*

$F_1 = AB + \bar{C}D + A\bar{B}C$.

(Ans. : $\bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}CD + AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD$)

42. *Reduce the following Boolean expressions :*

a) $B\bar{C}\bar{D} + BC\bar{D}$ **(Ans. : $B\bar{D}$)**

b) $(\bar{C} + B)(C + B)$ **(Ans. : B)**

c) $\overline{A \cdot (A + C)}$ **(Ans. : $\bar{A}$)**

d) $\overline{\overline{A\bar{B} + ABC} + A(B + A\bar{B})}$ **(Ans. : 0)**

43. *Simplify following logical expressions using Karnaugh maps*

i) $Y = A\bar{B} + AB + \bar{A}B$ **(Ans. : Y = A + B)**

ii) $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C}$ **(Ans. : $Y = \bar{A}\bar{B} + \bar{C}$)**

iii) $Y = \bar{A}\bar{B}CD + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}D + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D + ABCD$

(Ans. : $Y = ABD + \bar{A}\bar{B}D + \bar{B}\bar{C}$)

44. *Simplify the following Boolean expressions using Karnaugh map.*

i) $Y = \bar{A}C + \bar{B}C + A\bar{B}\bar{C} + \bar{A}B$ **(Ans. : $A\bar{B} + \bar{A}B + \bar{A}C$)**

ii) $Y = \bar{Q}RS + R\bar{S} + \bar{P}\bar{Q}\bar{R}\bar{S} + \bar{P}\bar{Q}R$ **(Ans. : $\bar{Q}R + R\bar{S} + \bar{P}\bar{Q}\bar{S}$)**

iii) $Y = \bar{A}B + C + A\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{C}\bar{D}$ **(Ans. : $A + B + C + \bar{D}$)**

iv) $Y = (\bar{P} + Q + \bar{R})(P + Q + R)(P + Q + \bar{R})$ **(Ans. : $Q + P\bar{R}$)**

45. *Simplify the following functions*

i) $f_1(A, B, C, D) = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$ **(Ans. : $(A \oplus B) \odot (C \oplus D)$)**

ii) $f_2(A, B, C, D) = \sum m(0, 1, 3, 8, 9, 13\ 15)$ **(Ans. : $ABD + \bar{A}\bar{B}D + \bar{B}\bar{C}$)**

iii) $f_3(A, B, C, D) = \sum m(0, 1, 2, 3, 11, 12, 14, 15)$ **(Ans. : $\bar{A}\bar{B} + AB\bar{D} + ACD$)**

iv) $f_4(W, X, Y, Z) = \sum m(0, 3, 4, 7, 9, 12, 14)$ **(Ans. : $WX\bar{Z} + \bar{W}(YZ + \bar{Y}\bar{Z}) + W\bar{X}\bar{Y}Z$)**

46. *Design a logic circuit to provide an output when any two or three of four switches are closed.*

(Ans. : $\bar{A}CD + BC\bar{D} + A\bar{B}C + B\bar{C}D + A\bar{C}D + AB\bar{C}$)

47. *Use a Karnaugh map to reduce each expression to a minimum sum of products form*
    - *i)* $Y = \bar{A}\,\bar{B}\,\bar{C}\,\bar{D} + \bar{A}\,\bar{B}\,\bar{C}\,D + A\,B\,C\,D + A\,B\,C\,\bar{D}$ **(Ans. : $\bar{A}\,\bar{B}\,\bar{C} + A\,B\,C$)**
    - *ii)* $Y = \bar{A}\,B(\bar{C}\,\bar{D} + \bar{C}\,D) + A\,B\,(\bar{C}\,\bar{D} + \bar{C}\,D) + A\,\bar{B}\,\bar{C}\,D$

(Ans. : $Y = B\,\bar{C} + A\,\bar{C}\,D$)

48. *What are don't care conditions ?*
49. *Write the names of basic logical operators.*
50. *What is a logic gate ?*
51. *Draw the logic symbol and construct the truth table for each of the following gates :*
    - *a) Two input NAND gate*
    - *b) Three input OR gate*
    - *c) Two input EX-OR gate*
    - *d) Three input EX-NOR gate*
    - *e) NOT gate*
52. *Write the names of Universal gates.*
53. *Why are NAND and NOR gates known as Universal gates ?*
54. *Give the Boolean expressions used for following gates*
    - *a) AND*
    - *b) NOR*
    - *c) EX-OR*
    - *d) OR*
    - *e) NOT*
55. *Develop a circuit for each of the following Boolean expressions using AND, OR, and NOT gates:*
    - *a)* $Y = AB + BC$
    - *b)* $Y = ABC + AD$
    - *c)* $Y = (A + C)\left(\bar{B} + D\right)$
    - *d)* $Y = A\,(\bar{B} + C)$
    - *e)* $Y = AB\,(C + D)$
56. *Develop a circuit for each of the following Boolean expressions using only NAND gates.*
    - *a)* $Y = (A + C)\,(\bar{B} + D)$
    - *b)* $Y = AB\,(C + D)$
57. *Develop a circuit for each of the following Boolean expressions using only NOR gates.*
    - *a)* $Y = ABC + AD$
    - *b)* $Y = A\,(\bar{B} + C)$

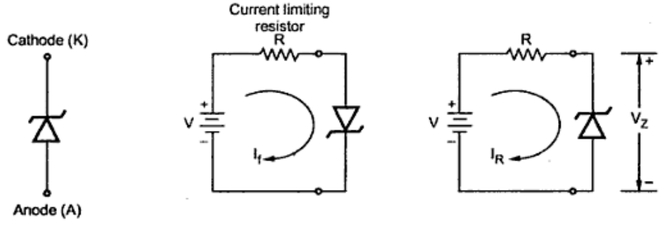
□□□

2

Zener Diode and Applications

2.1 Introduction

The zener diode is a silicon p-n junction semiconductor device, which is generally operated in its **reverse breakdown region.** The zener diodes are fabricated with precise breakdown voltages, by controlling the doping level during manufacturing. The zener diodes have breakdown voltage range from 3 V to 200 V. In 1934, a physicist Carl Zener investigated the breakdown phenomenon in the p-n junction diode.



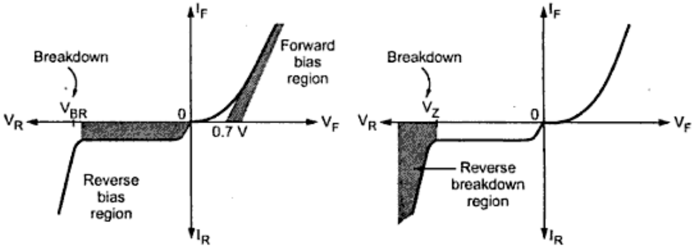
(a) Symbol **(b) Forward biasing** **(c) Reverse biasing**

Fig. 2.1 Zener diode

The Fig. 2.1 (a) shows the symbol of zener diode. The d.c. voltage can be applied to the zener diode so as to make it forward biased or reverse biased. This is shown in the Fig. 2.1 (b) and (c). Practically zener diodes are operated in **reverse biased mode.**

2.2 Characteristics of Zener Diode

In the forward biased condition, the normal rectifier diode and the zener diode operate in similar fashion. But the zener diode is designed to be operated in the reverse biased condition. In reverse biased condition, the diode carries reverse saturation current till the reverse voltage applied is less than the reverse breakdown voltage. When the reverse voltage exceeds reverse breakdown voltage, the current through it changes drastically but the voltage across it remains almost constant. Such a breakdown region is a normal operating region for a zener diode. The normal operating regions for a rectifier diode and a zener diode are shown in the Fig. 2.2 (a) and (b).



(a) Operating regions shown shaded for normal diode

(b) Operating regions shown shaded for zener diode

Fig. 2.2

The breakdown characteristic for a zener diode is significantly important, as it is an operating region for the diode. When the reverse voltage applied to a zener diode is increased, initially the current through it is very small, of the order of few μA or less. This is the reverse leakage current of the diode, denoted by I_0. At a certain reverse voltage, current through zener diode increases rapidly. The change from a low value to large value of current is very sharp and well defined. Such a sharp change in the reverse characteristics is called **knee** or **zener knee** of the curve. At this knee, a breakdown is said to occur in the device. The reverse bias voltage at which the breakdown occurs is called **zener breakdown voltage**, denoted as V_Z.

> **Key Point:** *The voltage V_Z is set by carefully controlling the doping level during manufacturing process.*

The current corresponding to a knee point is called **zener knee current** and it is a minimum current zener must carry to operate in reverse breakdown region. It is denoted as I_{ZK} or I_{Zmin}.

From the bottom of the knee, the zener breakdown voltage remains almost constant, though it increases slightly as the zener current I_Z, increases. The current at which the nominal zener breakdown voltage is specified is called **zener test current**, denoted as I_{ZT}. This value and corresponding zener voltage V_Z are specified on a datasheet of a zener diode. Every zener diode has a capacity to carry current. As current increases, the power dissipation $P_Z = V_Z I_Z$ increases. If this dissipation increases beyond certain value, the diode may get damaged.

The maximum current a zener diode can carry safely is called **zener maximum current** and is denoted as I_{ZM} or I_{Zmax}.

In practical circuits to limit the zener current between I_{Zmin} and I_{Zmax}, a current limiting resistor is used in series with the zener diode.

The complete V-I characteristics of the zener diode is shown in the Fig. 2.3.

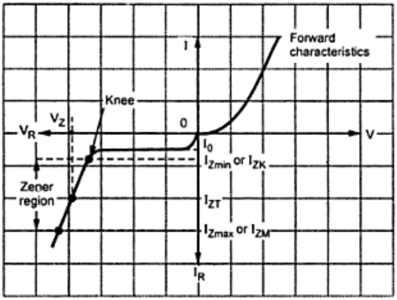


Fig. 2.3 V-I characteristics of zener diode

2.3 Equivalent Circuit of Zener Diode

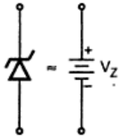
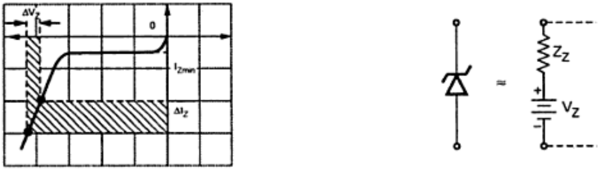


Fig. 2.4 Ideal equivalent circuit of zener diode

When the breakdown occurs then I_Z may increase from I_{Zmin} to I_{Zmax} but voltage across zener remains constant. Hence actually the internal zener imepdance decreases as current increases in the zener region. But this impedance is very small. Hence **ideally** the zener diode is indicated by a battery of voltage V_Z , which remains fairly constant in the zener region. This is shown in the Fig. 2.4.

Practically though very small, zener has its internal resistance. In the zener region, this resistance is called **dynamic resistance** of the zener denoted as Z_Z. Practically zener region is not exactly vertical. The small change in zener current ΔI_Z produces a small change in zener voltage ΔV_Z. The ratio of ΔV_Z to ΔI_Z is called zener resistance Z_Z. This is shown in the Fig. 2.5 (a). Hence practically zener equivalent circuit is shown with a battery of V_Z alongwith a series resistance Z_Z as indicated in the Fig. 2.5 (b).



(a) Dynamic resistance Fig. 2.5 (b) A.C. equivalent circuit

From the graph the dynamic resistance is defined as,

$$\boxed{Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{1}{\left[\dfrac{\Delta I_Z}{\Delta V_Z}\right]} = \frac{1}{\left[\begin{array}{l}\text{Slope of the reverse}\\ \text{characteristics in}\\ \text{zener region}\end{array}\right]}}$$

This value is specified generally at zener test current I_{ZT}.

Key Point: *In most of the cases this value is almost constant over the full range of zener region i.e. from I_{Zmin} to I_{Zmax}. It is of the order of few tens of ohms.*

2.4 Effect of Temperature on Zener Diode

The zener voltage V_Z changes with the temperature. The percentage change in the zener voltage V_Z for the every °C change in temperature is called **temperature coefficient** of a zener diode. It is denoted as TC and expressed as % / °C.

Mathematically it can be defined as,

$$\boxed{TC = \frac{\Delta V_Z}{V_Z(T_1 - T_0)} \times [100]\ \% / ^\circ C} \qquad \dots (1)$$

where T_1 is the final temperature of junction while T_0 is generally 25 °C at which nominal zener voltage V_Z is specified. ΔV_Z is the resulting change in the zener voltage due to the temperature variation.

A positive value of TC indicates that there is increase in V_Z due to increase in temperature or decrease in V_Z due to decrease in temperature. The negative value of TC indicates that there is increase in V_Z due to decrease in temperature or decrease in V_Z due to increase in temperature.

From the equation (1) we can write that the change in V_Z is,

$$\boxed{\Delta V_Z = \frac{V_Z TC\,(T_1 - T_0)}{100} = \frac{V_Z TC\,\Delta T}{100}} \qquad \dots (2)$$

where ΔT = change in temperature

Thus V_{Z2} at temperature T_2 can be obtained as,

$$\boxed{V_{Z2} = [V_{Z1} \text{ at } T_1] + \left[\frac{\Delta T \times TC \times V_Z}{100}\right]}$$

Sometimes TC for a zener diode is expressed in mV/°C and in such case, corresponding change in V_Z can be obtained as,

$$\boxed{\Delta V_Z = TC\,(T_1 - T_0) = TC \times \Delta T} \quad \ldots (3)$$

For zener diodes with V_Z less than 6 V, temperature coefficient is negative so V_Z decreases as temperature increases.

Key Point : *While for zener diodes with V_Z greater than 6 V, temperature coefficient is positive so V_Z increases as temperature increases.*

2.5 Zener Power Dissipation and Derating

Every zener diode has a capacity to dissipate certain power. This capacity is expressed as its maximum d.c. power dissipation rating, at a particular temperature. For example, the 1N961 zener is rated at a 320 mW while the 1 N 3305 A is rated at a 50 W. This d.c. power dissipation rating is denoted as $P_{D\,(max)}$. The d.c. power dissipation in zener is calculated as,

$$\boxed{P_D = V_Z I_Z}$$

The product of nominal zener voltage and I_{ZM} which is maximum zener current gives $P_{D(max)}$ rating for the zener.

$$\therefore \quad \boxed{P_{D(max)} = V_Z I_{ZM}}$$

As mentioned above, $P_{D(max)}$ rating is specified at or below certain temperature. For high temperature, the zener cannot dissipate same power but its power dissipation capacity reduces. This reduction in maximum power dissipation is according to a factor called **derating factor**. This is called **power derating** of a zener.

The derating factor is expressed as mW/°C and hence derated power dissipation can be obtained as,

$$\therefore \quad \boxed{\begin{aligned} P_{D(derated)} &= P_{D(max)} - [\text{Derating factor}]\,\Delta T \\ &= P_{D(max)} - [\text{mW}/^\circ\text{C}]\,\Delta T \end{aligned}}$$

➡ **Example 2.1 :** *A certain zener diode has maximum power rating of 320 mW at 50 °C, with a derating factor of 2.3 mW/ °C. Find the derated power rating at a temperature of* 100 °C.

Solution :

$$P_{D(max)} = 320 \text{ mW at } 50\ ^\circ\text{C, derating factor } 2.3 \text{ mW}/^\circ\text{C}$$

$$\begin{aligned} \therefore \quad P_{D(derated)} &= P_{D(max)} - [\text{Derating factor}]\,\Delta T \\ &= (320 \text{ mW}) - (2.3 \text{ mW}/\ ^\circ\text{C}) \times (100 - 50) \\ &= \mathbf{205\ mW} \end{aligned}$$

Thus maximum power zener can dissipate at 100 °C is **205 mW**.

2.6 Zener Diode Data Sheet Interpretation

The data sheets of various types of zener diodes are different from each other. But every data sheet consists of important basic information about a zener diode. The data sheet information can be divided into two types :

a) Electrical characteristics

b) Graphical information

2.6.1 Electrical Characteristics

The electrical characteristics of a zener diode includes information about important currents and voltages, related to the zener diode operation.

The Table 2.1 gives the electrical characteristics of 1N4728 - 1N 4732 series 1W zener diodes.

			Maximum zener impedance			**Leakage current**	
Type No.	**Nominal zener voltage V_Z at I_{ZT} (volts)**	**Test current I_{ZT} (mA)**	**Z_{ZT} at I_{ZT} (Ω)**	**Z_{ZK} at I_{ZK} (Ω)**	**I_{ZK} (mA)**	**I_R (μA) Max.**	**V_R (volts)**
1N4728	3.3	76	10	400	1.0	100	1.0
1N4729	3.6	69	10	400	1.0	100	1.0
1N4730	3.9	64	9.0	400	1.0	50	1.0
1N4731	4.3	58	9.0	400	1.0	10	1.0
1N4732	4.7	53	8.0	500	1.0	10	1.0

Table 2.1

These characteristics are specified at an ambient temperature of 25 °C. The maximum forward voltage is $V_f = 1.2$ V and $I_f = 200$ mA for all above mentioned types of zener diodes. These types of zeners have a standard tolerance on the nominal zener voltage of ± 10%.

In these characteristics, the first column indicates the type and number of a zener diode.

The second column indicates **nominal zener voltage** which is specified at a specific value of zener test current I_{ZT}. As the standard tolerance is ± 10%, the nominal V_Z value of 4.3 V can vary from 3.87 V to 4.73 V.

The third column gives the **zener test current** value I_{ZT} at which the nominal zener voltage V_Z is specified.

The fourth column gives the values of **dynamic zener impedance** Z_{ZT}, measured at zener test current. The dynamic means a.c. zener impedance which is the ratio of ΔV_Z to ΔI_Z as seen earlier. The ratio of V_Z and I_{ZT} gives d.c. zener impedance, which is not used and hence not specified in the table. This column also gives zener impedance calculated at knee current and the value of knee current I_{ZK}.

The fifth column gives **reverse leakage current** for the zener diode for the reverse voltage V_R less than the value at the knee of the characteristic curve. Thus V_R is value less than V_Z and hence reverse leakage current is similar to the reverse saturation current of nominal diodes, in the range of μA to nA.

Some data sheets include **maximum zener current** I_{ZM}. It is related to maximum power dissipation rating. If not specified, the approximate value of I_{ZM} can be obtained as,

$$\boxed{I_{ZM} = \frac{P_{D(max)}}{V_Z \text{ at } I_{ZT}}}$$

In addition to the electrical characteristics, the data sheet includes the table of maximum ratings. The Table 2.2 gives the maximum ratings for the 1N4728 - 1N4732 series 1W zener diodes.

Rating	Symbol	Value	Unit
DC power dissipation at T = 50°C	P_D	1.0	watt
Derate above 50 °C	Derating factor	6.67	mW/°C
Operating and storage junction temperature range	T_J, T_{stg}	– 65 to + 200	°C

Table 2.2 Maximum ratings

2.6.2 Graphical Information

The data sheet includes some curves indicating the graphical relations between some zener parameters. These curves can be referred to obtain the required information about the zener diode.

The data sheet for 1N4728 - 1N4732 series 1W zener diodes includes following three graphs :

i) Power derating curve

As mentioned in the electrical characteristics, maximum power dissipation is 1 W at 50 °C and it is to be derated above 50 °C. The graph shows that the $P_{D(max)}$ rating decreases linearily as the temperature increases. Thus using this graph, $P_{D(derated)}$ at any temperature can be obtained.

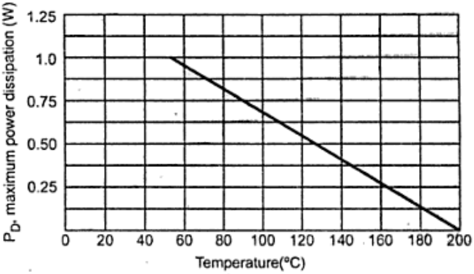


Fig. 2.6

ii) Temperature coefficient curve

As mentioned earlier, sometimes TC is expressed in mV/°C. The graph in datasheet gives the variations in TC with respect to zener voltage V_Z upto 12 V. The two curves on the graph define a range for the temperature coefficient. For example, a 5 V zener has a TC range approximately from 0 to 1.8 mV/°C, while a 10 V zener has a TC range from + 6 to 7.7 mV/°C.

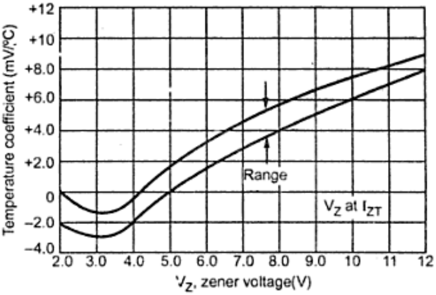


Fig. 2.7

iii) Zener impedance curve

This curve gives the effect of zener current on the zener impedance. The graph shows how the zener impedance Z_Z varies with zener current I_Z, for the selected values of the zener voltage. The graph shows that the zener impedance decreases as the zener current increases.

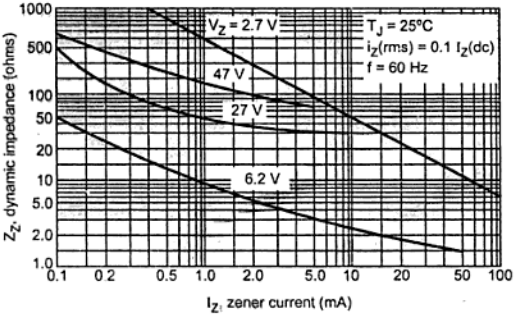


Fig. 2.8

Thus using the data sheet provided by the manufacturer, the proper zener diode, required for the application can be selected.

Example 2.2 : *For the circuit shown, calculate the zener diode current and the power dissipation.*

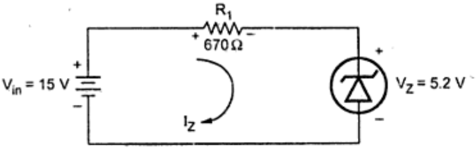


Fig. 2.9

Solution : Applying KVL,

$$-I_Z R_1 - V_Z + V_{in} = 0$$

$$\therefore \quad I_Z = \frac{V_{in} - V_Z}{R_1} = \frac{15 - 5.2}{670} = \mathbf{14.6268\ mA}$$

$$\therefore \quad P_D = V_Z I_Z = 5.2 \times 14.6268 \times 10^{-3} = \mathbf{76.059\ mW}$$

2.7 Breakdown Mechanisms in Zener Diode

There are two distinct mechanisms due to which breakdown may occur in the zener diode. One is called **zener breakdown** and the other **avalanche breakdown.** For most of commercially available silicon diodes, the maximum value of voltage breakdown by the zener mechanism is low, in the region of 5 V to 8 V. Consequently, for devices with breakdown voltages lower than 5 V, the zener mechanism predominates, between 5 and 8 V, both zener and avalanche mechanism are involved; whereas, above 8V the avalanche mechanism alone takes over.

> **Key Point:** *Practically zener breakdown is observed in the zener diodes with breakdown voltages less than 6 V while avalanche breakdown is observed in the zener diodes with breakdown voltages greater than 6 V.*

Commercially all such diodes are referred as **zener diodes** whether breakdown mechanism is zener or avalanche.

2.7.1 Zener Breakdown

The zener breakdown mechanism can be described qualitatively as follows :

The application of reverse bias, voltage (6 V or less) causes a field across the depletion region, at p-n junction, of the order of 3×10^5 V/cm. An electric field of such high magnitude exerts a large force on the valence electrons of the atom, tending to separate them from their respective nuclei. Actual breaking of the covalent bonds occurs when the electric field intensity becomes more than $3{\times}10^5$ V / cm. Hence, electron-hole pairs are generated in large numbers, and a sudden increase of current is observed. If a limiting resistance in the circuit does not prevent the current from increasing to high value, the diode may be destroyed because of excessive heating at the junction. In zener breakdown, the value of breakdown voltage decreases as p-n junction temperature increases, thus such diodes have negative temperature coefficient.

2.7.2 Avalanche Breakdown

As seen earlier, the applied reverse bias causes a small reverse current I_0 to flow in the device. This is due to movement of minority charge particles, viz. electrons from the p-material and holes from the n-material. The polarity of reverse bias voltage is such that only the minority charge particles are able to cross the p-n junction, while the majority charge particles move away from the junction. As the applied reverse bias voltage becomes larger, the minority charge carriers increasingly accelerate. There are collisions between these particles and electrons involved in the covalent bonds of the crystal structure.

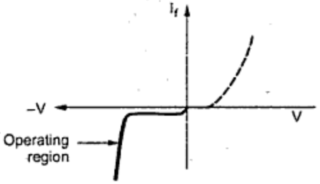
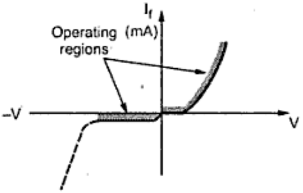
If the applied voltage is such that the travelling electrons do not have high velocity, then the collisions take some energy away from them, altering their velocity. If the applied voltage is increased, the velocity and hence the kinetic energy $(\text{K.E.} = \frac{1}{2}\text{mV}^2)$ of electron increases. If such an electron dashes against an electron involved in covalent bond, then the collision gives bond-valence electron enough energy to enable it to break its covalent bond. Thus, one electron by collision creates an electron-hole pair. These secondary particles are also accelerated and participate in collisions that generate new electron-hole pairs. This phenomenon is known as **carrier multiplication**. Electron-hole pairs are generated so quickly and in such large number that there is an apparent avalanche or self - sustained multiplication process. At this stage junction is said to be in breakdown and current starts increasing rapidly. **To limit such current below I_{Zmax}, current limiting resistor is necessary.**

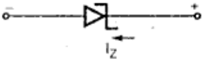
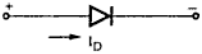
Zener diodes having zener voltage above 6 V exhibit avalanche breakdown and such diodes have positive temperature coefficient. The value of breakdown voltage increases as p-n junction temperature increases.

2.7.3 Comparison of Breakdown Mechanisms

	Zener Breakdown	Avalanche Breakdown
1.	Breaking of covalent bonds is due to intense electric field across the narrow depletion region. This generates large number of free electrons to cause breakdown.	Breaking of covalent bonds is due to collision of accelerated charge carriers having large velocities and kinetic energy with adjacent atoms. The process is called carrier multiplication.
2.	This occurs for zener diodes with V_Z less than 6 V.	This occurs for zener diodes with V_Z greater than 6 V.
3.	The temperature coefficient is negative.	The temperature coefficient is positive.
4.	The breakdown voltage decreases as junction temperature increases.	The breakdown voltage increases as the junction temperature increases.
5.	The V-I characteristics is very sharp in breakdown region.	The V-I characteristics is not as sharp as zener breakdown in breakdown region.

2.8 Comparison of Zener Diode and p-n Junction Diode

No.	Zener diode	P-N junction diode
1.	Operated in reverse breakdown condition.	Operated in forward biased condition and never operated in reverse breakdown condition.
2.	The characteristics lies in third quadrant.  	The characteristics lies in first quadrant. 
3.	Dynamic zener resistance is very small in reverse breakdown condition.	The diode resistance in reverse biased condition is very high.

4.	Zener diode symbol is,  	The p-n junction diode symbol is, 
5.	The conduction in zener is opposite to that of arrow in the symbol, as operated in breakdown region.	The conduction when forward biased is in same direction as that of arrow in the symbol, when forward biased.
6.	The power dissipation capability is very high.	The power dissipation capability is very low compared to zener diodes.
7.	Applications of zener diode are voltage regulator, protection circuits, voltage limiters etc.	Applications of p-n junction diode are rectifiers, voltage multipliers, clippers, clampers and many electronic devices.

2.9 Applications of Zener Diode

The various applications of zener diode are,

1. As a voltage regulating element in voltage regulators.
2. In various protection circuits.
3. In zener limiters i.e. clipping circuits which are used to clipp off the unwanted portion of the voltage waveform.

2.10 Regulated Power Supply

A typical d.c. regulated power supply consists of various stages. The Fig. 2.10 shows the block diagram of a typical d.c. regulated power supply, consisting of various circuits. The nature of voltages at various points is also shown in the Fig. 2.10.

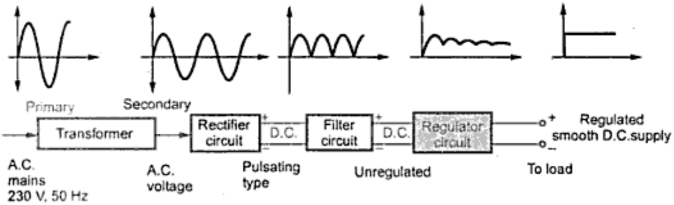

Primary
Secondary
Transformer
Rectifier circuit
D.C.
Filter circuit
D.C.
Regulator circuit
+
–
Regulated smooth D.C.supply
A.C. mains 230 V, 50 Hz
A.C. voltage
Pulsating type
Unregulated
To load

Fig. 2.10 A typical regulated power supply

The a.c. voltage (230 V, 50 Hz) is connected to the primary of the transformer. The transformer steps down the a.c. voltage, to the level required for the desired d.c. output. Thus, with suitable turns ratio we get desired a.c. secondary voltage. The rectifier circuit converts this a.c. voltage into a pulsating d.c. voltage. A pulsating d.c. voltage means a unidirectional voltage containing large varying component called ripple in it. The filter circuit is used after a rectifier circuit, which reduces the ripple content in the pulsating d.c. and tries to make it smoother. Still then the filter output contains some ripple. This voltage is called unregulated d.c. voltage. A circuit used after the filter is a regulator circuit which not only makes the d.c. voltage smooth and almost ripple free but it also keeps the d.c. output voltage constant though input d.c. voltage varies under certain conditions. It keeps the output voltage constant under variable load conditions, as well. The output of a regulator is called d.c. supply, to which the load can be connected. Now a days, complete regulator circuits are available in the integrated circuit (IC) form.

> **Key Point :** *Thus a voltage regulator circuit is the one which is designed to keep the output voltage of a power supply nearly constant, under varying input voltage conditions and varying load conditions.*

2.11 Zener Diode as a Shunt Regulator

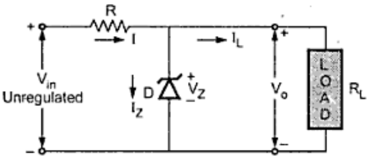


Fig. 2.11 Zener diode as a shunt regulator

The simplest shunt voltage regulator circuit uses a zener diode, to regulate the load voltage. The Fig. 2.11 shows the arrangement of zener diode in a regulator circuit.

To understand the working of the circuit, let us revise the V-I characteristics of a zener diode, as shown in the Fig. 2.12.

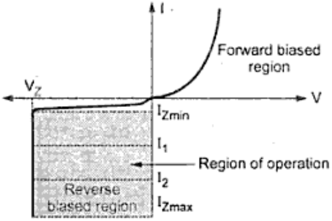


Fig. 2.12 V-I characteristics of zener diode

The zener diode is used in its reverse biased region. Under reverse biased condition, the current through the diode is very small of the order of few μA, upto certain limit. When the sufficient reverse bias is applied, electrical breakdown of the zener diode occurs. The large current flows through the zener diode. Such a breakdown occurs at a voltage called **zener voltage** V_Z. Under this condition, whatever may be the current, the voltage across the zener is constant equal to V_Z. The large current due to breakdown is limited by connecting the resistance in the circuit.

As the voltage across the zener diode remains constant equal to V_Z, it is connected across the load and hence the load voltage V_o is equal to the zener voltage V_Z. Thus zener diode acts as an ideal voltage source which maintains a constant load voltage, independent of the current.

2.11.1 Regulation with Varying Input Voltage

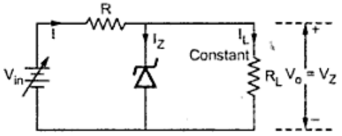


Fig. 2.13 Varying input condition

The Fig. 2.13 shows a zener regulator under varying input voltage condition.

It can be seen that the output is

$$V_o = V_Z \text{ is constant.}$$

$$\therefore \quad I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{constant}$$

$$\text{And } I = I_Z + I_L$$

Now if V_{in} increases, then the total current I increases. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L constant.

But as long as I_Z is between I_{Zmin} and I_{Zmax}, the V_Z i.e. output voltage V_o is constant. Thus the changes in input voltage get compensated and output is maintained constant.

Similarly if V_{in} decreases, then current I decreases. But to keep I_L constant, I_Z decreass. As long as I_Z is between I_{Zmax} and I_{Zmin}, the output voltage remains constant.

Process flowchart for zener regulator under varying V_{in} is,

V_{in} increases	→	$I = I_L + I_Z$ increases	→	I_L is constant (V_Z/R_L)	→	So I_Z increases ($I_Z = I - I_L$)	→	As long $I_Z < I_{Zmax}$, V_Z is constant i.e. output voltage is constant
V_{in} decreases	→	$I = I_L + I_Z$ decreases	→	I_L is constant (V_Z/R_L)	→	So I_Z decreases ($I_Z = I - I_L$)	→	As long $I_Z > I_{Zmin}$, V_Z is constant i.e. output voltage is constant

The maximum power dissipation for the zener diode is fixed and given by,

$$\boxed{P_D = V_Z I_{Z\,max}}$$

➡ **Example 2.3 :** *For a zener regulator shown in the Fig. 2.14, calculate the range of input voltage for which output will remain constant.*

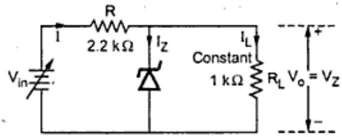


Fig. 2.14

$V_Z = 6.1V$, $I_{Zmin} = 2.5\ mA$, $I_{Zmax} = 25\ mA$, $r_Z = 0\ \Omega$

Solution : $R_L = 1\ \text{k}\Omega,\ V_Z = 6.1\ \text{V}$

$$\therefore \quad I_L = \frac{V_Z}{R_L} = \frac{6.1}{1\times10^3} = 6.1\ \text{mA constant}$$

For $V_{in(min)}$, $\quad I_Z = I_{Zmin} = 2.5\ \text{mA}$

$$\therefore \quad I = I_{Zmin} + I_L = 2.5 + 6.1 = 8.6\ \text{mA}$$

$$\therefore \quad V_{in(min)} = V_Z + IR = 6.1 + 8.6\times10^{-3}\times2.2\times10^3 = 25.02\ \text{V}$$

For $V_{in(max)}$, $\quad I_Z = I_{Zmax} = 25\ \text{mA}$

$$\therefore \quad I = I_{Zmax} + I_L = 25 + 6.1 = 31.1\ \text{mA}$$

$$\therefore \quad V_{in(max)} = V_Z + IR = 6.1 + 31.1\times10^{-3}\times2.2\times10^3 = 74.52\ \text{V}$$

Thus the range of input voltage is **25.02 V** to **74.52 V**, for which output will be constant.

➠ **Example 2.4 :** *Design a zener regulator for the following specifications*

Output voltage, $V_o = 5\ V$ *Input voltage,* $V_i = 12 \pm 3$ $I_{Zmin} = 10\ mA$

Load current, $I_L = 20\ mA$ *Zener wattage,* $P_Z = 500\ mW$

Solution : $V_{in(min)} = 12 - 3 = 9\ \text{V},\ V_{in(max)} = 12 + 3 = 15\ \text{V}$

$$I_L = 20\ \text{mA constant},\ V_o = V_Z = 5\ \text{V},\ P_Z = 500\ \text{mW}$$

Step 1 : The maximum power dissipation is corresponding to I_{Zmax}.

$$\therefore \quad P_Z(\text{given}) = V_Z\, I_{Zmax}$$

$$\therefore \quad 500\times10^{-3} = 5\, I_{Zmax}$$

$$\therefore \quad I_{Zmax} = \mathbf{100\ mA}$$

Step 2 : I_L is constant

For $V_{in(max)}$, $\quad I_Z = I_{Zmax}$

$$\therefore \quad I = I_L + I_{Zmax} = 20 + 100 = 120\ \text{mA}$$

$$\therefore \quad V_{in(max)} = V_Z + I\, R_{min}$$

$$\therefore \quad R_{min} = \frac{15-5}{120\times10^{-3}} = \mathbf{83.33\ \Omega}$$

When $R = R_{min}$, for $V_{in(max)}$ the current I will be at its maximum i.e. I_Z will be at its maximum.

Step 3 : To calculate R_{max}, I must be minimum i.e. I_Z must be minimum i.e. 10 mA.

$$\therefore \quad I = I_L + I_{Zmin} = 20 + 10 = 30 \text{ mA}$$

$$\therefore \quad V_{in(min)} = V_Z + I\,R_{max}$$

$$\therefore \quad R_{max} = \frac{9-5}{30\times10^{-3}} = \mathbf{133.33\ \Omega}$$

Thus R must be **greater than 83.33 Ω and less than 133.33 Ω** for proper regulating action.

2.11.2 Regulation with Varying Load

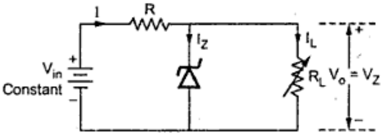


Fig. 2.15 Varying load condition

The Fig. 2.15 shows a zener regulator under varying load condition and constant input voltage.

The input voltage is constant while the load resistance R_L is variable. As V_{in} is constant and $V_o = V_Z$ is constant, then for constant R the current I is constant.

$$\therefore \quad I = \frac{V_{in} - V_Z}{R} \text{ constant } = I_L + I_Z$$

Now if R_L decreases so I_L increases, to keep I constant I_Z decreases. But as long as it is between I_{Zmin} and I_{Zmax}, output voltage V_o will be constant. Similarly if R_L increases so I_L decreases, to keep I constant I_Z increases. But as long as it is between I_{Zmin} and I_{Zmax}, output voltage V_o will be constant.

Process flowchart for zener regular under varying load is,

R_L increases I_L decreases	→	**$I = \frac{V_{in} - V_Z}{R}$ constant**	→	**$I_Z = I - I_L$ increases**	→	**As long $I_Z < I_{Zmax}$, V_Z is constant i.e. output voltage is constant.**
R_L decreases I_L increases	→	**$I = \frac{V_{in} - V_Z}{R}$ constant**	→	**$I_Z = I - I_L$ decreases**	→	**As long $I_Z > I_{Zmin}$, V_Z is constant i.e. output voltage is constant.**

Example 2.5 : *Determine the minimum and the maximum load currents for which the zener diode in Fig 2.16 will maintain regulation. What is the minimum R_L that can be used ? $V_Z = 10\,V$, $I_{Z\,min} = 5$ mA, and $I_{Z\,max} = 50$ mA. Assume $r_Z = 0\ \Omega$*

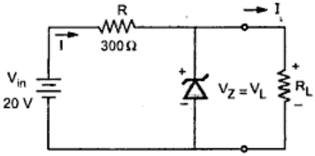


Fig. 2.16

Solution : $V_Z = 10$ V, $I_{Zmin} = 5$ mA, $I_{Zmax} = 25$ mA, $V_{in} = 20$ V

$$I = \frac{V_{in} - V_Z}{R} = \frac{20-10}{300} = 33.33 \text{ mA}$$

Now $I = I_L + I_Z = \text{constant}$

For $I_{L(min)}$, $I_Z = I_{Zmax}$

$$\therefore \quad I_{L(min)} = I - I_{Zmax} = 33.33 - 25 = 8.33 \text{ mA}$$

For $I_{L(max)}$, $I_Z = I_{Zmin}$

$$\therefore \quad I_{L(max)} = I - I_{Zmin} = 33.33 - 5 = 28.33 \text{ mA}$$

So load current can vary from 8.33 mA to 28.33 mA for which output will be constant.

The minimum R_L means maximum I_L hence

$$R_{L(min)} = \frac{V_Z}{I_{L\,(max)}} = \frac{10}{28.33 \times 10^{-3}} = 352.982\ \Omega$$

2.11.3 Circuit Protection

The zener diode can be employed to prevent overloading sensitive meter movements used in low range d.c. and a.c. voltmeters. A typical protective circuit is shown in Fig. 2.17.

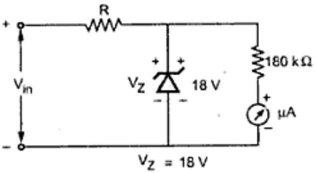


Fig. 2.17 Typical protective circuit using zener diode

Suppose that the meter movement used in the circuit requires 100 μA for full scale deflection. This is the maximum current that the movement can sustain. When the input voltage V_{in} exceeds the rated value, the zener diode goes into breakdown conditions. The zener voltage is 18 V which does not allow the current through meter to increase more than 100 μA, due to series resistance of 180 kΩ. Even though the input voltage may increase, the zener diode voltage remains constant which keeps the current through meter constant at 100 μA and thereby protects it.

2.11.4 Design of Zener Regulator with Varying Load and Varying Input Conditions

Let us see the design of zener regulator with varying load as well as varying input conditions.

Let V_{inmin} = Minimum value of input voltage

V_{inmax} = Maximum value of input voltage

I_{Lmax} = Maximum value of load current

I_{Lmin} = Minimum value of load current

I_{Zmax} = Maximum value of zener current

I_{Zmin} = Minimum value of zener current

V_o = V_Z = output voltage

The limiting values series resistance R for a given zener can be obtained as,

$$R_{max} = \frac{V_{inmin} - V_Z}{I_{Lmax} + I_{Zmin}} = \frac{V_{inmin} - V_o}{I_{Lmax} + I_{Zmin}} \quad \text{... (1)}$$

$$R_{min} = \frac{V_{inmax} - V_Z}{I_{Lmin} + I_{Zmax}} = \frac{V_{inmax} - V_o}{I_{Lmin} + I_{Zmax}} \quad \text{... (2)}$$

For any value of R between R_{max} and R_{min}, the circuit works successfully as a regulator.

If load current or input voltage is constant and not varying then its both maximum and minimum values must be treated as its constant value in the above equations, to obtain R_{max} and R_{min}. The I_{Lmin} value is generally treated to be zero.

To satisfy the equations (1) and (2), proper zener diode having I_{Zmin} and I_{Zmax} values, which can satisfy the required varying load conditions, must be used in the circuit.

Examples with Solutions

Example 2.6 : *Design and draw a zener regulator circuit to meet the following specifications :*

Load voltage = 8 V, Input voltage = 30 V

Load current = 0-50 mA, $I_{Zmin} = 5$ *mA,* $P_Z = 1$ *watts*

Solution : The input voltage is constant so

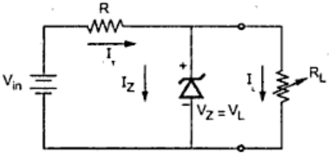


Fig. 2.18 Zener regulator with variable load

$$V_{inmin} = V_{inmax} = 30 \text{ V}$$

$$I_{Lmin} = 0 \text{ A}, \; I_{Lmax} = 50 \text{ mA}$$

$$I_{Zmax} = \frac{P_Z}{V_o} = \frac{1}{8} = 125 \text{ mA}$$

$$R_{Lmin} = \frac{V_o}{I_{Lmax}} = \frac{8}{50 \times 10^{-3}} = 160 \; \Omega$$

To find current limiting series resistance,

$$R_{max} = \frac{V_{inmin} - V_o}{I_{Lmax} + I_{Zmin}} = \frac{30-8}{50 \times 10^{-3} + 5 \times 10^{-3}} = \mathbf{400 \; \Omega}$$

$$R_{min} = \frac{V_{inmax} - V_o}{I_{Lmin} + I_{Zmax}} = \frac{30-8}{0 + 125 \times 10^{-3}} = \mathbf{176 \; \Omega}$$

For any value of R between 176 Ω to 400 Ω, the circuit will act as a regulator circuit.

Example 2.7 : *In a zener regulator, the input D.C. is 10 V ± 20%. The output requirements are 5 V, 20 mA. Assuming* $I_{Z\,min}$ *and* $I_{Z\,max}$ *as 5 mA and 80 mA. Design the Zener regulator.*

Solution : $V_o = 5$ V and $I_L = 20$ mA

$$\therefore \quad R_L = \frac{V_o}{I_L} = \frac{5}{20 \times 10^{-3}} = 250 \; \Omega$$

The maximum and minimum values of current limiting resistance can be obtained with,

$$I_{Lmax} = I_{Lmin} = 20 \text{ mA}$$

$$\therefore \quad R_{max} = \frac{V_{inmin} - V_o}{I_{Lmax} + I_{Zmin}}$$

Now

$$V_{inmin} = 10 - (0.2 \times 10) = 8 \text{ V}$$

$$V_{inmax} = 10 + (0.2 \times 10) = 12 \text{ V}$$

$$I_{Zmax} = 80 \text{ mA}$$

$$I_{Zmin} = 5 \text{ mA}$$

$$\therefore \quad R_{max} = \frac{8-5}{20\times10^{-3}+5\times10^{-3}} = \mathbf{120\ \Omega}$$

and

$$R_{min} = \frac{V_{inmax}-V_o}{I_{Lmin}+I_{Zmax}} = \frac{12-5}{20\times10^{-3}+80\times10^{-3}}$$

$$= \mathbf{70\ \Omega}$$

So series resistance R must be selected between 70 Ω to 120 Ω. So designed circuit is as shown in the Fig. 2.19.

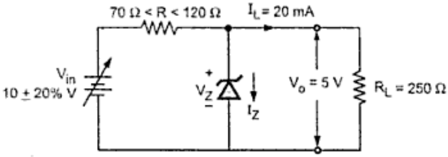


Fig. 2.19

Example 2.8 : *Design a voltage regulator using Zener diode to meet the following requirements.*

Unregulated i/p voltage : 20-30 volts.
Regulated o/p voltage : 10 volts.
Load current : 0-10 mA.
I_Z min : 2 mA.
I_Z max : 50 mA.

Draw the circuit diagram and insert the component values.

Solution : From the given specifications,

$$V_{inmax} = 30 \text{ V}, V_{inmin} = 20 \text{ V}, V_o = 10 \text{ V}$$

$$I_{Lmax} = 10 \text{ mA}, I_{Lmin} = 0 \text{ mA},$$

$$I_{Zmax} = 50 \text{ mA}, I_{Zmin} = 2 \text{ mA}$$

$$R_{Lmin} = \frac{V_o}{I_{Lmax}} = \frac{10}{10\times10^{-3}} = 1 \text{ k}\Omega$$

The current limiting series resistance is,

$$R_{max} = \frac{V_{inmin} - V_o}{I_{Lmax} + I_{Zmin}} = \frac{20-10}{10\times10^{-3}+2\times10^{-3}} = \mathbf{833.33\ \Omega}$$

$$R_{min} = \frac{V_{inmax} - V_o}{I_{Lmin} + I_{Zmax}} = \frac{30-10}{0+50\times10^{-3}} = \mathbf{400\ \Omega}$$

The designed circuit is shown in the Fig. 2.20.

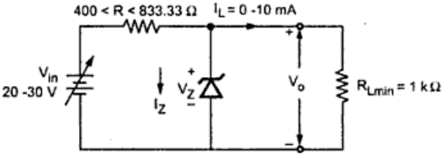


Fig. 2.20

Example 2.9 : *Find the voltage drop across 5 kΩ resistance shown in the Fig. 2.21.*

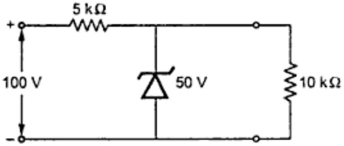


Fig. 2.21

(UPTU, Dec.-2002)

Solution : The circuit is zener voltage regulator. As long as the zener current is between I_{Zmax} and I_{Zmin}, the output voltage across 10 kΩ is $V_Z = 50$ V.

The input voltage is 100 V.

$\therefore$ Voltage drop across 5 kΩ = $V_i - V_Z = 100 - 50 =$ **50 V.**

Example 2.10 : *Find the range of I_L and R_L for the circuit shown if output voltage is to be maintained constant at 10 V.*

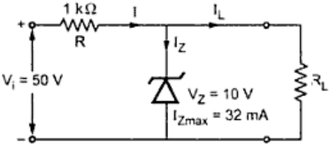


Fig. 2.22

(UPTU, May-2004)

Solution : From the circuit,

$$I = I_Z + I_L$$

From R,
$$I = \frac{V_i - V_Z}{R} = \frac{50-10}{1\times10^3} = 40 \text{ mA}$$

When I_L is minimum, I_Z is maximum and viceversa.

$$\therefore \quad I_L = I_{Zmax} + I_{Lmin} = I_{Zmin} + I_{Lmax}$$

$$\therefore \quad 40 = 32 + I_{Lmin} \quad \text{i.e.} \quad I_{Lmin} = \mathbf{8\ mA}$$

$$\therefore \quad R_{Lmax} = \frac{V_o}{I_{Lmin}} = \frac{10}{8\times10^{-3}} = \mathbf{1.25\ k\Omega}$$

And
$$I = I_{Zmin} + I_{Lmax}$$

Let
$$I_{Zmin} = 5 \text{ mA}$$

$$\therefore \quad I_{Lmax} = 40 - 5 = \mathbf{35\ mA}$$

$$\therefore \quad R_{Lmin} = \frac{V_o}{I_{Lmax}} = \frac{10}{35\times10^{-3}} = \mathbf{285.7142\ \Omega}$$

So range of I_L is 8 mA to 35 mA while range of R_L is 285.7142 Ω to 1.25 kΩ.

Example 2.11 : *The zener diode regulator circuit shown, has a fixed voltage drop of 12 V across zener as long as I_Z is between 20 mA to 200 mA. Find R_{in}, so that V_L remains 12 V and V_{DC} varies from 15 V to 19.5 V.*

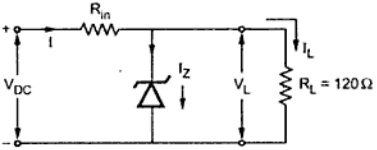


Fig. 2.23

(UPTU, Dec.-2003)

Solution : $I_{Zmax} = 200$ mA, $I_{Zmin} = 20$ mA, $V_L = 12$ V, $R_L = 120\ \Omega$.

$$I_L = \frac{V_L}{R_L} = \frac{12}{120} = 0.1 \text{ A} = 100 \text{ mA} \qquad \text{... constant}$$

$$I = I_L + I_Z$$

As I_L is constant, when I is I_{max}, I_Z is I_{Zmax} while when I is I_{min} , I_Z is I_{Zmin}.

$$\therefore \quad I_{max} = I_L + I_{Zmax} = 100 + 200 = 300 \text{ mA}$$

$$\text{and} \quad I_{min} = I_L + I_{Zmin} = 100 + 20 = 120 \text{ mA}$$

Now for minimum V_{DC}, the circuit should provide I_{Zmin} i.e. I_{min}.

$$\therefore \quad I_{min} = \frac{V_{DC}(\min) - V_L}{R_{in}}$$

$$\therefore \quad R_{in} = \frac{15-12}{120\times10^{-3}} = 25\ \Omega$$

Thus for V_{DC}(max),

$$I_{max} = \frac{V_{DC}(\max) - V_L}{R_{in}} = \frac{19.5-12}{25} = 300 \text{ mA}$$

Thus $R_{in} = 25\ \Omega$ is proper value.

➡ **Example 2.12 :** *For the circuit shown, calculate R_s if output is to be maintained at 6.2 V.*

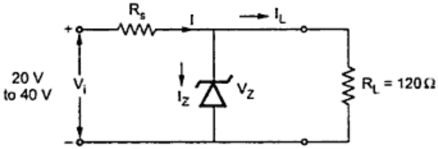


Fig. 2.24

(UPTU, May-2005)

Solution : The output $V_Z = 6.2$ V, $R_L = 120\ \Omega$

$$\therefore \quad I_L = \frac{V_Z}{R_L} = \frac{6.2}{120} = 51.667 \text{ mA}$$

$$\text{Now} \quad I_{max} = I_L + I_{Zmax}$$

$$\text{and} \quad I_{min} = I_L + I_{Zmin}$$

Let $I_{Zmax} = 200$ mA and $I_{Zmin} = 20$ mA

$$\therefore \quad I_{max} = 251.667 \text{ mA}, \qquad I_{min} = 71.667 \text{ mA}$$

For minimum input $V_i = 20$ V, the circuit must provide I_{Zmin}.

$$\therefore \quad I_{min} = \frac{V_i(\text{min}) - V_Z}{R_s}$$

$$\therefore \quad 71.667 \times 10^{-3} = \frac{20-6.2}{R_s}$$

$$\therefore \quad R_s = \mathbf{192.557\ \Omega}$$

For this R_s, check I_{max},

$$\therefore \quad I_{max} = \frac{V_i(\text{max}) - V_Z}{R_s} = \frac{40-6.2}{192.557} = 175.532 \text{ mA}$$

Thus zener current does not exceed its maximum value.

Example 2.13 : *The input voltage for the regulator shown varies from 35 V to 45 V, $V_Z = 20$ V, $r_Z = 5\ \Omega$, $I_L(min) = 0$ A, $I_L(max) = 100$ mA, $I_{Zmin} = 10$ mA, $I_{Zmax} = 400$ mA. Find the values of R and $P_Z(max)$.*

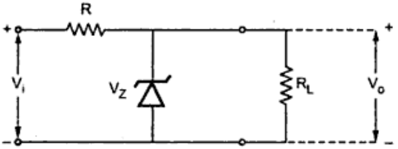


Fig. 2.25

(UPTU, Dec.-2005)

Solution : For the circuit,

$$I = I_L + I_Z$$

$$I_{min} = I_{Lmax} + I_{Zmin} = 100 + 10 = 110 \text{ mA}$$

$$I_{max} = I_{Lmin} + I_{Zmax} = 0 + 400 = 400 \text{ mA}$$

For minimum input voltage, the circuit must provide I_{Zmin}.

$$\therefore \quad I_{min} = \frac{V_{i\,(min)} - V_Z}{R}$$

$$\therefore \quad 110 \times 10^{-3} = \frac{35-20}{R}$$

$$\therefore \quad R = \mathbf{136.3636\ \Omega}$$

For this R, when V_i is maximum,

$$I = \frac{45-20}{136.3636} = 183.33 \text{ mA}$$

This does not exceed I_{Zmax}.

With $V_i = 45$ V and $I_L(\text{min}) = 0$ A then,

$$I = I_Z = 183.33 \text{ mA}$$

$$\therefore \quad P_{Z(\text{max})} = I_Z \times V_Z = 183.33 \times 10^{-3} \times 20 = \mathbf{3.66\ W}$$

Example 2.14 : *For the network shown determine V_L, V_R, I_Z and I_R.*

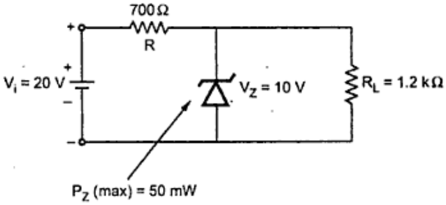


Fig. 2.26

(UPTU, May-2006)

Solution : The given network is zener shunt regulator.

$$\therefore \quad V_L = V_Z = \mathbf{10\ V}$$

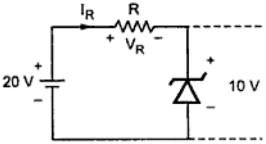


Fig. 2.26 (a)

Applying KVL to the loop,

$$-V_R - 10 + 20 = 0$$

$$\therefore \quad V_R = 10\text{V}$$

$$\therefore \quad I_R = \frac{V_R}{R} = \frac{10}{700} = \mathbf{14.285\ mA}$$

$$I_L = \frac{V_L}{R_L} = \frac{10}{1.2 \times 10^3} = \mathbf{8.333\ mA}$$

Now $\quad I_R = I_Z + I_L$

$$\therefore \quad I_Z = I_R - I_L = 14.285 - 8.333 = \mathbf{5.952\ mA}$$

Review Questions

1. *Draw and explain the characteristics of zener diode.*
2. *Draw and explain the equivalent circuit of zener diode.*
3. *Explain the two breakdown mechanisms in zener diodes.*
4. *Compare zener and avalanche breakdown.*
5. *Compare zener diode and p-n junction diode.*
6. *List the applications of zener diode.*
7. *Why Zener diode can be used as a regulator?*
8. *Explain how zener regulator works under varying input voltage conditions.*
9. *How zener regulator works under varying load conditions?*
10. *Design a zener regulator for the following specifications : Output voltage,* $V_0 = 5$ *V. Input voltage,* $V_i = 12 \pm 3$ *Load current* $I_L = 20$ *mA. Zener wattage* $P_Z = 500$ *mW.*
11. *A 24 V, 600 mW zener diode is used for providing a 24 V stabilized supply to a variable load. If the input voltage is 32 V, calculate*
    - *i) The value of series resistance required*
    - *ii) Diode current when the load is 1200 Ω.*

❑❑❑

3

Bipolar Junction Transistor

3.1 Introduction

In 1951, William Schockley invented the first junction transistor, a semiconductor device that can amplify electronic signals such as radio and television signals. It is essential ingredient of every electronic circuit; from the simplest amplifier or oscillator to the most elaborate digital computer. Thus a proper understanding of transistor is very important.

Before transistor, the amplification was achieved by using vaccum tubes as an amplifier. Now-a-days vaccum tubes are replaced by transistors because of following advantages of transistors.

- Low operating voltage
- Higher efficiency
- Small size and ruggedness and
- Does not require any filament power

Transistor is a three terminal device : base, emitter and collector, can be operated in three configurations common base, common emitter and common collector. According to configuration it can be used for voltage as well as current amplification. The input signal of a small amplitude is applied at the base to get the magnified output signal at the collector. This provides an amplification of the signal. The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance. This concept of transfer of resistance has given the name TRANSfer-resISTOR (TRANSISTOR).

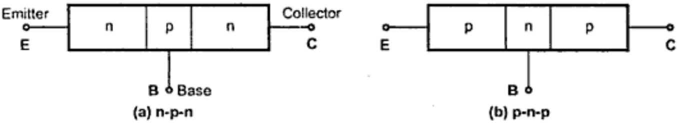
There are two types of transistors : **Unipolar junction transistor** and **Bipolar junction transistor**. In unipolar transistor the current conduction is only due to one type of carriers, majority carriers. The current conduction in bipolar transistor is because of both the types of charge carriers, holes and electrons. Hence this is called **Bipolar junction transistor,** hereafter referred to as **BJT**.

The BJTs are of two types :

- n-p-n type
- p-n-p type

3.2 Basic Construction

When a transistor is formed by sandwiching a single p–region between two n-regions, as shown in the Fig. 3.1 (a), it is an n-p-n type transistor. The p-n-p type transistor has a single n-region between two p-regions, as shown in Fig. 3.1(b).

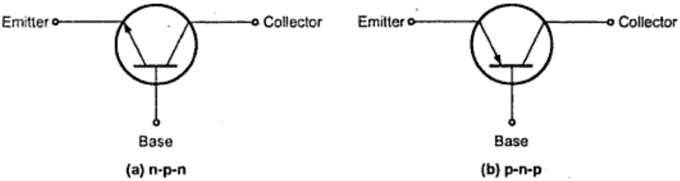


(a) n-p-n (b) p-n-p

Fig. 3.1 Bipolar transistor construction

The middle region of each transistor type is called the base of the transistor. This region is very thin and lightly doped. The remaining two regions are called **emitter** and **collector**. The emitter and collector are heavily doped. But the doping level in emitter is slightly greater than that of collector and the collector region-area is slightly more than that of emitter.

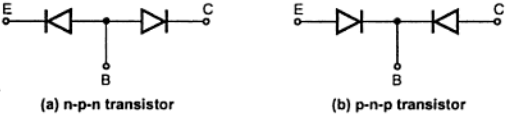
Fig. 3.2 (a) and (b) shows the symbols of npn and pnp transistors.



(a) n-p-n (b) p-n-p

Fig. 3.2 Standard transistor symbols

A transistor has two p-n junctions. One junction is between the emitter and the base, and is called the **emitter base junction,** or simply the **emitter junction** J_E. The other junction is between the base and the collector, and is called **collector-base junction,** or simply **collector junction** J_C. Thus transistor is like two pn junction diodes connected back-to-back as shown in the Fig. 3.3 (a) and (b).



(a) n-p-n transistor (b) p-n-p transistor

Fig. 3.3 Two-diode transistor analogy

However, we cannot replace transistor by back to back connected diodes because of the following reasons :

1. *Relative doping levels in the base, emitter and collector junctions must be satisfied to work that device as a transistor. Two normal p-n junction diodes can not satisfy this requirement.*
2. *In a transistor, emitter to base junction is forward biased while base to collector junction is reversed biased. But due to* ***diffusion process*** *almost entire emitter current reaches to collector and base current is negligibly small. Thus due to diffusion, device works as a transistor. While in back to back connected diodes there are two separate diodes, one forward biased and one reverse biased and diffusion can not take place. Thus maximum series current which can flow is reverse saturation current of a reverse biased diode. Hence the combination of back to back connected diodes can not be used as transistor.*

Another important point is that, the emitter area in the transistor is considerably smaller than the collector area. This is because the collector region has to handle more power than the emitter and more surface area is required for heat dissipation.

3.3 Transistor Action

3.3.1 Unbiased Transistor

An unbiased transistor means a transistor with no external voltage (biasing) is applied. Obviously, there will be no current flowing from any of the transistor leads. Since transistor is like two pn junction diodes connected back to back, there are depletion regions at both the junctions, emitter junction and collector junction, as shown in the Fig. 3.4.

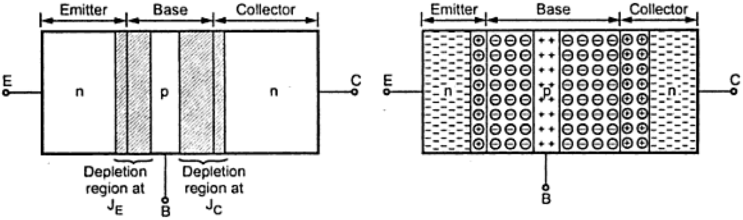


Fig. 3.4 Unbiased npn transistor

During diffusion process, depletion region penetrates more deeply into the lightly doped side in order to include an equal number of impurity atoms in the each side of the junction. As shown in the Fig. 3.4, depletion region at emitter junction penetrates less in the heavily doped emitter and extends more in the base region. Similarly, depletion region at collector junction penetrates less in the heavily doped collector and extends more in the base region. As collector is slightly less doped than the emitter, the depletion layer width at the collector junction is more than the depletion layer width at the emitter junction.

3.3.2 Biased Transistor

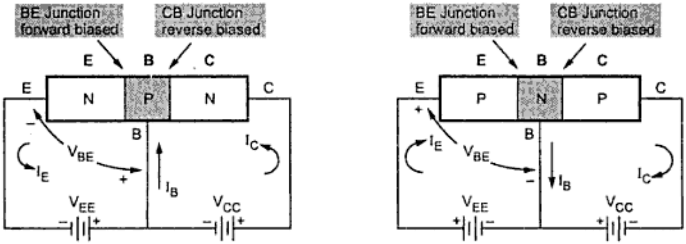
In order to operate transistor properly as an amplifier, it is necessary to correctly bias the two pn junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions, viz.

1) *Active region* 2) *Cut-off region* and 3) *Saturation region.*

Region	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

To bias the transistor in its active region, the emitter base junction is forward biased, while the collector-base junction in reverse-biased as shown in Fig. 3.5.

The Fig. 3.5 show the circuit connections for active region for both npn and pnp transistors.


BE Junction forward biased
CB Junction reverse biased
E
B
C
E
N
P
N
C
B
V_{BE}
I_E
I_B
I_C
V_{EE}
V_{CC}
BE Junction forward biased
CB Junction reverse biased
E
B
C
E
P
N
P
C
B
I_E
V_{BE}
I_B
I_C
V_{EE}
V_{CC}

(a) npn (b) pnp

Fig. 3.5 Transistor forward-reverse bias

The externally applied bias voltages are V_{EE} and V_{CC}, as shown in Fig. 3.5, which bias the transistor in its active region. The operation of the pnp is the same as for the npn except that the roles of the electrons and holes, the bias voltage polarities, and the current directions are all reversed. Note that in both cases the base-emitter (J_E) junction is forward-biased and the collector-base junction (J_C) is reversed biased. With these biasing conditions, what happens inside the transistor, is discussed in the next section.

3.3.3 Working of NPN Transistor

Let us consider the npn transistor for our discussion. The base to emitter junction is forward biased by the dc source V_{EE}. Thus, the depletion region at this junction is reduced. The collector to base junction is reverse biased, increasing depletion region at collector to base junction as shown in Fig. 3.6.

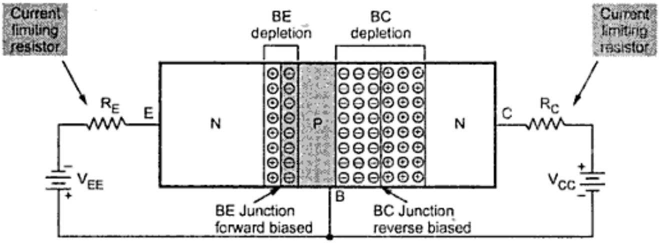

Current limiting resistor
BE depletion
BC depletion
Current limiting resistor
R_E
E
N
P
N
C
R_C
V_{EE}
V_{CC}
B
BE Junction forward biased
BC Junction reverse biased

Fig. 3.6 Internal effect of forward biased EB junction and reverse biased CB junction

The forward biased EB junction causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the p-type base, they tend to combine with holes in p-region (base).

We know that, the base region is very thin and lightly doped. The light doping means that the free electrons have a long lifetime in the base region. The very thin base region means that the free electrons have only a short distance to go to reach the collector. For these two reasons, very few of the electrons injected into the base from the emitter recombine with holes to constitute base current, I_B (Refer Fig. 3.7) and the remaining large number of electrons cross the base region and move through the collector region to the positive terminal of the external dc source as shown in Fig. 3.8.

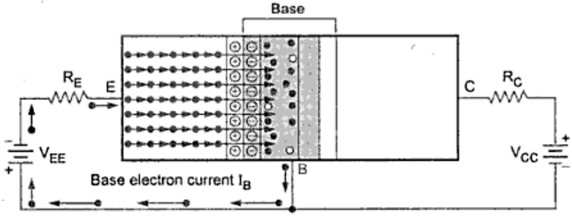

Base
R_E
E
C
R_C
V_{EE}
V_{CC}
B
Base electron current I_B

Fig. 3.7 Electron flow across emitter-base junction

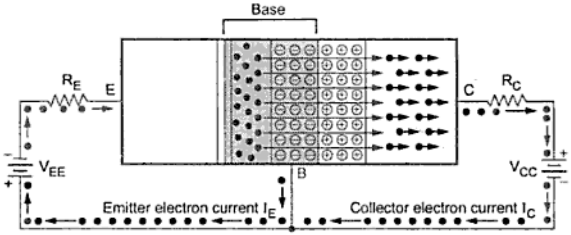

Base
R_E
E
C
R_C
V_{EE}
V_{CC}
B
Emitter electron current I_E
Collector electron current I_C

Fig. 3.8 Electron flow across base-collector junction

This constitutes collector current I_C. Thus the electron flow constitutes the dominant current in an npn transistor. Since, most of the electrons from emitter flow in the collector circuit and very few combine with holes in the base. Thus, the collector current is larger than the base current.

3.3.4 Working of PNP Transistor

The pnp transistor has its bias voltages V_{EE} and V_{CC} reversed from those in the npn transistor. This is necessary to forward-bias the emitter-base junction and reverse-bias the collector base junction. The forward biased EB junction causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E. As these holes flow through the n-type base, they tend to combine with electrons in n-region (base). As the base is very thin and lightly doped, very few of the holes injected into the base from the emitter recombine with electrons to constitute base current, I_B, as shown in the Fig. 3.10.

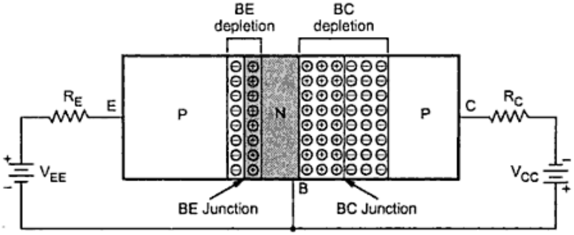

BE depletion
BC depletion
R_E
E
P
N
P
C
R_C
V_{EE}
V_{CC}
B
BE Junction
BC Junction

Fig. 3.9 Internal effect of forward biased EB junction and reverse biased CB junction

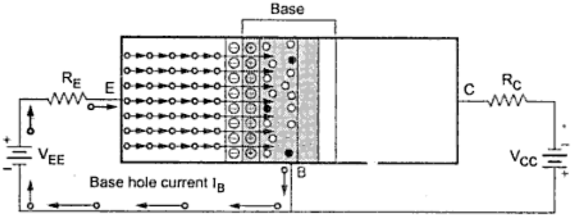


Fig. 3.10 Hole flow across base emitter junction

The remaining large number of holes cross the depletion region and move through the collector region to the negative terminal of the external dc source, as shown in Fig. 3.11. This constitutes collector current I_C. Thus the hole flow consistutes the dominant current in an pnp transistor.

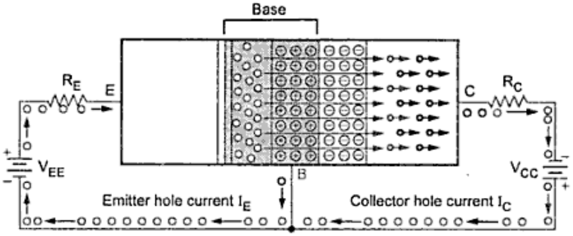


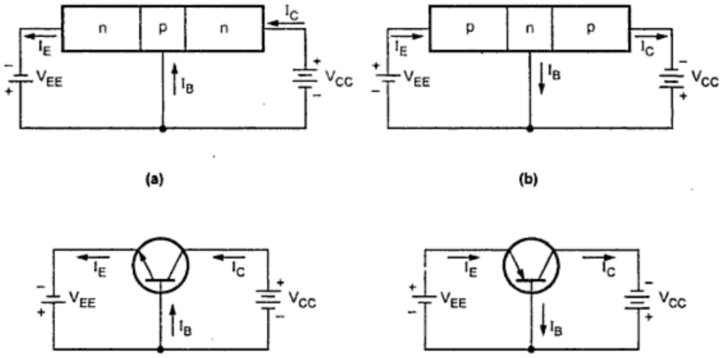
Fig. 3.11 Hole flow across base-collector junction

Highly doped emitter ensures that the emitter current consists almost entirely of holes in a pnp transistor and almost entirely of electrons in a npn transistor. Such a situation is desired since the current which results from electrons (in case of pnp transistor) or from holes (in case of npn transistor) crossing the emitter junction from base to emitter does not contribute carriers which can reach the collector.

3.3.5 Transistor Currents

The directions of conventional currents in an npn transistor are as shown in Fig. 3.12 (a) and Fig. 3.12 (c) and those for a pnp are shown in Fig. 3.12 (b) and 3.12 (d). Figures show the conventional currents using the schematic symbols of npn and pnp transistors, respectively. It can be noticed that the arrow at the emitter of the transistor's symbol points in the direction of conventional current.

Let us consider pnp transistor. The current flowing into the emitter terminal is referred to as the emitter current and identified as I_E. The currents flowing out of the collector and base terminals are referred to as collector current and base current, respectively. The collector current is identified as I_C and base current as I_B.



(a) **(b)**

(c) **(d)**

Fig. 3.12 Transistor conventional current directions

We have seen, for an n–p–n transistor, electrons are injected into the base. These electrons constitute the emitter current, I_E. For sake of explanation, assume that 100 electrons are injected into the base region. Since the base is very thin, very few of them, say 2 in number, recombine with holes. This constitutes the base current, I_B. The remaining electrons, 98 in this case, cross the base-collector reverse biased p-n junction and appear on the collector side, constituting the collector current I_C. Thus we see that the emitter current I_E is always equal to the sum of base and collector currents, I_B and I_C respectively. This is true for both types of transistor. Hence

$$I_E = I_B + I_C$$

As we have seen, the base current is a very small fraction of emitter current, 2% or even less, the emitter current and collector current are nearly equal.

$$I_C \approx I_E \qquad \because I_B << I_C$$

Example 3.1 : *In a certain transistor, the emitter current is 1.02 times as large as the collector current. If the emitter current is 12 mA, find the base current.*

Solution : Given : $I_E = 12$ mA $I_E = 1.02\ I_C$

$$\therefore \quad 1.02\ I_C = 12 \times 10^{-3}$$

$$I_C = 11.765 \text{ mA}$$

$$I_E = I_B + I_C$$

$$\therefore \quad I_B = I_E - I_C = (12 - 11.765) \text{ mA}$$

$$\therefore \quad I_B = 0.235 \text{ mA} = 235\ \mu\text{A}$$

Actually, there is one more current component flows inside the transistor, called the reverse saturation current (I_{CBO}). This reverse saturation current flows across the reverse biased collector junction when emitter is open circuited. Hence, the collector current is constituted by two components, namely the curent due to injected charge carriers from emitter to collector crossing the base and current due to reverse saturation current.

3.4 BJT Configurations

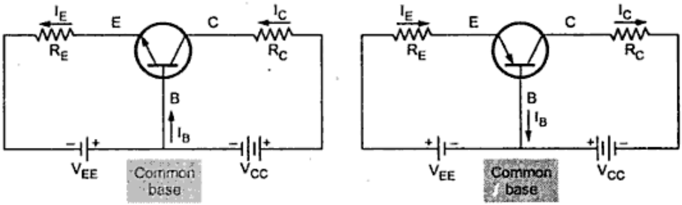
In the previous section we have seen that base is taken as common point/terminal to connect transistor in common-base configuration. Similarly, we can use emitter and collector as a common points/terminals to connect transistor in common emitter and common collector configurations, respectively. Thus, the transistor can be connected in a circuit in the following three configurations.

1. Common base configuration
2. Common emitter configuration
3. Common collector configuration

Note 1 : Regardless of circuit configuration, the base emitter junction is always forward biased while the collector-base junction is always reverse biased, to operate transistor in active region.

3.4.1 Common Base Configuration

As shown in Fig. 3.13, in this configuration input is applied between emitter and base and output is taken from the collector and base. Here, base of the transistor is common to



(a) (b)

Fig. 3.13 Common base configuration

both input and output circuits and hence the name common base configuration. Common base configurations for both npn and pnp transistors are shown in Fig. 3.13 (a) and 3.13 (b), respectively.

3.4.1.1 Common Base Characteristics

To understand complete electrical behaviour of a transistor it is necessary to study the interrelation of the various currents and voltages. These relationships can be plotted graphically which are commonly known as the **characteristics of transistor.** The most important characteristics of transistor in any configuration are input and output characteristics.

A) Input Characteristics :

It is the curve between input current I_E (emitter current) and input voltage V_{EB} (emitter-base voltage) at constant collector-base voltage V_{CB}. The emitter current is taken along Y-axis and emitter base voltage along X-axis. Fig. 3.14 shows the input characteristics of a typical transistor in common-base configuration.

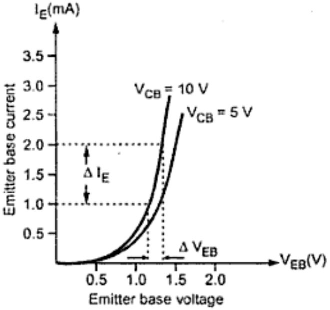


Fig. 3.14 Input characteristics of transistor in CB configuration

From this characteristics we can observe the following important points :

1. After the cut-in voltage (barrier potential, normally 0.7 V for silicon and 0.3 V for Germanium), the emitter current (I_E) increases rapidly with small increase in emitter-base voltage (V_{EB}). It means that input resistance is very small. Because input resistance is a ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}), this resistance is also known as the dynamic input resistance of the transistor in CB configuration.

$$r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$

2. It can be observed that there is slight increase in emitter current (I_E) with increase in V_{CB}. This is due to change in the width of the depletion region in the base region under the reverse biased condition.

As shown in Fig. 3.15, when reverse bias voltage V_{CB} increases, the width of depletion region also increases, which reduces the electrical base width. Due to reduction of the electrical base width, now there are more charge particles per unit area. In other words, due to reduction of the electrical base width, concentration of the charge gradient increases in the base region. This increase in concentration of charge carriers causes more diffusion of electrons from n-type emitter to p-type base increasing emitter current slightly.

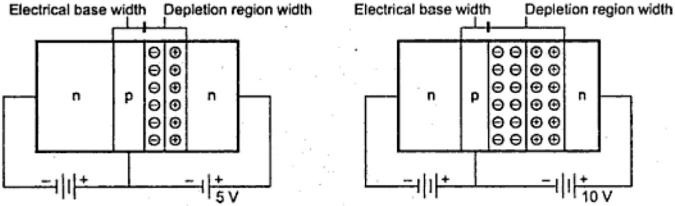


Fig. 3.15 Change in base and depletion region width with change in reverse biased voltage

Early Effect : As shown in Fig. 3.15, when reverse bias voltage V_{CB} increases, the width of depletion region also increases, which reduces the electrical base width. This effect is called as **'Early Effect'** or **'Base Width Modulation'**.

B) Output Characteristics :

It is the curve between collector current I_C and collector base voltage V_{CB} at constant emitter current I_E. The collector current is taken along Y-axis and collector-base voltage magnitude along X-axis. Fig. 3.16 shows the output characteristics of a typical transistor in common base configuration. (See Fig. 3.16 on next page)

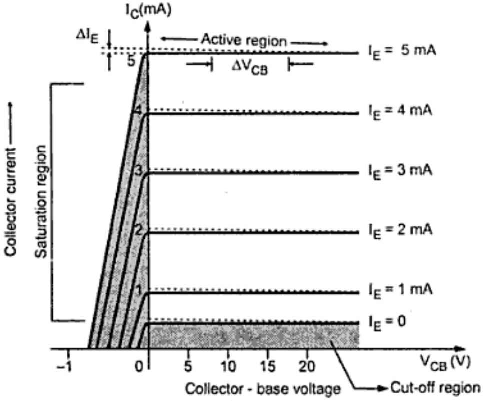


Fig. 3.16 CB output characteristics

From this characteristics we observe following points :

1. The output characteristics has three basic regions : active, cutoff and saturation.

State	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

Table 3.1

2. For the operation in the active region, the emitter base junction is forward biased while collector base junction is reverse biased. In this region collector current I_C is approximately equal to the emitter current (I_E) and transistor works as an amplifier.
3. If the emitter current is zero, the collector current is simply I_{CBO} as shown in Fig. 3.17.

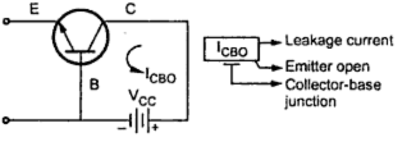


Fig. 3.17 CB configuration with emitter open

This current is so small in magnitude compared to the vertical scale of I_C that it virtually appears on the same horizontal line as $I_C = 0$. However, in Fig. 3.17, this has been shown on the exaggerated scale for understanding purpose. The region below the curve $I_E = 0$ is known as cut-off region, where the collector current is nearly zero and the collector-base and emitter-base junctions of a transistor are reverse biased.

4. The saturation region is that region of the characteristics which is to the left of $V_{CB} = 0$ V. In the Fig. 3.16, the horizontal scale is expanded to clearly show the change in characteristics in the region. Note the exponential increase in collector current as the voltage V_{CB} increases towards 0 V, in this saturation region, the emitter-base and collector-base junctions are both forward biased.
5. In the active region, the collector current is essentially almost constant, and the graph is almost parallel to x-axis. The collector current I_C is almost independent on collector base voltage V_{CB} and the transistor can be said to work as constant-current source. This provides very high dynamic output resistance. Dynamic output resistance is the ratio of change in collector base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current (I_E)

$$R_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}$$

6. As I_E increases I_C also increases. Thus, I_C depends upon input current I_E but not on collector voltage. Hence, input current controls output current. Since transistor requires some current to drive it, it is called current operating device.
7. In the active region, the collector-base junction is reversed-biased. For every transistor there is limit on the maximum value for this reverse bias voltage.

Punch-Through Effect

As shown in Fig. 3.18, collector base junction is reverse biased. As mentioned earlier, this reverse bias voltage must be within the maximum safe limits specified by the manufacturer. If this maximum limit is exceeded, transistor breakdown occurs (same as the diode breakdown). Fig. 3.18 shows this breakdown condition.

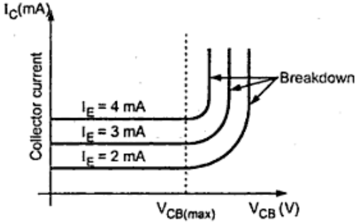
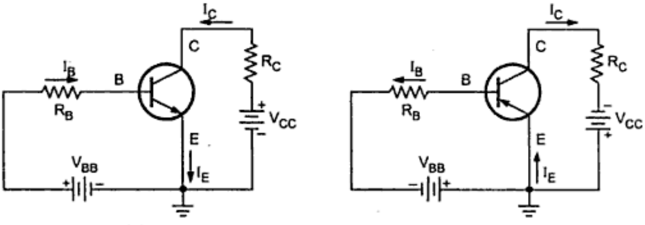


Fig. 3.18 Output characteristics of a transistor showing maximum collector base voltage rating in CB configuration

The curves shown at the right side of dotted line ($V_{CB\,max}$ is exceeded) represent the breakdown condition. When collector to base voltage increases, width of the depletion region at the junction increases. Therefore, when V_{CB} increases above the $V_{CB\,max}$, increase in depletion region is such that it penetrates into the base until it makes contact with emitter-base depletion region. This condition is called **'punch-through'** or **'reach through'** effect. When this situation occurs, breakdown occurs. i.e. large collector current flows which destroys the transistor. To avoid this punch-through effect V_{CB} should always be kept below the maximum safe limit specified by the manufacturer.

3.4.2 Common-Emitter Configuration

As shown in Fig. 3.19, in this configuration input is applied between base and emitter, and output is taken from collector and emitter. Here, emitter of the transistor is common to both, input and output circuits, and hence the name common emitter configuration. Common emitter configurations for both npn and pnp transistors are shown in Fig. 3.19 (a) and 3.19 (b), respectively.



(a) npn

(b) pnp

Fig. 3.19 Common emitter configurations

As shown in Fig. 3.19 the bias voltage V_{BB} forward biases the base-emitter junction and V_{CC} is used to reverse bias the collector-base junction.

The Fig. 3.20 shows the input and output voltages and currents for the common-emitter configuration.

The input voltage in the CE configuration is the base-emitter voltage, and the output voltage is the collector-emitter voltage. The input current is I_B and the output current is I_C.

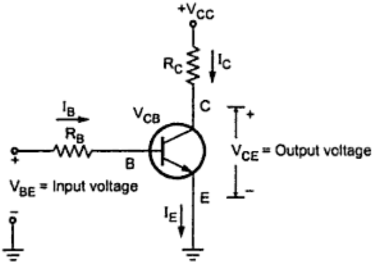


Fig. 3.20 Transistor currents and voltages in common emitter configuration

3.4.2.1 Common Emitter Characteristics

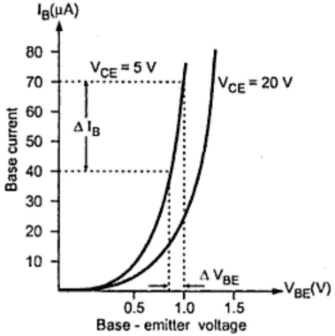


Fig. 3.21 Input characteristics of the transistor in CE configuration

A) Input Characteristics :

It is the curve between input current I_B (base current) and input voltage V_{BE} (base-emitter voltage) at constant collector-emitter voltage, V_{CE}. The base current is taken along Y-axis and base emitter voltage V_{BE} is taken along X-axis. Fig. 3.21 shows the input characteristics of a typical transistor in common-emitter configuration.

From this characteristics we observe the following important points :

1. As the input to a transistor in the CE configuration is between the base-to-emitter junction, the CE input characteristics resembles a family of forward-biased diode curves. A typical set of CE input characteristics for an n-p-n transistor is shown in Fig. 3.21.
2. After the cut-in voltage the base current (I_B) increases rapidly with small increase in base emitter voltage (V_{BE}). It means that dynamic input resistance is small in CE configuration. It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector emitter voltage V_{CE}. It is given by

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE=\text{ constant}}}$$

3. For a fixed value of V_{BE}, I_B decreases as V_{CE} is increased. A larger value of V_{CE} results in a large reverse bias at collector-base p-n junction. This increases the depletion region and reduces the effective width of the base. Hence, there are fewer recombinations in the base region, reducing the base current I_B.

B) Output Characteristics :

1. This characteristics shows the relation between the collector current I_C and collector voltage V_{CE}, for various fixed values of I_B. This characteristics is often called collector characteristics. A typical family of output characteristics for an n-p-n transistor in CE configuration is shown in Fig. 3.22.

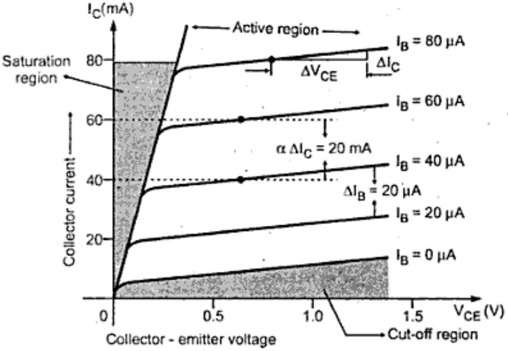


Fig. 3.22 Output characteristics of the transistor in CE configuration

2. The value of β_{dc} of the transistor can be found at any point on the characteristics by taking the ratio I_C to I_B at that point, i.e. $\beta_{dc} = \frac{I_C}{I_B}$. This is known as DC beta for the transistor. For a fixed value of V_{CE}, if we take the ratio of small change in I_C, ΔI_C to small change in I_B, ΔI_B, we get AC beta;

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{\Delta V_{CE=0}}$$

Generally dc and ac values of beta of the transistor are nearly equal.

3. From the output characteristics we can see that change in collector-emitter voltage (ΔV_{CE}) causes the little change in the collector current (ΔI_C) for constant base current I_B. Thus the output dynamic resistance is high in CE configuration.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant OR } \Delta I_B = 0}$$

4. The output characteristics of common emitter configuration consists of three regions : Active, Saturation, and Cut-off.

5. **Active region** : The region where the curves are approximately horizontal is the "active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increases. This causes depletion region to spread more in base than in collector, reducing the chances of recombinations in the base. This increases the value of α_{dc}. This early effect causes collector current to rise more sharply with increasing V_{CE} in the linear region of output characteristics of CE transistor.
6. **Saturation region** : If V_{CE} is reduced to a small value such as 0.2 V, then collector-base junction becomes forward biased, since the emitter base junction is already forward biased by 0.7 V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration is similar to forward characteristics of p-n junction diode. (considering silicon transistor). When both the junctions are forward biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of V_{CE}, designated $V_{CE(sat)}$, usually ranges between 0.1 V to 0.3 V.
7. **Cut-off region** : When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}. The region below $I_B = 0$ is the cutoff region of operation for the transistor. In this region, both the junctions of the transistor are reverse biased.
8. In the active region, the collector base junction is reverse-biased. For every transistor there is limit on the maximum value for this reverse bias voltage. If this limit is exceeded as shown in Fig. 3.23, the breakdown occurs in the transistor. This effect is commonly known as **punch through effect.**

This large current may damage transistor. Hence, in practice, maximum collector emitter voltage rating, V_{CE} (max) should never be exceeded for the safe operation of the transistor.

Junction Voltages :

In different conditions such as active, saturation and cutoff there are different junction voltages. The junction voltages for a typical npn transistor at 25 °C are given in the Table 3.2.

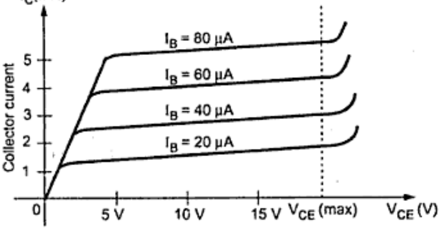


Fig. 3.23 Maximum collector-emitter voltage rating

Type	$V_{CE\,sat}$	$V_{BE\,sat}$	$V_{BE\,active}$	$V_{BE\,cutin}$	$V_{BE\,cutoff}$
Si	0.2	0.8	0.7	0.5	0.0
Ge	0.1	0.3	0.2	0.1	– 0.1

Table 3.2 Typical npn transistor junction voltages at 25 °C

The entries in the table are appropriate for an npn transistor. For pnp transistor the signs of all entries should be reversed.

3.4.2.2 Definition of α_{dc} and β_{dc}

α_{dc} : It is defined as the ratio of the collector current resulting from carrier injection to the total emitter current.

$$\therefore \qquad \alpha_{dc} = \alpha = \frac{I_C[INJ]}{I_E} \approx \frac{I_C}{I_E}$$

Since $I_C < I_E$ the value of α_{dc} is always less than unity. It ranges from 0.95 to 0.995. It represents the current gain in the CB configuration.

β_{dc} : It is defined as the ratio of the collector current to the base current.

$$\therefore \qquad \beta_{dc} = \beta = \frac{I_C}{I_B}$$

3.4.2.3 Relationship between α_{dc} and β_{dc}

We know that,

$$\beta_{dc} = \frac{I_C}{I_B} \qquad \text{and} \qquad \alpha_{dc} = \frac{I_C}{I_E}$$

We have, $I_E = I_C + I_B$ i.e. $I_B = I_E - I_C$

$$\beta_{dc} = \frac{I_C}{I_E - I_C} \qquad \because \; I_B = I_E - I_C$$

Dividing the numerator and denominator of R.H.S. of above equation by I_E, we get,

$$\beta_{dc} = \frac{I_C/I_E}{I_E/I_E - I_C/I_E}$$

$$\therefore \qquad \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} \qquad \because \; \alpha_{dc} = \frac{I_C}{I_E}$$

Dividing the R.H.S and L.H.S. by 1 + β_{dc} we get,

$$\frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\frac{\alpha_{dc}}{1-\alpha_{dc}}}{1+\beta_{dc}}$$

$$\frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\dfrac{\alpha_{dc}}{1-\alpha_{dc}}}{1+\dfrac{\alpha_{dc}}{1-\alpha_{dc}}} \qquad \because \quad \beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

$$\frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\dfrac{\alpha_{dc}}{1-\alpha_{dc}}}{\dfrac{1-\alpha_{dc}+\alpha_{dc}}{1-\alpha_{dc}}}$$

Cancelling common denominator terms we get,

$$\frac{\beta_{dc}}{1+\beta_{dc}} = \frac{\alpha_{dc}}{1-\alpha_{dc}+\alpha_{dc}} = \alpha_{dc}$$

$$\therefore \qquad \alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

Example 3.2 : *a) Find α_{dc} for each of the following values of β_{dc} = 50 and 190. b) Find β_{dc} for each of the following values of α_{dc} = 0.995 and 0.9765.*

Solution :

a) $$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

For $\beta_{dc} = 50, \quad \alpha_{dc} = \frac{50}{1+50} = \mathbf{0.9804}$

For $\beta_{dc} = 190, \quad \alpha_{dc} = \frac{190}{1+190} = \mathbf{0.9947}$

b) $$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

For $\alpha_{dc} = 0.995, \quad \beta_{dc} = \frac{0.995}{1-0.995} = \mathbf{199}$

For $\alpha_{dc} = 0.9765, \quad \beta_{dc} = \frac{0.9765}{1-0.9765} = \mathbf{41.55}$

Example 3.3 : *If the base current in a transistor is 20 µA when the emitter current is 6.4 mA, what are the values of α_{dc} and β_{dc} ? Also calculate the collector current.*

Solution : Given : $I_B = 20\ \mu A \quad I_E = 6.4$ mA

$$I_E = I_B + I_C = I_B + I_B\,\beta_{dc}$$

$$= I_B\,(1+\beta_{dc})$$

$$\beta_{dc} + 1 = \frac{I_E}{I_B} = \frac{6.4 \times 10^{-3}}{20 \times 10^{-6}} = 320$$

$$\therefore \qquad \beta_{dc} = \mathbf{319}$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{319}{1+319} = \mathbf{0.9968}$$

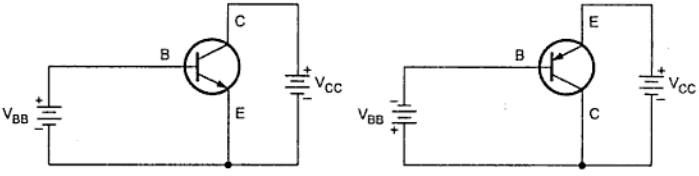
$$I_C = \beta_{dc}\ I_B = (319)\ (20\ \mu A) = 6380\ \mu A = \mathbf{6.38\ mA}$$

Also,

$$I_C = \alpha_{dc}\ I_E = (0.9968)\ (6.4\ mA) = \mathbf{6.379\ mA}$$

3.4.3 Common Collector Configuration

As shown in Fig. 3.24, in this configuration input is applied between base and collector, and output is taken from emitter and collector. Here, collector of the transistor is common to both input and output circuits, and hence the name common collector configuration. Common collector connections for both npn and pnp transistors are shown in Fig. 3.24 (a) and 3.24 (b), respectively.



(a) (b)

Fig. 3.24 Common collector configurations

It is important to note that collector is not at dc ground , but it is at ac ground because the V_{CC} *source has 0 resistance (ideally) to an ac signal. Taking this into consideration, we can very well say that collector is a common terminal between input and output for ac signal purposes.*

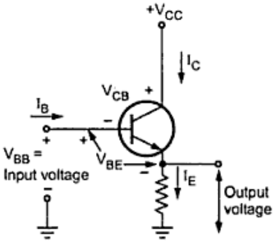


Fig. 3.25 Transistor currents and voltages in common collector configuration

The common collector configuration is same as the common emitter configuration, with the exception that the load resistance is in the emitter circuit rather than in the collector circuit and output is taken from emitter lead instead of the collector.

Fig. 3.25 shows the input and output voltages and currents for the common collector configuration.

The input voltage in the CC configuration is the base collector voltage, and the output voltage is the emitter-collector voltage. The input current is I_B and the output current is I_E.

Current gain in CC configuration

In CC configuration, I_B is the input current and the I_E is the output current. Now we are interested in knowing how the output current I_E is related with the input current I_B.

We have $$I_E = I_B + I_C = I_B + \beta I_B \qquad \text{... (1)}$$

$$\therefore \quad I_E = (1+\beta_{dc})\, I_B$$

$$\therefore \quad \frac{I_E}{I_B} = (1+\beta_{dc}) \qquad \text{... (2)}$$

Thus equation (2) shows that the dc current gain using CC configuration is $(1+\beta_{dc})$. Since β_{dc} is quite large compared to '1', we see that current gains of CE and CC are nearly same.

r_i and r_o in CC configuration :

In the common collector configuration, the junction at the input (collector-base) is in the reverse-biased condition, and the junction at the output (emitter-base) is in the forward biased. Hence this configuration has very high input resistance (r_i) and low output resistance (r_o).

Voltage and current gains in CC configuration :

As we know, in CC configuration base voltage (input) is kept always greater than the emitter voltage (output) to provide forward bias to base emitter junction, voltage gain provided by the CC configuration is always less than 1.

The current amplification factor in CC configuration is given by $(1+\beta_{dc})$. Thus the current gain provided by the CC is much larger than the current gain of CB configuration, but is nearly equal current gain of CE configuration.

The common collector configuration has very high input impedance and very low output impedance. Due to this it is commonly used for impedance matching. As its current gain is high and voltage gain is nearly unity it is also commonly used as a buffer.

3.4.4 Why CE Configuration is Widely used in Amplifier Circuits ?

The common-emitter configuration is widely used amongst three transistor configurations. The main reasons for the wide-spread use of this circuit arrangement are :

1. The CE configuration is the only configuration which provides both voltage gain as well as current gain greater than unity. In case of CB configuration current gain is less than unity and in case of CC configuration voltage gain is less than unity.

   The power gain is a product of voltage gain and current gain. CE configuration provides voltage gain nearly equal to voltage gain provided by CB configuration (voltage gain is maximum in CB) and current gain nearly equal to current gain provided CC configuration (current gain is maximum in CC). Thus the power gain of the CE amplifier is much greater than the power gain provided by the other two configurations (voltage gain in CC and current gain in CB are less than unity).

2. In a common emitter circuit, the ratio of output resistance to input resistance is small, may range from 10 Ω to 100 Ω. This makes configuration an ideal for coupling between various transistor stages. However, in other connections, the ratio of output resistance to input resistance is very large and hence coupling becomes highly inefficient due to large mismatch of resistance.

Note : Maximum power is transferred from stage 1 to stage 2, when output resistance of stage 1 is equal to the input resistance of stage 2.

3.4.5 Comparison of Transistor Configurations

Sr.No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1 kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1 MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	less than unity
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

Table 3.3

3.4.6 Leakage Current

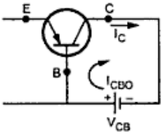


Fig. 3.26 Common base configuration with emitter-base junction open

Let us consider Fig. 3.26. Here, emitter is open circuited. Since the emitter is open, no carriers are injected from emitter into the base and emitter current is zero. Under this condition the collector base junction J_C acts as a reverse biased diode, and the collector current is equal to the reverse saturation current I_{CBO} even though emitter current is zero. Therefore, when emitter base junction is forward biased and collector base junction is reversed biased, the total collector current will be sum of two currents. One, the current due to injected carriers (α_{dc} I_E) and the other, I_{CBO}. Therefore, current I_C is given by

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad ...(3)$$

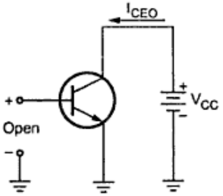


Fig. 3.27 Common emitter configuration with base open

The I_{CBO} is nothing but the I_{CO} (Reverse saturation current) for physical (a real, non idealized) transistor. It is also defined as the current when emitter current is zero. As I_{CBO} is defined for physical transistor, it constitutes the leakage current flowing around the junction and across the surfaces.

The leakage current in common-emitter configuration is larger than that in common-base configuration. I_{CEO} is the collector current which flows when base-emitter circuit is left open and collector–base junction is reverse biased, as indicated in Fig. 3.27.

The leakage current in common emitter configuration, I_{CEO} is given by

$$I_{CEO} = (1 + \beta_{dc}) I_{CBO}$$

The reverse current I_{CEO} is in the same direction as normal collector current through the transistor. The current I_{CEO} is reverse current and it is temperature sensitive. It increases with increase in temperature. Due to this, the collector current I_C will increase with temperature. This may create problems when the temperature increases. Hence thermal stability becomes essential for the common emitter configuration.

Although I_{CEO} is much greater than I_{CBO}, it is generally quite small compared to βI_B; and hence it is often neglected in many practical circuits. Neglecting I_{CEO}, we have,

$$I_C = \beta_{dc} I_B$$

➡ **Example 3.4 :** *In a certain transistor, 99.6 % of the carriers injected into the base cross the collector-base junction. If the leakage current is 5 μA and the collector current is 20 mA, calculate (i) the value of α_{dc} (ii) the emitter current.*

Solution : Given : $I_C = 0.996\ I_E$, $I_{CBO} = 5\ \mu A$, $I_C = 20$ mA

i) $$\alpha_{dc} = \frac{I_C}{i_E} = \mathbf{0.996}$$

ii) We know that, $$I_C = \alpha_{dc} I_E + I_{CBO}$$

∴ $$I_E = \frac{I_C - I_{CBO}}{\alpha_{dc}} = \frac{20\ mA - 5\mu A}{0.996} = \mathbf{20.07\ mA}$$

➠ **Example 3.5 :** *Calculate the values of collector current and base current for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 10\ \mu A$. The emitter current is measured as 8 mA.*

Solution : Given : $\alpha_{dc} = 0.99$, $I_{CBO} = 10\ \mu A$

$$I_E = 8\ mA$$

From equation $I_C = \alpha_{dc} I_E + I_{CBO}$

$$I_C = 0.99 \times 8\ mA + 10\mu A = \mathbf{7.93\ mA}$$

From equation $I_B = (1 - \alpha_{dc}) I_E - I_{CBO}$

$$I_B = (1 - 0.99) \times 8\ mA - 10\mu A = \mathbf{70\ \mu A}$$

➠ **Example 3.6 :** *Calculate the values of collector current and emitter current for a transistor with $\alpha_{dc} = 0.98$ and $I_{CBO} = 5\ \mu A$. The base current is measured as 100 μA.*

Solution : Given : $I_B = 100\ \mu A$, $\alpha_{dc} = 0.98$ and

$$I_{CBO} = 5\ \mu A$$

We know that, $I_B = (1 - \alpha_{dc}) I_E - I_{CBO}$

Thus $$I_E = \frac{I_B + I_{CBO}}{1 - \alpha_{dc}} = \frac{100\mu A + 5\mu A}{1 - 0.98} = \frac{105\mu A}{0.02} = \mathbf{5.25\ mA}$$

From equation $I_C = I_E - I_B$ we get,

$$I_C = 5.25\ mA - 100\ \mu A = \mathbf{5.15\ mA}$$

➠ **Example 3.7 :** *For a certain transistor, $\alpha_{dc} = 0.98$, $I_C = 5$ mA and $I_{CBO} = 10\ \mu A$. Find I_B.*

Solution : Given : $I_C = 5$ mA, $I_{CBO} = 10\ \mu A$, $\alpha_{dc} = 0.98$

We know that, $I_C = \alpha_{dc} I_E + I_{CBO}$

$$\therefore \quad I_E = \frac{I_C - I_{CBO}}{\alpha_{dc}} = \frac{5\ mA - 10\mu A}{0.98} = \mathbf{5.092\ mA}$$

From equation $I_B = I_E - I_C$ we get,

$$I_B = 5.092 \times 10^{-3} - 5 \times 10^{-3} = \mathbf{92\ \mu A}$$

➠ **Example 3.8 :** *The reverse leakage current of the transistor, when connected in common-base configuration is 1.1 μA, while it is 21 μA when the same transistor is connected in common-emitter configuration. Calculate the α_{dc} and β_{dc} of the transistor.*

Solution : Given : $I_{CBO} = 1.1\ \mu A$, $I_{CEO} = 21\ \mu A$

$$I_{CEO} = (1 + \beta_{dc})\, I_{CBO}$$

$$\therefore \quad 1 + \beta_{dc} = \frac{I_{CEO}}{I_{CBO}} = \frac{21\,\mu A}{1.1\,\mu A} = 19$$

$$\therefore \quad \beta_{dc} = 18$$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{18}{1+18} = 0.947$$

3.5 Biasing of Transistor

3.5.1 Operating Point

The transistor can be operated in three regions : cut-off, active and saturation by applying proper biasing conditions as shown in the Table 3.4.

Region of Operation	Emitter Base Junction	Collector Base Junction
Cut-off	Reverse biased	Reverse biased
Active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased

Table 3.4 Operating regions and bias conditions

In order to operate transistor in the desired region we have to apply external d.c. voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor. Because d.c. voltages are used to bias the transistor, biasing is known as **d.c. biasing** of the transistor.

When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or **d.c. operating point** or **quiescent point**. The operating point must be stable for proper operation of the transistor. However, the operating point shifts with changes in transistor parameters such as β, I_{CO} and V_{BE}. As transistor parameters are temperature dependent, the operating point also varies with changes in temperature.

3.5.2 Need for Biasing BJT

From the above discussion, it is clear that we have to supply external d.c. voltages (d.c. biasing) of correct polarity and magnitude to the two junctions of the transistor, to operate it in the desired region.

In transistor circuits, output signal power is always greater than input signal power. Now the question is how this amplification of power is achieved. The d.c. sources(d.c. biasing) supplies the power to the transistor circuit to get the output signal power greater than input signal power.

3.6 Fixed Bias Circuit

The Fig. 3.28 shows the fixed bias circuit. It is the simplest d.c. bias configuration. For the d.c. analysis we can replace capacitor with an open circuit because the reactance of a capacitor for d.c. is $X_C = 1/2\pi fC = 1/2\pi(0)C = \infty$. The d.c. equivalent of fixed bias circuit is shown in Fig. 3.28(b).

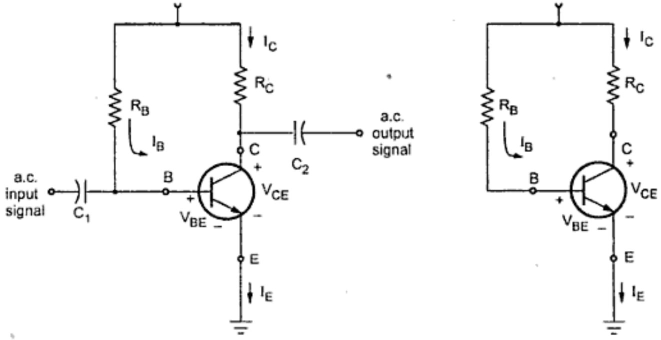


Fig. 3.28

3.6.1 Circuit Analysis

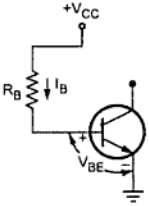


Fig. 3.29 Base circuit of the fixed bias circuit

Base Circuit :

Let us consider the base circuit as shown in Fig. 3.29

Applying Kirchhoff's voltage law to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for the current I_B,

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \quad \ldots (1)$$

Collector Circuit

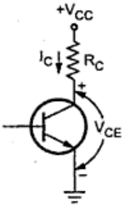


Fig. 3.30 Collector circuit of the fixed bias circuit

We now consider the collector circuit as shown in Fig. 3.30. Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad \boxed{V_{CE} = V_{CC} - I_C R_C} \qquad \dots (2)$$

The magnitude of collector current is given by,

$$\therefore \quad \boxed{I_C = \beta I_B} \qquad \dots (3)$$

and from equation (2) we have,

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}} \qquad \dots (4)$$

It is important to note that since the base current is controlled by the value of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Changing R_C to any level will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, the change in R_C will change the value of V_{CE}.

$$\boxed{V_{CE} = V_C - V_E} \qquad \dots (5)$$

Where, V_C : Collector voltage

V_E : Emitter voltage

Similarly,

$$\boxed{V_{BE} = V_B - V_E} \qquad \dots (6)$$

Where, V_B : Base voltage

In this circuit, $V_E = 0$,

$$\therefore \quad \boxed{V_{BE} = V_B} \qquad \dots (7)$$

$$\text{and} \quad \boxed{V_{CE} = V_C} \qquad \dots (8)$$

➡ **Example 3.9 :** *For the circuit shown in the Fig. 3.31 calculate* $I_B, I_C, V_{CE}, V_B, V_C$ *and* V_{BC}. *Assume* $V_{BE} = 0.7\ V$ *and* $\beta = 50$.

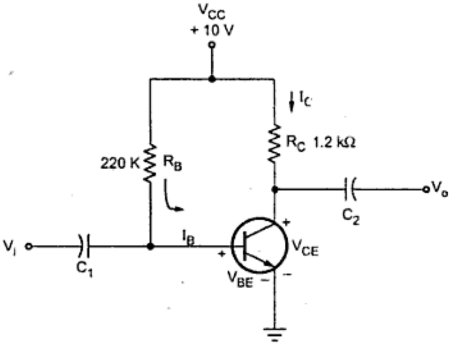


Fig. 3.31

Solution :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{220 \times 10^3} = \mathbf{42.27\ \mu A}$$

$$I_C = \beta I_B = 50 \times 42.27 \times 10^{-6} = \mathbf{2.1135\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^3$$

$$= \mathbf{7.4638\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V}$$

$$V_C = V_{CE} = \mathbf{7.4638\ V}$$

$$V_{BC} = V_B - V_C = 0.7 - 7.4638 = \mathbf{-\ 6.7638}$$

The negative voltage V_{BC} indicates that base-collector junction is reverse biased.

3.6.2 Load Line and Quiescent Point

For fixed-bias circuit, we have

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \left[\frac{1}{R_C}\right] V_{CE}$$

$$= -\left[\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C}$$

By comparing this equation with equation of straight line y = mx + c, where m is the slope of the line and c is the intercept on Y-axis, then we can draw a straight line on the graph of I_C versus V_{CE} which is having slope $-1/R_C$ and Y-intercept V_{CC}/R_C. To determine the two points on the line we assume $V_{CE} = V_{CC}$ and $V_{CE} = 0$.

a) When $V_{CE} = V_{CC}$; $I_C = 0$ and we get a point A and

b) When $V_{CE} = 0$; $I_C = V_{CC}/R_C$ and we get a point B

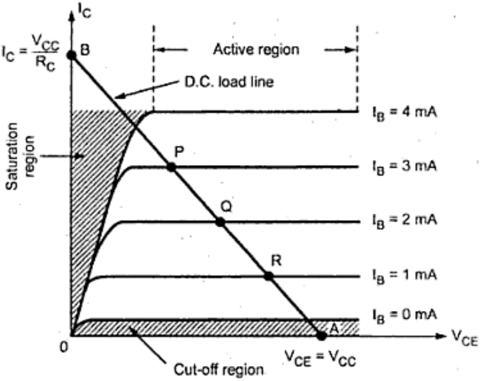


Fig. 3.32 Common emitter output characteristics with d.c. load line

The Fig. 3.32 shows the output characteristics of a common emitter configuration with points A and B, and line drawn between them. The line drawn between points A and B is called **d.c. load line**. The 'd.c.' word indicates that only d.c. conditions are considered, i.e. input signal is assumed to be zero.

The d.c. load line is a plot of I_C versus V_{CE}. For a given value of R_C and a given level of V_{CC}. Thus, it represents all collector current levels and corresponding collector-emitter voltages that can exist in the circuit. Knowing any one of I_C, I_B or V_{CE}, it is easy to determine the other two from the load line. The slope of the d.c. load line depends on the value of R_C. It is negative and equal to reciprocal of the R_C.

Applying Kirchhoff's voltage law to the base circuit of Fig. 3.28 we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The intersection of curves of different values of I_B with d.c. load line gives different operating points. For different values of I_B, we have different intersection points (quiescent point or Q point) such as P, Q and R.

Example 3.10 : *Design the fixed bias circuit from the load line given in the Fig. 3.33.*

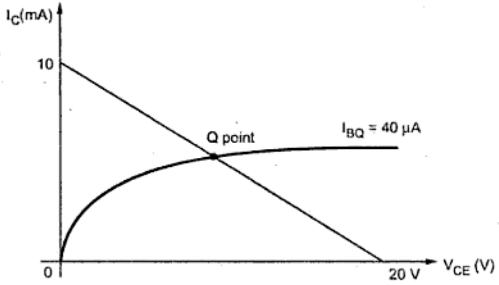


Fig. 3.33

Solution : From the load line we have,

$$V_{CC} = 20 \text{ V}$$

$$\frac{V_{CC}}{R_C} = 10 \times 10^{-3} \qquad \therefore \; R_C = \frac{20}{10 \times 10^{-3}} = 2 \text{ K}$$

We have,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \qquad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 - 0.7 \text{ V}}{40 \times 10^{-6}}$$

$$= \mathbf{482.5 \ k\Omega}$$

3.6.3 Selection of Operating Point

The operating point can be selected at different positions on the d.c. load line : near saturation region, near cut-off region or at the center, i.e. in the active region. Refer Fig. 3.33. The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the d.c. load line to prevent any possible distortion in the amplified output signal. This is well-understood by going through following cases.

Case 1 : Biasing circuit is designed to fix a Q point at point P, as shown in Fig. 3.34 Point P is very near to the saturation region. As shown in Fig. 3.34 the collector current is clipped at the positive half cycle. So, eventhough base current varies sinusoidally, collector current is not a useful sinusoidal waveform. i.e. distortion is present at the output. Therefore, point P is not a suitable operating point.

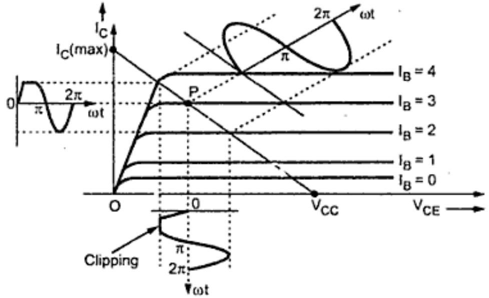

I_C
$I_C(max)$
2π
ωt
π
P
0
$I_B = 4$
$I_B = 3$
$I_B = 2$
$I_B = 1$
$I_B = 0$
O
V_{CC}
V_{CE}
Clipping
ωt

Fig. 3.34 Operating point near saturation region gives clipping at the positive peaks

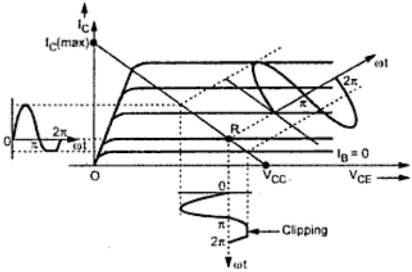

I_C
$I_C(max)$
ωt
2π
π
R
0
$I_B = 0$
O
V_{CC}
V_{CE}
Clipping
ωt

Fig. 3.35 Operating point near cut-off region gives clipping at the negative peaks

Case 2 : Biasing circuit is designed to fix a Q point at point R as shown in Fig. 3.35 Point R is very near to the cut-off region. As shown in Fig. 3.35 the collector current is clipped at the negative half cycle. So, point R is also not a suitable operating point.

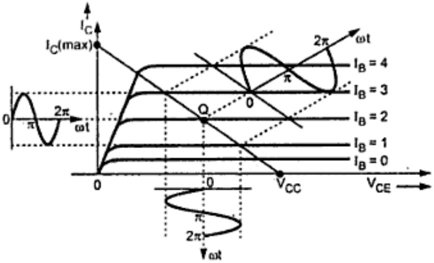

I_C
$I_C(max)$
2π
ωt
π
Q
0
$I_B = 4$
$I_B = 3$
$I_B = 2$
$I_B = 1$
$I_B = 0$
V_{CC}
V_{CE}
ωt

Fig. 3.36 Operating point at the centre of active region is most suitable

Case 3 : Biasing circuit is designed to fix a Q point at point Q as shown in Fig. 3.36 The output signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.

3.6.4 Typical Junction Voltages and Conditions for Operating Region

We have seen that, we can operate transistor configurations in different operating regions by selecting appropriate operating point. For the analysis and design of such circuits we should know the typical junction voltages in different operating regions.

The Table 3.5 shows the typical junction voltages for cut-off, active and saturation regions for n-p-n silicon and germanium transistors. For p-n-p transistors we have to reverse the polarities of voltages given in Table 3.5.

Transistor	$V_{CE\,(sat)}$	$V_{BE\,(sat)}$	$V_{BE\,(active)}$	$V_{BE\,(cut\text{-}in)}$	$V_{BE\,(cut\text{-}off)}$
Si	0.2 V	0.8 V	0.7 V	0.5 V	0 V
Ge	0.1 V	0.3 V	0.2 V	0.1 V	– 0.1 V

Table 3.5 Typical junction voltages

To identify the operating region of transistor we can observe certain conditions. These are :

For saturation : $I_B > \frac{I_C}{\beta_{dc}}$

For active region : $V_{CE} > V_{CE\,(sat)}$

➠ **Example 3.11 :** *In the circuit shown in Fig. 3.37, for* $R_B = 300\ k\Omega$ *, and* $R_B = 150\ k\Omega$ *calculate* I_B, I_C *and* V_{CE} *and determine region of operation.*

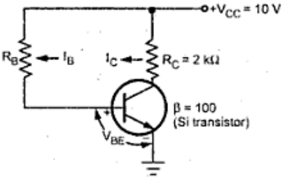


Fig. 3.37

Solution : i) $R_B = 300\ k\Omega$

Since base emitter junction is not reverse biased, we can say that transistor is not in cut-off region. Assume transistor is operating in an active region.

Applying KVL around base loop we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore \quad 10 = I_B \times 300 \times 10^3 + 0.7$$

$$\therefore \qquad I_B = \frac{9.3}{300 \times 10^3}$$

$$I_B = 0.031 \text{ mA} = \mathbf{31\ \mu A}$$

In active region $I_C = \beta I_B$

$$\therefore \qquad I_C = 100 \times 31\ \mu\text{A} = \mathbf{3.1\ mA}$$

Now, applying KVL around collector loop we get,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \qquad 10 = 3.1 \times 10^{-3} \times 2 \times 10^3 + V_{CE}$$

$$\therefore \qquad V_{CE} = 10 - 6.2 = \mathbf{3.8\ V}$$

V_{CE} is equal to 3.8 V i.e. $V_{CE\,(active)} > V_{CE\,(sat)}$, collector to base junction is reverse biased and we can say that our assumption that transistor is in active region is justified.

ii) R_B = 150 kΩ

Since base emitter junction is not reverse biased we can say that transistor is not in cut-off region. Assume transistor is operating in an active region.

Applying KVL around base loop we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore \qquad 10 = I_B \times 150 \times 10^3 + 0.7$$

$$\therefore \qquad I_B = \frac{9.3}{150 \times 10^3} = 0.062 \text{ mA} = \mathbf{62\ \mu A}$$

In active region $I_C = \beta I_B$

$$\therefore \qquad I_C = 100 \times 62\ \mu\text{A} = \mathbf{6.2\ mA}$$

Now, applying KVL around collector loop we get,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \qquad 10 = 6.2 \times 10^{-3} \times 2 \times 10^3 + V_{CE}$$

$$\therefore \qquad V_{CE} = 10\text{V} - 12.4\text{V} = \mathbf{-2.4\ V}$$

It is important to note that collector voltage has to be positive or zero. Hence our assumption that transistor is in active region is wrong and it is in saturation region.

Applying KVL around base loop we get,

$$V_{CC} = I_B R_B + V_{BE\,(sat)}$$

$$10 = I_B\,(150 \times 10^3) + 0.8$$

$$\therefore \qquad I_B = \frac{9.2}{150 \times 10^3} = \mathbf{61.33\ \mu A}$$

Applying KVL around collector loop we get,

$$V_{CC} = I_C R_C + V_{CE(sat)}$$

$$10 = I_C\,(2 \times 10^3) + 0.2$$

$$\therefore \qquad I_C = \frac{9.8}{2 \times 10^3} = \mathbf{4.9\ mA}$$

To justify that transistor is in saturation

$$I_B > \frac{I_C}{\beta}$$

$$\frac{I_C}{\beta} = \frac{4.9 \times 10^{-3}}{100} = \mathbf{49\ \mu A}$$

Therefore $\frac{I_C}{\beta}$ is less than I_B and our assumption that transistor in saturation is justified.

3.6.5 Variation of Quiescent Point

From the points discussed so far, it is clear that the biasing circuit should be designed to fix the operating point or Q point at the center of the active region. But only fixing of the operating point is not sufficient. While designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region (i.e. into cut-off or saturation region). Designing the biasing circuit to stabilize the Q point is known as **bias stability.**

Two important factors are to be considered while designing the biasing circuit which are responsible for shifting the operating point.

I) Temperature

1) I_{CO} : The flow of current in the circuit produces heat at the junctions. This heat increases the temperature at the junctions. We know that the minority carriers are temperature dependent. They increase with the temperature. The increase in the minority carriers increases the leakage current I_{CEO},

$$\because \qquad I_{CEO} = (1 + \beta)\, I_{CBO} \qquad \text{... (9)}$$

Specifically, I_{CBO} doubles for every 10°C rise in temperature. Increase in I_{CEO} in turn increases the collector current,

$$\because \qquad I_C = \beta I_B + I_{CEO} \qquad \text{... (10)}$$

The increase in I_C further raises the temperature at the collector junction and the same cycle repeats. This excessive increase in I_C shifts the operating point into the saturation region, changing the operating condition set by biasing circuit.

As the power dissipated within a transistor is predominantly the power dissipated at its collector base junction, the power dissipation is given as,

$$P_D = V_C I_C \quad \dots (11)$$

The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increases the collector current. The process is cumulative. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called **'Thermal runaway'** of the transistor. For any transistor, maximum power dissipation is always a fixed value. That is known as **maximum power dissipation** rating of a transistor. This value is specified by the manufacturer in data sheets. As shown in Fig. 3.38, the hyperbola gives the maximum power dissipation for transistor. If this limit is crossed, the device will fail.

2) **V_{BE}** : Base to emitter voltage V_{BE} changes with temperature at the rate of 2.5 mV/°C. Base current, I_B depends upon V_{BE}. As base current I_B depends on V_{BE} and I_C depends on I_B, I_C depends on V_{BE}. Therefore collector current I_C changes with temperature due to change in V_{BE}. The change in collector current change the operating point.

3) **β_{dc}** : β_{dc} of the transistor is also temperature dependent. As β_{dc} varies, I_C also varies, since $I_C = \beta I_B$. The change in collector current change the operating point.

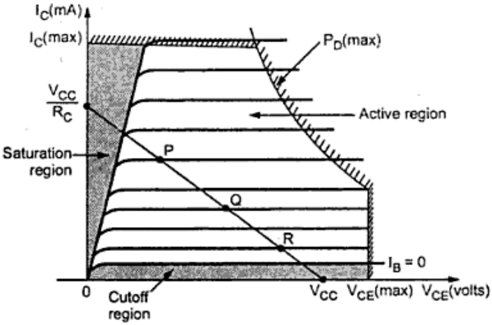


Fig. 3.38 Output characteristics of a transistor in common-emitter configuration. Maximum current, voltage and power ratings are indicated

Therefore, to avoid thermal instability, the biasing circuit should be designed to provide a degree of temperature stability i.e. even though there are temperature changes, the changes in the transistor parameters (V_{CEQ}, I_{CQ}, P_{Dmax}) should be very less so that the operating point shifting is minimum in the middle of the active region.

II) Transistor current gain h_{FE} /β

Eventhough there is tremendous advancement in semiconductor technology, there are changes in the transistor parameters among different units of the same type, same number. This means if we take two transistor units of same type (i.e. same number, construction, parameter specified etc.) and use them in the circuit, there is change in the β value in actual practice. The biasing circuit is designed according to the required β value. But due to change in β from unit to unit, the operating point may shift.

Fig. 3.39 shows the common emitter output characteristics for two transistors of the same type. The dashed characteristics are for a transistor whose β is much larger than that of the transistor represented by the solid curves.

So for stabilizing the operating point the factors discussed so far should be considered while designing the biasing circuit. From all this explanation we can summarize the requirements of a biasing circuit as follows :

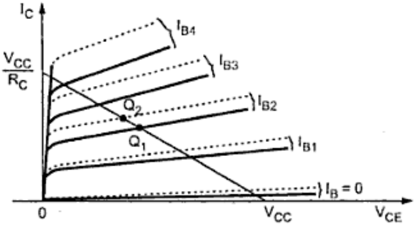


Fig. 3.39 Graphs showing the collector characteristics for two transistors of the same type

Requirements of a biasing circuit

i) The emitter-base junction must be forward biased (forward biased voltage 0.6 V to 0.7 V) and collector-base junction must be reverse biased (within maximum limits). i.e. the transistor should be operated in the middle of the active region or operating point (Q point) should be fixed at the center of the active region.

ii) The circuit design should provide a degree of temperature stability.

iii) The operating point should be made independent of the transistor parameters (such as β).

To maintain the operating point stable by keeping I_C and V_{CE} constant so that the transistor will always work in active region, the following techniques are normally used

(i) Stabilization techniques (ii) Compensation techniques.

Key Points :

1. *Stabilization techniques refer to the use of resistive biasing circuits which allow* I_B *to vary so as to keep* I_C *relatively constant with variations in* I_{CO}, β *, and* V_{BE}.
2. *Compensation techniques refer to the use of temperature-sensitive devices such as diodes, transistors thermistors, etc., which provide compensating voltages and currents to maintain the operating point stable.*

3.6.6 Advantages of Fixed Bias Circuit

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B. Thus, it provides maximum flexibility in the design.

3.6.7 Disadvantages of Fixed Bias Circuit

1. This circuit does not provide any check on the collector current which increases with the rise in temperature. i.e. thermal stability is not provided by this circuit. So the operating point is not maintained.

$$I_C = \beta I_B + I_{CEO}$$

2. Since $I_C \approx \beta I_B$ and I_B is already fixed; I_C depends on β which changes unit to unit and shifts the operating point.

Thus stabilization of operating point is very poor in the fixed bias circuit.

Key Point: *If the transistor is replaced by another transistor, eventhough the type is same their characteristic may differ slightly. In fixed bias circuit, the change in the characteristic of transistor changes the operating point. For example, if there is a change in value of* β, *there is change in* $I_C = \beta I_B$ *as* I_B *is constant in fixed biased circuit. The change in* I_C *changes the operating point and hence we can say that a fixed bias circuit is unsatisfactory if the transistor is replaced by another of the same type.*

➡ **Example 3.12 :** *Design a fixed biased circuit using a silicon transistor having* β *value of 100.* V_{CC} *is 10 V and d.c. bias conditions are to be* $V_{CE} = 5$ *V and* $I_C = 5$ *mA.*

Solution : Applying KVL to collector circuit we get,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$\therefore \quad R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{10-5}{5\text{ mA}} = 1\text{ K}$$

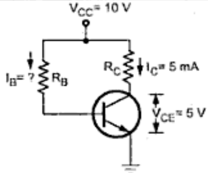


Fig. 3.40

$$I_B = \frac{I_C}{\beta} = \frac{5\text{ mA}}{100} = 50\ \mu A$$

Now, applying KVL to base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{50\,\mu A} = 186\ k\Omega$$

Example 3.13 : *The fixed biased circuit in Fig. 3.41 is subjected to an increase in junction temperature from 25 °C to 75 °C. If $\beta = 100$ at 25 °C and $\beta = 125$ at 75 °C, determine percent change in Q point values (V_{CE}, I_C) over the temperature range. Neglect any change in V_{BE}.*

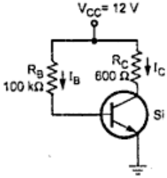


Fig. 3.41

Solution :

At 25 °C :

Applying KVL to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{100 \times 10^3} = 113\ \mu A$$

$$\therefore \quad I_C = \beta I_B = 100 \times 113 \times 10^{-6} = 11.3\ mA$$

Applying KVL to the collector circuit we get

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C = 12 - 11.3 \times 10^{-3} \times 600$$

$$= 5.22\ V$$

At 75 °C
$$I_B = 113\ \mu A$$
$$I_C = \beta I_B = 125 \times 113 \times 10^{-6} = 14.125\ mA$$
$$V_{CE} = V_{CC} - I_C R_C = 12 - 14.125 \times 10^{-3} \times 600 = 3.525\ V$$

The percent change in I_C is

$$\% \, \partial I_C = \frac{I_C(75°C) - I_C(25°C)}{I_C(25°C)} \times 100\% = \frac{14.25 \times 10^{-3} - 11.3 \times 10^{-3}}{11.3 \times 10^{-3}} \times 100\%$$
$$= 25\%\ \text{(an increase)}$$

The percent change in V_{CE} is

$$\% \, \partial V_{CE} = \frac{V_{CE}(75°C) - V_{CE}(25°C)}{V_{CE}(25°C)} \times 100\% = \frac{3.525 - 5.22}{5.22} \times 100\%$$
$$= -32.47\%\ \text{(a decrease)}$$

3.7 Stability Factors

Stabilization techniques give different biasing circuits which are discussed in the following sections. In order to compare the stability provided by these circuits, one term is raised called **stability factor**, which indicates degree of change in operating point due to variation in temperature. Since there are three variables which are temperature dependent, we can define three stability factors as below :

i) $$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}} \quad \text{or} \quad S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}} \quad \ldots (1)$$

ii) $$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}} \quad \text{or} \quad S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}} \quad \ldots (2)$$

iii) $$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}} \quad \ldots (3)$$

Key Point :

1. *Ideally, stability factor should be perfectly zero to keep operating point stable.*
2. *Practically stability factor should have the value as minimum as possible. Thermal stability of a circuit is assessed by deriving a stability factor, S.*

3.7.1 Stability Factor S

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$

or
$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad \ldots (4)$$

When I_{CBO} changes by ΔI_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C. So this equation becomes,

$$\partial I_C = \beta \partial I_B + (1+\beta)\partial I_{CBO}$$

$$\therefore 1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \quad 1 - \beta\frac{\partial I_B}{\partial I_C} = (1+\beta)\frac{\partial I_{CBO}}{\partial I_C}$$

$$\therefore \frac{\partial I_{CBO}}{\partial I_C} = \frac{1-\beta(\partial I_B/\partial I_C)}{1+\beta}$$

$$S = \frac{\partial I_C}{\partial I_{CBO}}$$

$$S = \frac{(1+\beta)}{1-\beta(\partial I_B/\partial I_C)} \qquad \ldots (5)$$

The above equation can be considered as a standard equation for derivation of stability factors of other biasing circuits.

Key Point: *The general procedure to obtain stability factors for various biasing circuits is as follows :*

Step 1 : *Obtain the expression for I_B.*

Step 2 : *Obtain $\partial I_B / \partial I_C$ and use it in equation 5 to get S.*

Step 3 : *In standard equation of I_C, replace I_B in terms of V_{BE} to get S'.*

Step 4 : *Differentiate the equation obtained in step 3 with respect to β' to get S".*

Stability Factors for Fixed Bias Circuit

Stability factor S

$$I_B \cong \frac{V_{CC}}{R_B}$$

When I_B changes by ∂I_B, V_{CC} and V_{BE} are unaffected.

$\therefore \frac{\partial I_B}{\partial I_C} = 0 \quad \because I_C$ is not present in the equation.

Substituting this value in equation (5), we get,

$$S = \frac{1+\beta}{1-\beta(\partial I_B/\partial I_C)} = \frac{1+\beta}{1-0}$$

$$\therefore \qquad S = 1+\beta \qquad \ldots (6)$$

Stability Factor S'

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta\ \text{constant}}$$

From equation (4) we have,

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

Now representing I_B in terms of V_{BE} we get,

$$I_C = \beta \frac{(V_{CC} - V_{BE})}{R_B} + (\beta + 1) I_{CBO}$$

$$\therefore \quad I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta + 1) I_{CBO} \quad \text{... (7)}$$

$$\therefore \quad \frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0 = \frac{-\beta}{R_B}$$

$$\therefore \quad S' = \frac{-\beta}{R_B} \quad \text{... (8)}$$

Relation between S and S′

We know that $S = 1 + \beta$ and $S' = \frac{-\beta}{R_B}$

Multiplying numerator and denominator by $(1 + \beta)$ we have

$$S' = \frac{-\beta(1+\beta)}{R_B(1+\beta)}$$

$$S' = \frac{-\beta S}{R_B(1+\beta)} \qquad \because S = 1 + \beta \quad \text{... (9)}$$

Stability Factor S''

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{V_{BE},\, I_{CO}\ \text{constant}}$$

From equation (7) we have

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta + 1) I_{CBO}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CBO} = I_B + I_{CBO} = \frac{I_C}{\beta}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta} \quad \textbf{Since } I_B = \frac{I_C}{\beta} \textbf{ and } I_B >> I_{CBO} \quad \text{... (10)}$$

Relation between S and S″

We know that $S = 1 + \beta$ and $S'' = \frac{I_C}{\beta}$

Multiplying numerator and denominator by $(1 + \beta)$ we have

$$S'' = \frac{I_C (1+\beta)}{\beta(1+\beta)}$$

$$\therefore \quad S'' = \frac{I_C\, S}{\beta\,(1+\beta)} \qquad \because \; S = 1 + \beta \qquad \ldots (11)$$

Example 3.14 : *In the circuit shown in Fig. 3.42 calculate stability factor S.*

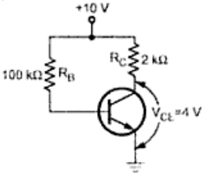


Fig. 3.42

Solution : The circuit shown in Fig. 3.42 is a fixed bias circuit. Thus the stability factor :

$$S = 1 + \beta$$

To calculate β, it is necessary to find I_C and I_B.

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{10-4}{2 \times 10^3} = \mathbf{3\ mA}$$

Now, Applying KVL to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10-0.7}{100 \times 10^3} = \mathbf{93\ \mu A}$$

Now $$\beta = \frac{I_C}{I_B} = \frac{3 \times 10^{-3}}{93 \times 10^{-6}} = 32.258$$

and stability factor $S = 1 + \beta = 1 + 32.258 = \mathbf{33.258}$

3.8 Collector to Base Bias Circuit

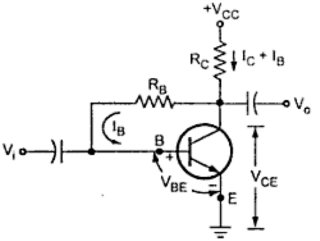


Fig. 3.43 D.C. bias with voltage feedback

The Fig. 3.43 shows the dc bias with voltage feedback. It is also called the collector to base bias circuit. It is an improvement over the fixed-bias method. In this the biasing resistor is connected between the collector and the base of the transistor to provide a feedback path. Thus I_B flows through R_B and $(I_C + I_B)$ flows through the R_C.

3.8.1 Circuit Analysis

Base Circuit

Let us consider the base circuit of Fig. 1.50. Applying voltage law to the base circuit we get,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$\therefore \quad V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$= (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}} \qquad \because \beta >> 1$$

Note that the only difference between the equation for I_B and that obtained for the fixed bias configuration is the term βR_C. Thus, we can say that the feedback path results in a reflection of the resistance R_C to the input circuit.

Collector Circuit

Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$\therefore \quad V_{CE} = V_{CC} - (I_C + I_B) R_C$$

If there is a change in β due to piece to piece variation between transistors or if there is a change in β and I_{CO} due to the change in temperature, then collector current I_C tends to increase, since $I_C = \beta I_B + I_{CEO}$. As a result, voltage drop across R_C increases. Since supply voltage V_{CC} is constant, due to increase in $I_C R_C$, V_{CE} decreases. Due to reduction in V_{CE}, I_B reduces. As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

In this circuit, R_B appears directly across input (base) and output (collector). A part of the output is fed back to the input, and increase in collector current decreases the base current. Thus negative feedback exists in the circuit, so this circuit is also called voltage feedback bias circuit

➡ **Example 3.15 :** *Calculate the Q point values (I_C and V_{CE}) for the circuit in Fig. 3.44.*

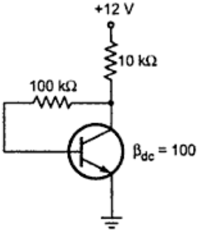


Fig. 3.44

Solution :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} = \frac{12-0.7}{100\times10^3 + (1+100)\times10\times10^3}$$

$$= \mathbf{10.18\ \mu A}$$

$$\therefore \quad I_C = \beta I_B = 100 \times 10.18\ \mu A = \mathbf{1.018\ mA}$$

$$V_{CE} = V_{CC} - (I_B + I_C)\, R_C$$

$$= 12 - (10.18 \times 10^{-6} + 1.018 \times 10^{-3}) \times 10 \times 10^3 = \mathbf{1.7182\ V}$$

➡ **Example 3.16 :** *Design a collector to base bias circuit for the specified conditions : V_{CC} = 15 V, V_{CE} = 5 V, I_C = 5 mA, and β = 100.*

Solution :

$$I_B = \frac{I_C}{\beta} = \frac{5\ mA}{100} = 50\ \mu A$$

We know that for collector to base bias circuit, $V_{CE} = V_{CC} - (I_B + I_C)\, R_C$

Thus we can write,

$$R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C} = \frac{15-5}{50\times10^{-6} + 5\times10^{-3}} = 1.98\ \text{k}\Omega$$

$$\therefore \quad R_C = \mathbf{1.98\ k\Omega}$$

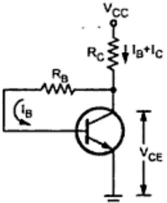


Fig. 3.45

Applying KVL to the input circuit we have,

$$V_{CE} - I_B R_B - V_{BE} = 0$$

$$\therefore \quad R_B = \frac{V_{CE} - V_{BE}}{I_B}$$

$$= \frac{5-0.7}{50\times10^{-6}}$$

$$= \mathbf{86\ k\Omega}$$

3.8.2 Modified Collector to Base Bias Circuit

To further improve the level of stability, the emitter resistance is connected in this circuit, as shown in the Fig. 3.46.

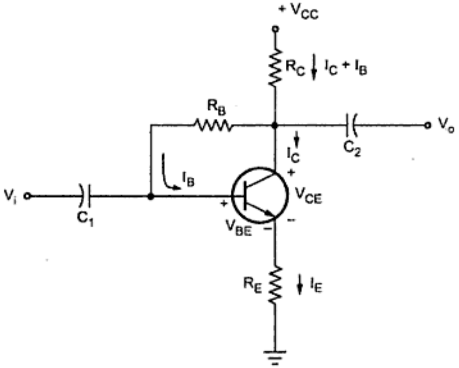


Fig. 3.46 Modified d.c. bias with voltage feedback

Base Circuit

Applying KVL to the base circuit shown in the Fig. 3.46 we have,

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\therefore \quad V_{CC} - V_{BE} = (1+\beta)\, R_C + I_B R_B + (1+\beta)\, R_E$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)}}$$

$$\therefore \quad \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}} \qquad \because \beta >> 1$$

Note that the only difference between the equation for I_B and that obtained for the fixed-bias configuration is the term $\beta(R_C + R_E)$. Thus we can say that the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general we can say that,

$$\boxed{I_B = \frac{V'}{R_B + \beta R'}} \qquad \because \beta >> 1$$

Where $V' = V_{CC} - V_{BE}$

and $R' = 0$ for fixed bias.

$R' = R_E$ for emitter bias.

$R' = R_C$ for collector to base bias.

$R' = R_C + R_E$ for collector to base bias with R_E.

Collector Circuit

Applying KVL to collector circuit we have,

$$V_{CC} - (I_C + I_B)R_C - V_{CE} - I_E R_E = 0$$

$$\therefore \quad \boxed{V_{CE} = V_{CC} - I_E(R_C + R_E)}$$

➠ **Example 3.17 :** *For the circuit shown in the Fig. 3.47, determine the quiescent levels of I_C and V_{CE}.*

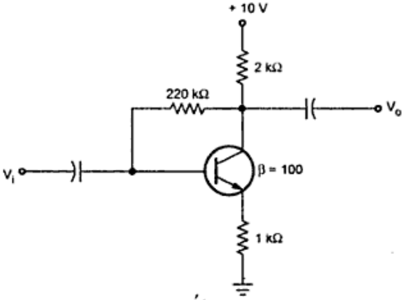


Fig. 3.47

Solution :

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)} = \frac{10 - 0.7}{220\times10^3 + (1+100)(2\times10^3 + 1\times10^3)}$$

$$= \mathbf{17.78\ \mu A}$$

$$I_{CQ} = \beta I_{BQ} = 100 \times 17.78 \times 10^{-6} = \mathbf{1.778\ mA}$$

$$I_{EQ} = I_{BQ} + I_{CQ} = 17.78 \times 10^{-6} + 1.778\times10^{-3} = \mathbf{1.796 \times 10^{-3}}$$

$$V_{CEQ} = V_{CC} - I_E(R_C + R_E) = 10 - 1.796 \times 10^{-3}(2\times10^3 + 1\times10^3)$$

$$= \mathbf{4.612\ V}$$

Example 3.18 : *For the circuit shown in the Fig. 3.48 determine the* I_{BQ}, I_{CQ} *and* V_{CEQ}.

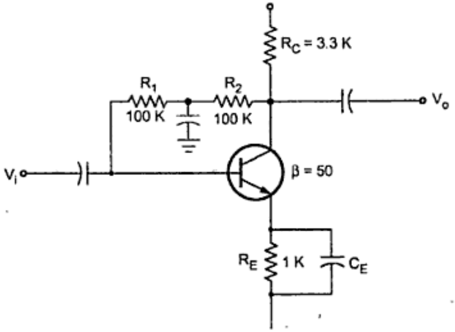


Fig. 3.48

Solution : For the d.c. analysis capacitors are open circuit, therefore $R_B = R_1 + R_2$.

$$\therefore \quad I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)(R_C + R_E)} = \frac{12 - 0.7}{200\times10^3 + (1+50)\,(3.3\times10^3 + 1\times10^3)}$$

$$= \mathbf{26.95\ \mu A}$$

$$\therefore \quad I_{CQ} = \beta I_{BQ} = 50 \times 26.95 \times 10^{-6} = \mathbf{1.347\ mA}$$

$$I_{EQ} = I_{BQ} + I_{CQ} = 26.95 \times 10^{-6} + 1.347\times10^{-3}$$

$$= \mathbf{1.3739\ mA}$$

$$V_{CEQ} = V_{CC} - I_E(R_C + R_E)$$

$$= 12 - 1.3739 \times 10^{-3}(3.3\times10^{3} + 1\times10^{3})$$

$$= \mathbf{6.09\ V}$$

Stability Factor S for Collector to Base Bias Circuit

$$V_{CC} = I_C R_C + I_B (R_C + R_B) + V_{BE}$$

When I_{CBO} changes by $\partial\ I_{CBO}$, I_B changes by $\partial\ I_B$ and I_C changes by $\partial\ I_C$. There is no effect on V_{CC} and V_{BE}. So the equation becomes,

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B)$$

$$\therefore \quad -\partial I_C R_C = \partial I_B (R_C + R_B)$$

$$\therefore \quad \frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B}$$

Substituting this value in equation (5),

We get $$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_C+R_B}\right)}$$

$$\therefore \quad \mathbf{S} = \frac{\mathbf{1+\beta}}{1+\beta\left(\frac{\mathbf{R_C}}{\mathbf{R_C+R_B}}\right)} \qquad \ldots (1)$$

Collector to base bias circuit is having lesser stability factor than for fixed bias circuit. Hence this circuit provides better stability than fixed bias circuit.

Stabilization with Changes in β

The equation (1) shows that the stability factor, S for this circuit also depends on β. But if we design the circuit with condition $\beta R_C >> R_B$ then we can make stability factor independent of β. We can prove it mathematically as follows :

We know,

$$I_C = (1+\beta) I_{CBO} + \beta I_B$$

$$\therefore \quad I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta}$$

Applying KVL to base circuit we can write,

$$-V_{CC} + (I_B + I_C) R_C + I_B R_B + V_{BE} = 0$$

$$-V_{CC} + I_B (R_C + R_B) + I_C R_C + V_{BE} = 0$$

Substituting value of I_B in above equation

$$-V_{CC} + \left[\frac{I_C - (1+\beta)I_{CO}}{\beta}\right](R_C + R_B) + I_C R_C + V_{BE} = 0$$

Multiplying by β on both sides we get,

$$-\beta V_{CC} + I_C (R_C + R_B) - (1+\beta) I_{CO} (R_C + R_B) + \beta I_C R_C + \beta V_{BE} = 0$$

$$I_C [R_C + R_B + \beta R_C] = [\beta V_{CC} + I_{CO} (1+\beta)(R_C + R_B) - \beta V_{BE}]$$

As $\beta >> 1$, $1 + \beta \approx \beta$

$$I_C [\beta R_C + R_B] = \beta [V_{CC} - V_{BE} + I_{CO} (R_C + R_B)]$$

$$\therefore \quad I_C \approx \frac{\beta [V_{CC} - V_{BE} + I_{CO} (R_C + R_B)]}{(R_B + \beta R_C)} \quad \ldots (2)$$

As said earlier,

If we make $\beta R_C >> R_B$ the equation (2) becomes,

$$\therefore \quad I_C \approx \frac{V_{CC} - V_{BE} + I_{CO} (R_C + R_B)}{R_C} \quad \ldots (3)$$

and we can say that, the collector current has become independent of β and hence stabilized against change in β.

Stability Factor S'

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$$

By applying KVL to circuit shown in Fig. 3.43.

We have

$$V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

$$\therefore \quad \frac{I_C}{\beta} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

$$\therefore \quad \frac{I_C}{\beta} + \frac{I_C R_C}{R_C + R_B} = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$\therefore \quad I_C \left[\frac{1}{\beta} + \frac{R_C}{R_C + R_B}\right] = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$\therefore \quad I_C \left[\frac{R_C + R_B + \beta R_C}{\beta (R_C + R_B)}\right] = \frac{V_{CC} - V_{BE}}{(R_C + R_B)}$$

$$\therefore \quad I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1+\beta) R_C}$$

$$\therefore \quad \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_C}$$

$$\therefore \quad S' = \frac{-\beta}{R_B + (1+\beta) R_C} \quad \text{...(4)}$$

Relation between S and S′

We have
$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)} \text{ and } S' = \frac{-\beta}{R_B+(1+\beta)R_C}$$

$$S = \frac{(1+\beta)(R_C+R_B)}{R_C+R_B+\beta R_C} = \frac{(1+\beta)(R_C+R_B)}{R_B+(1+\beta)R_C} \quad \text{... (5)}$$

$$\frac{S}{(1+\beta)(R_C+R_B)} = \frac{1}{R_B+(1+\beta)R_C}$$

$$\therefore \quad \frac{-S\beta}{(1+\beta)(R_C+R_B)} = \frac{-\beta}{R_B+(1+\beta)R_C} = S'$$

$$\therefore \quad S' = \frac{-S\beta}{(1+\beta)(R_C+R_B)} \quad \text{... (6)}$$

If S is small, S′ is still smaller. If we provide stability against I_{CO} variations, we get stability against V_{BE} variations also.

Stability Factor S″

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\, V_{BE} \text{ constant}}$$

For collector to base bias circuit we have,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$\therefore \quad V_{CC} - V_{BE} = (\beta I_B + I_B) R_C + I_B R_B = I_B [(\beta + 1) R_C + R_B]$$

$$\therefore \quad I_B = \frac{V_{CC}-V_{BE}}{(\beta+1)R_C+R_B}$$

$$\therefore \quad I_C = \frac{\beta(V_{CC}-V_{BE})}{(\beta+1)R_C+R_B} \quad \text{... (7)}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \frac{[(\beta+1)R_C+R_B](V_{CC}-V_{BE})-\beta(V_{CC}-V_{BE})(R_C)}{[(\beta+1)R_C+R_B]^2}$$

$$\left[\text{Hint : } \frac{d}{dt}\left(\frac{u}{v}\right) = \frac{v\times\frac{du}{dt} - u\times\frac{dv}{dt}}{v^2}\right]$$

$$= \frac{(V_{CC}-V_{BE})\,[(\beta+1)\,R_C+R_B-\beta R_C]}{[(\beta+1)R_C+R_B]^2} = \frac{(V_{CC}-V_{BE})\,(R_B+R_C)}{[(\beta+1)R_C+R_B]^2}$$

$$= \frac{(V_{CC}-V_{BE})\,(R_B+R_C)}{[(\beta+1)\,R_C+R_B]\,[(\beta+1)\,R_C+R_B]}$$

From equation (7) we have

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C\,(R_B+R_C)}{\beta\,[(\beta+1)R_C+R_B]}$$

Relation between S and S″

$$S'' = \frac{I_C\,(R_B+R_C)}{\beta\,[(\beta+1)R_C+R_B]} = \frac{I_C}{\beta}\,\frac{S}{(1+\beta)} \qquad \text{... (Refer equation 5)}$$

$$\therefore \qquad S'' = \frac{I_C}{\beta}\left(\frac{S}{(1+\beta)}\right) \qquad \text{... (8)}$$

Key Point: *If S is small, S″ will also be small. Thus, if we provide stability against* I_{CO} *variations, we get stability against β variations also.*

3.9 Voltage Divider Bias / Self Bias Circuit

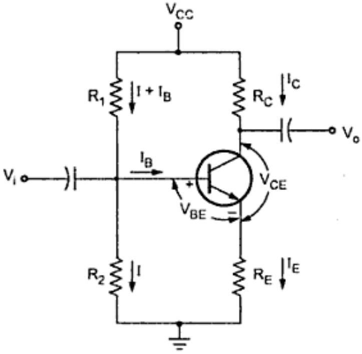


Fig. 3.49 Voltage divider bias circuit

Fig. 3.49 shows the voltage divider bias circuit. In this circuit, the biasing is provided by three resistors : R_1, R_2 and R_E. The resistors R_1 and R_2 act as a potential divider giving a fixed voltage to point B which is base. If collector current increases due to change in temperature or change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}). Due to reduction in V_{BE}, base current I_B and hence collector current I_C also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current I_C compensates for the original change in I_C.

3.9.1 Circuit Analysis

Base circuit

Let us consider the base circuit as shown in Fig. 3.50.

Voltage across R_2 is the base voltage V_B. Applying the voltage divider theorem to find V_B, we get,

$$V_B = \frac{R_2\,(I)}{R_1\,(I+I_B)+R_2\,(I)} \times V_{CC} \qquad \dots (9)$$

$$V_B = \frac{R_2}{R_1+R_2} \times V_{CC} \qquad \because\ I >> I_B \qquad \dots (10)$$

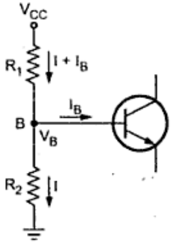


Fig. 3.50 Base circuit

Collector Circuit

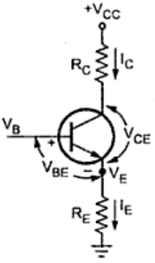


Fig. 3.51 Divider biased

Now, let us consider the collector circuit as shown in Fig. 3.51.

Voltage across R_E (V_E) can be obtained as,

$$V_E = I_E R_E = V_B - V_{BE}$$

$$\therefore \quad I_E = \frac{V_B - V_{BE}}{R_E} \qquad \dots (11)$$

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E \qquad \dots (12)$$

3.9.2 Simplified Circuit of Voltage Divider Bias

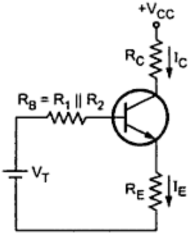


Fig. 3.52 Thevenin's equivalent circuit for voltage divider bias

Fig. 3.52 shows simplified circuit of voltage divider bias. Here, R_1 and R_2 are replaced by R_B and V_T, where R_B is the parallel combination of R_1 and R_2 and V_T is the Thevenin's voltage. R_B can be calculated as

$$R_B = \frac{R_1\,R_2}{R_1+R_2} \qquad \dots (13)$$

Applying KVL to the base circuit of Fig. 3.52 we get,

$$V_T = I_B R_B + V_{BE} + I_E R_E \qquad \dots (13a)$$

$$\therefore \quad V_T = V_{BE} + (R_B + R_E) I_B + I_C R_E \qquad \because\ I_E = I_C + I_B$$

$$\therefore \quad V_{BE} = V_T - (R_B + R_E) I_B - I_C R_E \qquad \text{... (14)}$$

We can use simplified/approximate analysis when

$$\boxed{\beta R_E \geq 10 R_2}$$

condition is satisfied. Under this condition results of exact and approximate analysis are nearly same.

Example 3.19 : *For the circuit shown in Fig. 3.53, $\beta = 100$ for the silicon transistor. Calculate V_{CE} and I_C.*

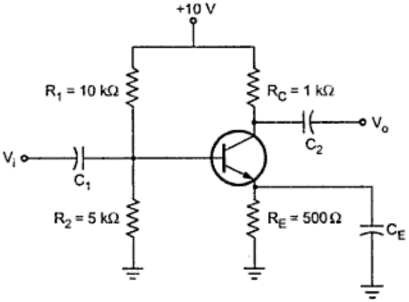


Fig. 3.53

Solution : Since $\beta R_E = 50{,}000 = 10 R_2$

We can use approximate analysis

$$V_B \cong \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{10 \times 10^3 + 5 \times 10^3} \times 10 = 3.33\ \text{V}$$

We know that, $$V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63\ \text{V}$$

and $$I_E = \frac{V_E}{R_E} = \frac{2.63\ \text{V}}{500} = 5.26\ \text{mA}$$

We know that, $$I_B = \frac{I_E}{1 + \beta} = \frac{5.26 \times 10^{-3}}{101} = 52.08\ \mu\text{A}$$

and $$I_C = \beta I_B = 100 \times 52.08 \times 10^{-6} = \mathbf{5.208\ mA}$$

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 5.208 \times 10^{-3} \times 1 \times 10^3 - 5.26 \times 10^{-3} \times 500$$

$$= \mathbf{2.162\ V}$$

➡ **Example 3.20 :** *For a circuit shown in Fig. 3.54,* $V_{CC} = 20\ V$, $R_C = 2\ k\Omega$, $\beta = 50$, $V_{BEact} = 0.2\ V$, $R_1 = 100\ k\Omega$, $R_2 = 5\ k\Omega$ *and* $R_E = 100\ \Omega$. *Calculate* I_B, V_{CE} & I_C .

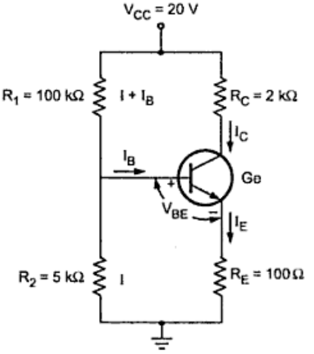


Fig. 3.54

Solution : Since $\beta R_E = 5000 < 10\ R_2$ we have to use exact analysis.

$$V_{CC} = R_1 [I + I_B] + I R_2$$

$$\therefore \quad I = \frac{V_{CC} - I_B R_1}{R_1 + R_2}$$

$$V_{CC} = R_1 [I + I_B] + V_{BE} + I_E R_E$$

We know that, $I_E = I_B + I_C = I_B + \beta I_B$

$$\therefore \quad V_{CC} = R_1 [I + I_B] + V_{BE} + (1+\beta) I_B R_E$$

Substituting value of I we get,

$$V_{CC} = R_1 \left[\frac{V_{CC} - I_B R_1}{R_1 + R_2} + I_B\right] + V_{BE} + (1+\beta) I_B R_E$$

$$= R_1 \left[\frac{V_{CC} - I_B R_1 + I_B R_1 + I_B R_2}{R_1 + R_2} \right] + V_{BE} + (1+\beta) I_B R_E$$

$$= R_1 \left[\frac{V_{CC} + I_B R_2}{R_1 + R_2} \right] + V_{BE} + (1+\beta) I_B R_E$$

Substituting values of V_{CC}, R_1, R_2, V_{BE}, β and R_E

We get,
$$20 = 100 \times 10^3 \left[\frac{20 + I_B \times 5 \times 10^3}{100 \times 10^3 + 5 \times 10^3} \right] + 0.2 + (51) I_B \times 100$$

$$20 = 19.047619 + 4761.9\, I_B + 0.2 + 5100\, I_B$$

$$0.752381 = 9861.9\, I_B$$

$$\therefore \quad I_B = \mathbf{76.29\ \mu A}$$

As
$$I_C = \beta I_B = 50 \times 76.29\ \mu A = \mathbf{3.814\ mA}$$

Applying KVL to collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + (1+\beta) I_B R_E$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - (1+\beta) I_B R_E$$

$$\therefore \quad V_{CE} = 20 - 3.814 \times 10^{-3} \times 2 \times 10^3 - (51) \times 76.29 \times 10^{-6} \times 100$$

$$= \mathbf{11.983\ V}$$

➠ **Example 3.21 :** *Draw the d.c. load line for the following transistor configuration. Obtain the quiescent point.*

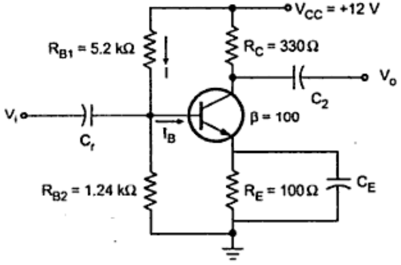


Fig. 3.55

Solution : Since, βR_E = 20 K and which is greater than 10 R_2 we can use approximate analysis.

$$\therefore \quad I = \frac{V_{CC}}{R_{B1} + R_{B2}} = \frac{12}{5.2\text{ K} \times 1.24\text{ K}} = \mathbf{1.863\text{ mA}}$$

$$\therefore \quad V_{TH} = V_{RB2} = I \times R_{B2} = 1.863\text{ mA} \times 1.24\text{ K} = \mathbf{2.31\text{ V}}$$

$$R_{TH} = R_{B1} \,||\, R_{B2} = \frac{5.2\text{ K} \times 1.24\text{ K}}{5.2\text{ K} + 1.24\text{ K}} = \mathbf{1\text{ K}}$$

Therefore, equivalent circuit becomes as shown in the Fig. 3.56.

Applying KVL to the base circuit we get,

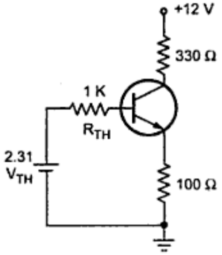


Fig. 3.56

$$V_{TH} - I_B R_{TH} - 0.7 - 101\, I_B R_E = 0$$

$$\therefore \quad I_B = \frac{V_{TH} - 0.7}{R_{TH} + 101\, R_E} = \frac{2.31 - 0.7}{1\text{K} + 101 \times 200}$$

$$= \mathbf{75.94\ \mu A}$$

$$I_C = \beta I_B = 100 \times 75.94\ \mu\text{A} = \mathbf{7.594\text{ mA}}$$

Applying KVL to collector circuit we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 12 - (7.549\text{ mA} \times 330) - (101 \times 75.49\ \mu\text{A} \times 200)$$

$$= 12 - 2.491 - 1.5248 = \mathbf{7.9842\text{ V}}$$

The d.c. load line for the above circuit can be drawn as shown in the Fig. 3.57.

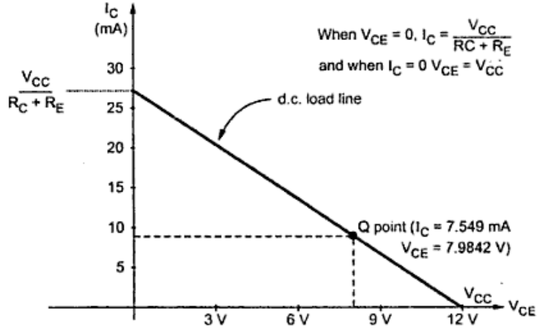


Fig. 3.57

Stability Factor S for Voltage Divider Bias

For determining stability factor S for voltage divider bias we will consider the equivalent circuit as seen in the previous section. Fig. 3.58 shows the Thevenin's equivalent circuit for voltage divider bias.

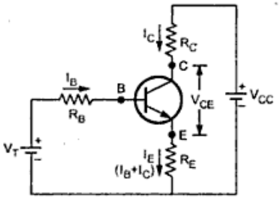


Fig. 3.58 Thevenin's equivalent circuit for voltage divider bias

Here Thevenin's equivalent voltage V_T is given by

$$V_T = \frac{R_2 \times V_{CC}}{R_1 + R_2} \quad \text{and}$$

the R_1 and R_2 are replaced by R_B which is the parallel combination of R_1 and R_2 .

$$\therefore \qquad R_B = \frac{R_1 \, R_2}{R_1 + R_2}$$

Applying KVL to the base circuit we get,

$$V_T = I_B \, R_B + V_{BE} + (I_B + I_C) \, R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\therefore \qquad \frac{\partial I_B}{\partial I_C} (R_E + R_B) = -R_E$$

$$\therefore \qquad \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B} \qquad \dots (15)$$

We have already seen the generalized expression for stability factor S given by

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} \qquad \dots (16)$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the equation (16) we get,

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)} \qquad \dots (17)$$

$$S = \frac{(1+\beta)(R_E + R_B)}{R_B + R_E + \beta R_E} = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$$

Dividing each term by R_E we get,

$$S = (1+\beta)\ \frac{1+R_B/R_E}{(1+\beta)+R_B/R_E} \qquad \ldots (18)$$

From equation (16) we can observe following important points

1. The ratio R_B/R_E controls value of stability factor S. If $R_B/R_E << 1$ then equation (18) reduces to

   $$S = (1+\beta)\cdot\frac{1}{(1+\beta)} = 1 \qquad \ldots (19)$$

   Practically $R_B/R_E \neq 0$. But to have better stability factor S we have to keep ratio R_B/R_E as small as possible.

2. To keep R_B/R_E small, it is necessary to keep R_B small. This means that $R_1 \| R_2$ must be small. Due to small value of R_1 and R_2, potential divider circuit will draw more current from V_{CC} reducing the life of the battery. So while designing if we make R_2 much smaller than R_1 then parallel combination results small R_B without drawing more current through V_{CC}. Another important aspect is that reducing R_B will reduce input impedance of the circuit, since R_B comes in parallel with the input. This reduction of input impedance in amplifier circuits is not desirable and hence R_B cannot be made very small.

3. Emitter resistance R_E is the another parameter we can use to decrease ratio R_B/R_E. By increasing R_E we can make R_B/R_E small. But as we increase R_E, drop $I_E R_E$ will also increase and since V_{CC} is constant, drop across R_C will reduce. This shifts the operating point Q which is not desirable and hence there is limit for increasing R_E.

Thus while designing voltage divider bias circuit we have to find compromising values :

S - Small

R_B - Reasonably small

R_E - Not very large

4. If ratio R_B/R_E is fixed, S increases with β. Therefore stability decreases with increasing β.

5. Stability factor S is essentially independent of β for small value of S.

Key Point : *Stability factor S for voltage divider bias or self bias is less as compare to other biasing circuits studied. So this circuit is more stable and hence it is most commonly used. (Advantage of self bias or voltage divider bias circuit.)*

➡ **Example 3.22 :** *For a circuit shown in Fig. 3.59, $V_{CC} = 20$ V, $R_C = 2$ kΩ, $\beta = 50$, $V_{BEact} = 0.2$ V, $R_1 = 100$ kΩ, $R_2 = 5$ kΩ and $R_E = 100$ Ω. Calculate I_B, V_{CE}, I_C and stability factor S.*

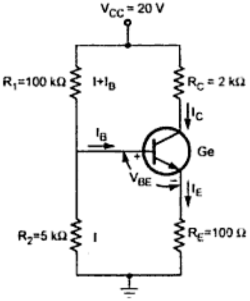


Fig. 3.59

Solution :

$$V_{CC} = R_1 [I + I_B] + I R_2$$

$$\therefore \quad I = \frac{V_{CC} - I_B R_1}{R_1 + R_2}$$

$$V_{CC} = R_1 [I + I_B] + V_{BE} + I_E R_E$$

We know that, $I_E = I_B + I_C = I_B + \beta I_B$

$$\therefore \quad V_{CC} = R_1 [I + I_B] + V_{BE} + (1+\beta) I_B R_E$$

Substituting value of I we get,

$$V_{CC} = R_1 \left[\frac{V_{CC} - I_B R_1}{R_1 + R_2} + I_B\right] + V_{BE} + (1+\beta) I_B R_E$$

$$= R_1 \left[\frac{V_{CC} - I_B R_1 + I_B R_1 + I_B R_2}{R_1 + R_2}\right] + V_{BE} + (1+\beta) I_B R_E$$

$$= R_1 \left[\frac{V_{CC} + I_B R_2}{R_1 + R_2}\right] + V_{BE} + (1+\beta) I_B R_E$$

Substituting values of V_{CC}, R_1, R_2, V_{BE}, β and R_E

We get,

$$20 = 100 \times 10^3 \left[\frac{20 + I_B \times 5 \times 10^3}{100 \times 10^3 + 5 \times 10^3}\right] + 0.2 + (51) I_B \times 100$$

$$20 = 19.047619 + 4761.9\, I_B + 0.2 + 5100\, I_B$$

$$0.752381 = 9861.9\, I_B$$

$$\therefore \quad I_B = 76.29\ \mu A$$

As $\quad I_C = \beta I_B = 50 \times 76.29\ \mu A = 3.814$ mA

Applying KVL to collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + (1+\beta) I_B R_E$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - (1+\beta) I_B R_E$$

$$\therefore \quad V_{CE} = 20 - 3.814 \times 10^{-3} \times 2 \times 10^{3} - (51) \times 76.29 \times 10^{-6} \times 100$$

$$= 11.983 \text{ V}$$

Stability factor for voltage divider bias is given as

$$S = \frac{\beta + 1}{1 + \beta \dfrac{R_E}{R_E + R_B}}$$

Before substituting the values in the equation it is necessary to calculate R_B.

We know that $R_B = R_1 \,||\, R_2$

$$= \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10^3 \times 5 \times 10^3}{100 \times 10^3 + 5 \times 10^3} = 4761.9 \ \Omega$$

Now substituting values of , R_E and β in the equation of stability factor we get,

$$S = \frac{50 + 1}{1 + 50 \times \dfrac{100}{100 + 4761.9}} = 25.143$$

Example 3.23 : *For the circuit shown in Fig. 3.60* $I_C = 2$ *mA,* $\beta = 100$*, calculate* R_E *,* V_{CE} *and stability factor S.*

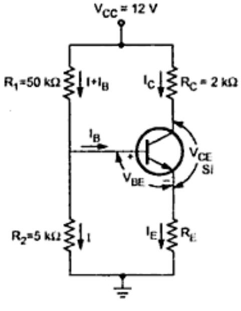


Fig. 3.60

Solution : $I_C = \beta I_B$

$$\therefore \quad I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{100} = 20\ \mu\text{A}$$

Applying KVL to voltage divider we get,

$$V_{CC} - R_1 [I + I_B] - R_2 I = 0$$

$$\therefore\ 12 - 50\times10^3 \times (I + 20\times10^{-6}) - 5\times10^3 (I) = 0$$

$$12 - 50\times10^3\ I - 1 - 5\times10^3\ I = 0$$

$$\therefore \quad 11 = 55000\ I$$

$$\therefore \quad I = 0.2\text{ mA}$$

$$\therefore \quad V_B = R_2 \times I = 5\times10^3 \times 0.2\times10^{-3} = 1\text{ V}$$

We know that,

$$V_B = V_{BE} + I_E R_E = V_{BE} + (I_B + I_C) R_E$$

$$1 = 0.7 + (20\times10^{-6} + 2\times10^{-3}) R_E$$

$$\therefore \quad R_E = 148.51\ \Omega$$

Applying KVL to collector circuit we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

$$= 12 - 2\times10^{-3} \times 2\times10^{3} - (20\times10^{-6} + 2\times10^{-3})\times148.51$$

$$= 7.70\text{ V}$$

Stability factor for voltage divider bias is given as

$$S = \frac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_E + R_B}\right)}$$

Before substituting the values in the equation it is necessary to calculate R_B.

We know that

$$R_B = R_1 \parallel R_2$$

$$= \frac{R_1 R_2}{R_1 + R_2} = \frac{50\times10^3 \times 5\times10^3}{50\times10^3 + 5\times10^3}$$

$$= 4.545\text{ k}\Omega$$

Now substituting values of R_B, R_E and β in the equation of stability factor we get,

$$S = \frac{100+1}{1+100\times\dfrac{148.51}{148.51+4.545\times10^{3}}} = \mathbf{24.254}$$

Example 3.24 : *Design a voltage divider bias circuit for the specified conditions.* $V_{CC} = 12\ V$, $V_{CE} = 6\ V$, $I_C = 1\ mA$, $S = 20$, $\beta = 100$ *and* $V_E = 1\ V$

Solution :

$$I_B = \frac{I_C}{\beta} = \frac{1\text{mA}}{100} = 10\ \mu\text{A}$$

$$I_E = I_B + I_C = 10\ \mu\text{A} + 1\ \text{mA} = 1.01\ \text{mA}$$

$$R_E = \frac{V_E}{I_E} = \frac{1\text{V}}{1.01\ \text{mA}} = 990\ \Omega$$

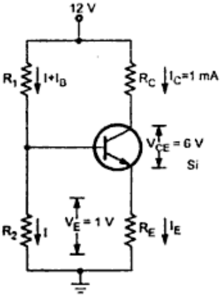


Fig. 3.61

We know that

$$S = \frac{1+\beta}{1+\beta\dfrac{R_E}{R_E+R_B}}$$

$$20 = \frac{1+100}{1+100\times\dfrac{990}{990+R_B}}$$

$$20 = \frac{101}{1+\dfrac{99000}{990+R_B}}$$

$$20 = \frac{101}{\dfrac{990+R_B+99000}{990+R_B}}$$

$$20 = \frac{101\,(990+R_B)}{990+R_B+99000}$$

$$20\,(990+R_B+99000) = 101\,(990+R_B)$$

$$19800 + 20R_B + 1980000 = 99990 + 101R_B$$

$$1899810 = 81\ R_B$$

$$\therefore \quad R_B = 23454.5\ \Omega$$

We know, $V_B = V_{BE} + V_E = 0.7 + 1 = 1.7\ V$

$\therefore$ Drop across R_2 = **1.7**

and drop across $R_1 = 12 - 1.7 = 10.3$

We know that,
$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$\therefore \quad \frac{R_1 R_2}{R_1 + R_2} = 23454.5$$

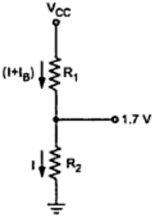


Fig. 3.62

Fig. 3.62 shows that current through R_1 is $I+I_B$. R_1 can be calculated as
$$R_1 = \frac{10.3}{I+I_B}$$

Similarly R_2 can be calculated as
$$R_2 = \frac{1.7}{I}$$

Now, substituting values of R_1 and R_2 we can write
$$R_B = \frac{\dfrac{10.3}{I+10\times 10^{-6}} \times \dfrac{1.7}{I}}{\dfrac{10.3}{I+10\times 10^{-6}} + \dfrac{1.7}{I}}$$

$$\therefore \quad 23454.5 = \frac{\dfrac{10.3}{I+10\times 10^{-6}} \times \dfrac{1.7}{I}}{\dfrac{10.3}{I+10\times 10^{-6}} + \dfrac{1.7}{I}} = \frac{\dfrac{10.3\times 1.7}{(I+10\times 10^{-6})\,I}}{\dfrac{10.3\,I+1.7\,(I+10\times 10^{-6})}{(I+10\times 10^{-6})\,I}}$$

$$= \frac{10.3\times 1.7}{10.3\,I+1.7\,(I+10\times 10^{-6})}$$

$$\therefore \; 23454.5\left[(10.3\,I)+1.7\,(I+10\times 10^{-6})\right] = 17.51$$

$$241581.35\,I + 39872.65\,I + 0.3987265 = 17.51$$

$$\therefore \quad 281454\,I = 17.111274$$

$$\therefore \quad I = \mathbf{60.8\ \mu A}$$

Substituting value of I in equation of R_1 and R_2
$$R_1 = \frac{10.3}{(60.8\times 10^{-6}+10\times 10^{-6})} = \mathbf{145480\ \Omega}$$

$$R_2 = \frac{1.7}{60.8 \times 10^{-6}} = \mathbf{27960.5\ \Omega}$$

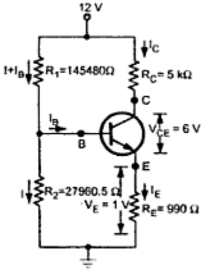


Fig. 3.63

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$I_C R_C = V_{CC} - V_{CE} - I_E R_E$$

$$\therefore \quad R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$

$$= \frac{12 - 6 - 1}{1 \times 10^{-3}} = \frac{5}{1 \times 10^{-3}}$$

$$= \mathbf{5\ k\Omega}$$

Fig. 3.63 shows the voltage divider bias circuit with designed values.

Stability Factor S′

Stability factor S′ is given by

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO}, \beta \text{ constant}}$$

It is the variation of I_C with V_{BE} when I_{CO} and β are considered constant.

We know that,

$$I_C = (1 + \beta) I_{CO} + \beta I_B \qquad \text{... (20)}$$

and $$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$\therefore \quad V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C \qquad \text{... (21)}$$

By writing equation (20) in terms of I_B we get,

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta} \qquad \text{... (22)}$$

Now, substituting I_B in equation (22) we get,

$$V_{BE} = V_T - (R_E + R_B)\left[\frac{I_C - (1+\beta) I_{CO}}{\beta}\right] - R_E I_C$$

$$= V_T - \frac{(R_E + R_B) I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} - R_E I_C$$

$$\therefore \quad V_{BE} = V_T - \frac{[(1+\beta) R_E + R_B\ ] I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} \qquad \text{... (23)}$$

Differentiating the equation (23) w.r.t. V_{BE} with I_{CO} and β constant we get,

$$1 = 0 - \frac{[R_B + (1+\beta)R_E]}{\beta} \frac{\partial I_C}{\partial V_{BE}} + 0$$

$$\therefore \quad \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E} \qquad \text{... (24)}$$

$$\therefore \quad S' = \frac{-\beta}{R_B + (1+\beta)R_E} \qquad \text{... (25)}$$

Relation Between S and S′

We know from equation (17)

$$S = 1+\beta \frac{1+R_B/R_E}{1+\beta+R_B/R_E}$$

Multiplying both denominator and numerator by R_E we get,

$$S = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E} \qquad \text{... (26)}$$

$$\therefore \quad \frac{S}{(1+\beta)(R_E+R_B)} = \frac{1}{R_B+(1+\beta)R_E}$$

Substituting value of $\frac{1}{R_B+(1+\beta)R_E}$ in equation (25) we get,

$$S' = -\beta \frac{S}{(1+\beta)(R_E+R_B)} = -\frac{S}{(R_E+R_B)} \cdot \frac{\beta}{(1+\beta)} \qquad \text{... (27)}$$

From equation (27) we can see that lower the value of S, lower is the value of S′. Thus as we reduce S towards unity, we minimize the change of I_C with respect to both, V_{BE} and I_{CO}.

Stability Factor S″

Stability factor S″ is given by

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE}\text{ constant}}$$

It is the variation of I_C with β when I_{CO} and V_{BE} are considered constant. We recall equation (23) which is

$$V_{BE} = V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + \left[\frac{(R_E+R_B)(1+\beta)}{\beta}\right] I_{CO}$$

$$= V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + V' \qquad \text{... (28)}$$

where $$V' = \left[\frac{(R_B + R_E)(\beta + 1)}{\beta}\right] I_{CO} = (R_B + R_E) I_{CO} \qquad \because \ \beta >> 1$$

If we write equation (28) in terms of I_C we get,

$$I_C = \frac{\beta(V_T + V' - V_{BE})}{R_B + R_E(1+\beta)} \qquad \ldots (29)$$

Differentiating equation (29) and taking V' independent of β, we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + R_E(1+\beta)(V_T + V' - V_{BE}) - \beta(V_T + V' - V_{BE}) R_E}{(R_B + R_E(1+\beta)^2)}$$

$$\left[\ \textbf{Hint:}\ \frac{d}{dt}\left(\frac{u}{v}\right) = \frac{v \times \frac{du}{dt} - u \times \frac{dv}{dt}}{v^2}\ \right]$$

Multiplying numerator and denominator by $(1 + \beta)$ we get,

$$= \frac{(1+\beta)(R_B + R_E)(V_T + V' - V_{BE})}{(1+\beta)[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]}$$

$$= \frac{S(V_T + V' - V_{BE})}{(1+\beta)[R_B + R_E(1+\beta)]}$$

Since $$S = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$$ from equation (26)

Multiplying numerator and denominator by β we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{\beta(V_T + V' - V_{BE}) S}{\beta(1+\beta)[R_B + R_E(1+\beta)]} = \frac{I_C S}{\beta(1+\beta)} \qquad \ldots (30)$$

Since $$I_C = \frac{\beta(V_T + V' - V_{BE})}{[R_B + R_E(1+\beta)]}$$

$\therefore$ $$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C S}{\beta(1+\beta)} \qquad \ldots (31)$$

Thus, change in collector current due to change in β is

$$\partial I_C = S'' \partial \beta = \frac{I_C S}{\beta(1+\beta)} \partial \beta \qquad \ldots (32)$$

where $\partial \beta = \beta_2 - \beta_1$ may represent a large change in β. Hence it is not clear whether to use β_1, β_2, S'' is obtained by taking finite differences rather than by evaluating a derivative.

Thus $$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_{C2} - I_{C1}}{\beta_2 - \beta_1} \qquad \ldots (33)$$

We know that,
$$I_C = \frac{\beta(V_T + V' - V_{BE})}{R_B + R_E(1+\beta)}$$

$$\therefore \quad \frac{I_{C2}}{I_{C1}} = \frac{\beta_2[R_B + R_E(1+\beta_1)]}{\beta_1[R_B + R_E(1+\beta_2)]}$$

Subtracting (1) from both sides we get,

$$\frac{I_{C2} - I_{C1}}{I_{C1}} = \frac{\beta_2[R_B + R_E(1+\beta_1)] - \beta_1[R_B + R_E(1+\beta_2)]}{\beta_1(R_B + R_E(1+\beta_2))}$$

$$\therefore \quad \frac{\partial I_C}{I_{C1}} = \frac{\beta_2 R_B + \beta_2 R_E + \beta_1 \beta_2 R_E - \beta_1 R_B - \beta_1 R_E - \beta_1 \beta_2 R_E}{\beta_1(R_B + R_E(1+\beta_2))}$$

$$= \frac{\beta_2(R_B + R_E) - \beta_1(R_B + R_E)}{\beta_1(R_B + R_E(1+\beta_2))} = \left(\frac{\beta_2 - \beta_1}{\beta_1}\right)\left(\frac{R_B + R_E}{R_B + R_E(1+\beta_2)}\right)$$

$$= \frac{\partial \beta}{\beta_1} \cdot \frac{R_B + R_E}{R_B + R_E(1+\beta_2)}$$

$$\therefore \quad \frac{\partial I_C}{\partial \beta} = \frac{I_{C1}}{\beta_1} \frac{R_B + R_E}{R_B + R_E(1+\beta_2)}$$

Multiplying numerator and denominator of R.H.S. by $(1 + \beta)$ we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{I_{C1}}{\beta_1} \frac{(R_B + R_E)(1+\beta)}{R_B + R_E(1+\beta_2)(1+\beta)}$$

$$\therefore \quad S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_{C1} S_2}{\beta_1(1+\beta_2)} \qquad \dots (34)$$

Since
$$S_2 = S = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$$

When $\beta = \beta_2$

As $\partial \beta = \beta_2 - \beta_1 \rightarrow 0$ equation (33) reduces to equation (31).

Key Point : *It is clear from equation (34) that minimizing S also minimizes S″. This means that the ratio R_B/R_E must be small to have better stability factor S″.*

3.10 Emitter Stabilized Bias Circuit

To improve the stability of the biasing circuit over the fixed bias circuit, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as **emitter bias circuit** and it is shown in the Fig. 3.64

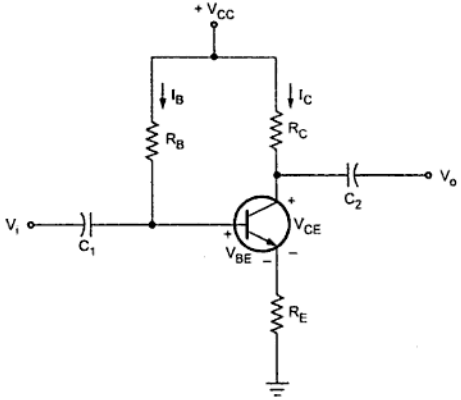

+ V_{CC}
I_B
R_B
I_C
R_C
V_o
C_2
V_i
C_1
+
V_{CE}
−
+
V_{BE}
−
R_E

Fig. 3.64 Emitter bias circuit

3.10.1 Circuit Analysis

Base Circuit

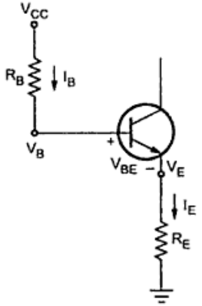

V_{CC}
R_B
I_B
V_B
+
V_{BE}
−
V_E
I_E
R_E

Fig. 3.65 Base circuit

Let us consider the base circuit shown in the Fig. 3.65.

Applying KVL to the base circuit we get,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad ...(35)$$

We have,

$$I_E = (1+\beta) I_B$$

I_E in equation (35) we get,

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$\therefore \; V_{CC} - V_{BE} = I_B R_B + (1+\beta) \; I_B R_E$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E}} \qquad \because \beta >> 1$$

Note that the only difference between the equation for I_B and that obtained for the fixed-bias configuration is the term βR_E.

$$V_B = V_{BE} + V_E \quad \text{or} \quad V_{CC} - I_B R_B$$

Since $\quad V_E = I_E R_E$

$$\boxed{V_B = V_{BE} + I_E R_E}$$

Collector Circuit

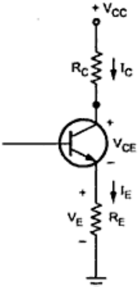


Fig. 3.66

We now consider the collector circuit as shown in the Fig. 3.66. Applying KVL to the collector circuit we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\boxed{V_C = V_{CC} + I_C R_C - I_E R_E}$$

$$\boxed{V_E = I_E R_E}$$

$$\boxed{V_{CE} = V_C - V_E}$$

$$\boxed{V_C = V_{CC} - I_C R_C}$$

Example 3.25 : *For the circuit shown in Fig. 3.67, calculate I_B, I_C, V_{CE}, V_C, V_E, V_B and V_{BC}. Assume $\beta = 100$.*

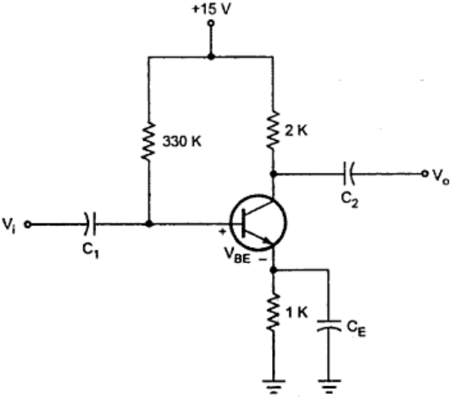


Fig. 3.67

Solution :

$$I_B = \frac{V_{CC}-V_{BE}}{R_B+(1+\beta)R_E} = \frac{15-0.7}{330\times10^3+(1+100)\times10^3}$$

$$= \mathbf{33.18\ \mu A}$$

$$I_C = \beta I_B = 100 \times 33.18\ \mu A = \mathbf{3.318\ mA}$$

$$I_E = I_B + I_C = \mathbf{3.351\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 15 - 3.318 \times 10^{-3} \times 2\times10^3 - 3.351 \times 10^{-3} \times 1\times10^3$$

$$= \mathbf{5\ V}$$

$$V_C = V_{CC} - I_C R_C = 15 - 3.318\times10^{-3}\times2\times10^3$$

$$= \mathbf{8.364\ V}$$

$$V_E = I_E R_E = 3.351\times10^{-3}\times1\times10^3$$

$$= \mathbf{3.351\ V}$$

$$V_B = V_E + V_{BE} = 3.351 + 0.7 = \mathbf{4.051\ V}$$

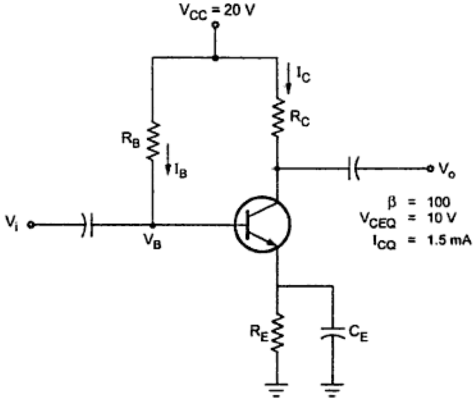
$$V_{BC} = V_B - V_C = 4.051 - 8.364$$

$$= \mathbf{-4.313\ V}$$

3.10.2 Stability Improvement

The addition of the emitter resistance, R_E in the emitter bias circuit provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit against the changes in temperature and transistor β (beta).

➡ **Example 3.26 :** *Determine the resistor values of the circuit shown in the Fig. 3.68 for given operating point and supply voltage.*



$V_{CC} = 20$ V
I_C
R_C
R_B
I_B
V_o
$\beta = 100$
$V_{CEQ} = 10$ V
$I_{CQ} = 1.5$ mA
V_i
V_B
R_E
C_E

Fig. 3.68

Solution : Let us assume that $V_E = \frac{1}{10}$ of V_{CC}, therefore

$$V_E = 2 \text{ V}$$

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.5\,\text{mA}}{100} = 15\ \mu\text{A}$$

$$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_B + I_C} = \frac{2}{15\times10^{-6} + 1.5\times10^{-3}} = \mathbf{1.32\ k\Omega}$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20-10-2}{1.5\times10^{-3}}$$

$$= \mathbf{5.33\ k\Omega}$$

$$R_B = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20-0.7-2}{15\times10^{-6}}$$

$$= \mathbf{1.15\ M\Omega}$$

The stability factor S for emitter stabilized bias circuit is same as that of voltage divider bias circuit.

3.11 Comparison of Biasing Circuits

The Table 3.6 shows the comparison of biasing circuits

Sr. No.	Parameter	Fixed Bias	Collector to Base Bias	Self Bias or Voltage Divider Bias
1.	Resistors required	1	1	3
2.	Stability provided	Poor	Medium	More
3.	Simplicity of the circuit	More	More	Less
4.	Feedback provided	No	Negative (Voltage shunt)	Negative (Current series)

Table 3.6 Comparison of biasing circuits

Examples with Solutions

➡ **Example 3.27 :** *For the transistor shown in Fig. 3.69, the value of* β *is 100. Calculate the value of* R_B *that will just saturate the transistor. Assume* $V_{CE_{sat}} = 0.3$ V.

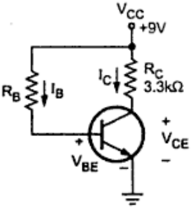


Fig. 3.69

Solution : Given : $V_{CC} = 9$ V, $V_{CE(sat)} = 0.3$ V, $\beta = 100$

Apply KVL to collector side

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \quad 9 = I_C (3.3\text{ K}) + 0.3$$

$$\therefore \quad I_C = \frac{9-0.3}{3.3\text{ K}}\text{ A}$$

$$= 2.636\text{ mA}$$

If the transistor is to be just saturated then

$$V_{BE} = 0.7\ V$$

and $$I_B = \frac{I_C}{\beta_{dc}}$$

$$= \frac{2.636\ mA}{100} = 26.36\ \mu A$$

Apply KVL to base side

$$V_{CC} = I_B R_B + V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{9 - 0.7}{26.36\mu A}\ \Omega$$

$$= 314.87\ k\Omega$$

➡ **Example 3.28 :** *In the circuit shown in Fig. 3.70, for R_B = 300 kΩ, and R_B =150 kΩ calculate I_B, I_C and V_{CE} and determine region of operation.*

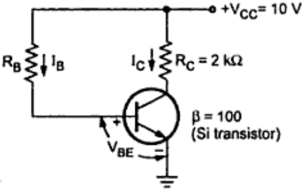


Fig. 3.70

Solution : i) R_B = 300 kΩ

Since base emitter junction is not reverse biased, we can say that transistor is not in cut-off region .

Assume transistor is operating in an active region.

Applying KVL around base loop we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore \quad 10 = I_B \times 300 \times 10^3 + 0.7\ V$$

$$\therefore \quad I_B = \frac{9.3}{300 \times 10^3}$$

$$I_B = 0.031\ mA$$

$$= 31\ \mu A$$

In active region $I_C = \beta I_B$

$$\therefore \quad I_C = 100 \times 31\ \mu A$$

$$= 3.1\ mA$$

Now, applying KVL around collector loop we get,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \quad 10 = 3.1 \times 10^{-3} \times 2 \times 10^{3} + V_{CE}$$

$$\therefore \quad V_{CE} = 10 - 6.2$$

$$= 3.8\ V$$

As V_{CE} is equal to 3.8 V, collector to base junction is reverse biased and we can say that our assumption that transistor is in active region is justified.

ii) R_B = 150 kΩ

Since base emitter junction is not reverse biased we can say that transistor is not in cut-off region.

Assume transistor is operating in an active region.

Applying KVL around base loop we get,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore \quad 10 = I_B \times 150 \times 10^{3} + 0.7$$

$$\therefore \quad I_B = \frac{9.3}{150 \times 10^{3}} = 0.062\ mA$$

$$= 62\ \mu A$$

In active region $I_C = \beta I_B$

$$\therefore \quad I_C = 100 \times 62\ \mu A$$

$$= 6.2\ mA$$

Now, applying KVL around collector loop we get,

$$V_{CC} = I_C R_C + V_{CE}$$

$$\therefore \quad 10 = 6.2 \times 10^{-3} \times 2 \times 10^{3} + V_{CE}$$

$$\therefore \quad V_{CE} = 10\ V - 12.4\ V$$

$$= -2.4\ V$$

It is important to note that collector voltage has to be positive or zero. Hence our assumption that transistor is in active region is wrong and it is in saturation region.

Applying KVL around base loop we get,

$$V_{CC} = I_B R_B + V_{BE\,sat}$$

$$10 = I_B(150\times10^3)+0.8\text{ V}$$

$$\therefore \qquad I_B = \frac{9.2}{150\times10^3} = 61.33\ \mu\text{A}$$

Applying KVL around collector loop we get,

$$V_{CC} = I_C R_C + V_{CE(sat)}$$

$$10 = I_C(2\times10^3)+0.2\text{ V}$$

$$\therefore \qquad I_C = \frac{9.8}{2\times10^3} = 4.9\text{ mA}$$

To justify that transistor is in saturation

$$I_B > \frac{I_C}{\beta}$$

$$\frac{I_C}{\beta} = \frac{4.9\times10^{-3}}{100} = 49\ \mu\text{A}$$

Therefore $\frac{I_C}{\beta}$ is less than I_B and our assumption that transistor in saturation is justified.

➠ **Example 3.29 :** *CB transistor is biased using single D.C. source. The transistor is silicon with V_{BEQ} = 0.7 volts, β = 99 and I_{BQ} = 30 μA. Find a) R_2 b) V_{CEQ}.*

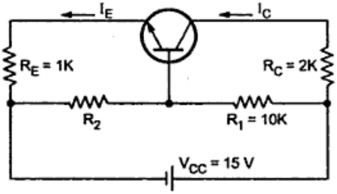


Fig. 3.71

Solution : $I_{CQ} = \beta I_{BQ} = 99 \times 30 \times 10^{-6}$

$$= 2.97 \text{ mA}$$

$$\therefore \quad I_E = I_C + I_B = 2.97 \times 10^{-3} + 30 \times 10^{-6} = 3 \text{ mA}$$

Applying KVL to collector-emitter side,

$$V_{CC} = I_{CQ} R_C + V_{CEQ} + I_E R_E$$

$$\therefore \quad 15 = 2.97 \times 10^{-3} \times 2 \times 10^3 + V_{CEQ} + 3 \times 10^{-3} \times 1 \times 10^3$$

$$\therefore \quad V_{CEQ} = 6.06 \text{ volts.}$$

Voltage at the base

$$V_B = I_E R_E + V_{BEQ}$$

$$\therefore \quad V_B = 3 \times 10^{-3} \times 1 \times 10^3 + 0.7$$

$$\therefore \quad V_B = 3.7 \text{ V}$$

Applying KVL to voltage divider circuit we have,

$V_{CC} = (I + I_B) R_1 + V_B$ . . . . . . By taking current through R_2 as I and hence through R_1 as $I + I_B$

$$\therefore \quad 15 = (I + I_B) R_1 + 3.7$$

$$\therefore \quad I + I_B = \frac{15 - 3.7}{10 \times 10^3} = 1.13 \text{ mA}$$

$$\therefore \quad I = 1.13 \times 10^{-3} - 30 \times 10^{-6} = 1.1 \text{ mA}$$

We know that, $V_B = R_2 I$

$$\therefore \quad R_2 = \frac{V_B}{I} = \frac{3.7}{1.1 \times 10^{-3}} = 3.363 \text{ k}\Omega$$

➡ **Example 3.30 :** *In the circuit shown in Fig. 3.72 transistor has* $\beta = 100$ *and* $V_{BE(active)} = 0.6$ *V. Calculate the values of* R_1 and R_3 *such that collector current of 1 mA and* $V_{CE} = 2.5$ *V.*

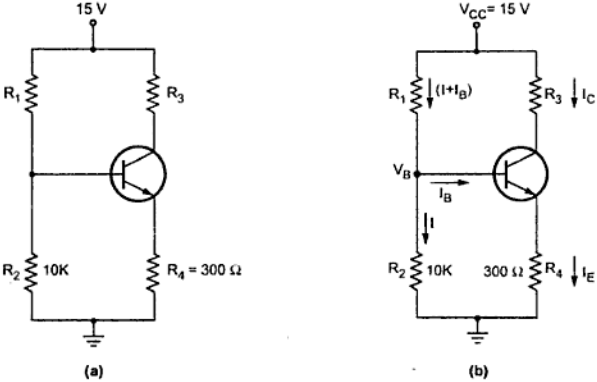


Fig. 3.72

Solution : Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_3 - V_{CE} - I_E R_4 = 0$$

$$\therefore \quad V_{CC} - I_C R_3 - V_{CE} - (I_C + I_B) R_4 = 0$$

$$\beta = \frac{I_C}{I_B}, \quad \therefore \quad I_B = \frac{I_C}{\beta}$$

$$\therefore \quad V_{CC} - I_C R_3 - V_{CE} - \left(I_C + \frac{I_C}{\beta}\right) R_4 = 0$$

$$\therefore \quad V_{CC} - I_C R_3 - V_{CE} - \left(1 + \frac{1}{\beta}\right) I_C R_4 = 0$$

$$\therefore \quad 15 - 1 \times 10^{-3} \times R_3 - 2.5 - \left(1 + \frac{1}{100}\right) \times 1 \times 10^{-3} \times 300 = 0$$

$$\therefore 12.197 - 10^{-3} \times R_3 = 0$$

$$\therefore \quad R_3 = \frac{12.197}{10^{-3}}$$

$$\therefore \quad R_3 = 12.197 \text{ k}\Omega$$

$$I_B = \frac{I_C}{\beta}$$

$$\therefore \quad I_B = \frac{1 \times 10^{-3}}{100}$$

$$\therefore \quad I_B = 10\ \mu A$$

$$I_E = I_C + I_B$$

$$\therefore \quad I_E = 1\times 10^{-3} + 10\times 10^{-6}$$

$$\therefore \quad I_E = 1.01\ mA$$

Voltage at the base,

$$V_B = I_E\ R_4 + V_{BE}$$

$$\therefore \quad V_B = 1.01\times 10^{-3}\times 300 + 0.6$$

$$\therefore \quad V_B = 0.903V$$

Using approximate analysis :

Voltage at the base can also be given as,

$$V_B = \frac{R_2}{R_1 + R_2}\times V_{CC} \ldots\ldots \quad \because\ I >> I_B$$

$$\therefore \quad 0.903 = \frac{10\times 10^3}{R_1 + 10\times 10^3}\times 15$$

$$\therefore \quad R_1 = \frac{10\times 10^3\times 15}{0.903} - 10\times 10^3$$

$$\therefore \quad R_1 = 10\times 10^3\left(\frac{15}{0.903} - 1\right)$$

$$\therefore \quad R_1 = 156.11\ k\Omega$$

Using exact analysis :

Current through R_2,

$$I = \frac{V_B}{R_2}$$

$$\therefore \quad I = \frac{0.903}{10\times 10^3}$$

$$\therefore \quad I = 90.3\ \mu A$$

Current through R_1,

$$I + I_B = 90.3\times 10^{-6} + 10\times 10^{-6}$$

$$= 100.3\ \mu A$$

Voltage across R_1,

$$V_{CC} - V_B = R_1\ (I + I_B\ )$$

$$\therefore \quad 15 - 0.903 = R_1 \times 100.3 \times 10^{-6}$$

$$\therefore \quad R_1 = 140.54 \text{ k}\Omega$$

➡ **Example 3.31 :** *A Ge transistor used in self bias circuit has $V_{CC} = 20$ V, $R_C = 2$ K. The nominal operating point is $V_{CE} = 10$ V and $I_C = 4$ mA. If $h_{FE} = 50$, calculate R_1, R_2 and R_E if stability factor $S = \frac{\partial I_C}{\partial I_{CO}} = 10$ is desired. If $S \leq 3$ is required, what will be the "price paid"?*

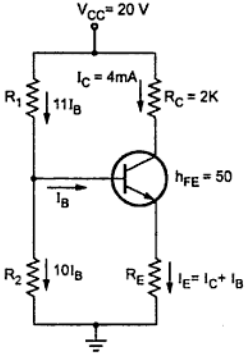


Fig. 3.73

Solution :

$$I_B = \frac{I_C}{\beta} = \frac{4 \times 10^{-3}}{50}$$

$$= 80 \ \mu\text{A}$$

Applying KVL to the collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$I_E = I_C + I_B$$

$$\therefore \quad V_{CC} = I_C R_C + V_{CE} + (I_C + I_B) R_E$$

$$\therefore \quad R_E = \frac{V_{CC} - V_{CE} - I_C R_C}{I_C + I_B}$$

$$\therefore \quad R_E = \frac{20 - 10 - 4 \times 10^{-3} \times 2 \times 10^3}{4 \times 10^{-3} + 80 \times 10^{-6}}$$

$$\therefore \quad R_E = 0.49 \text{ K}$$

$$S = (1+\beta)\left[\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}\right]$$

$$S = 10$$

$$\therefore \quad 10 = 51 \times \frac{1+\frac{R_B}{490}}{51+\frac{R_B}{490}}$$

$$\therefore \quad R_B = 5.485 \text{ K}$$

Voltage at the base,

$$V_B = V_{BE} + I_E R_E$$

$$\therefore \quad V_B = 0.3 + R_E (I_C + I_B)$$

$$\therefore \quad V_B = 0.3 + 0.49 \times 10^3 (4 \times 10^{-3} + 80 \times 10^{-6})$$

$$\therefore \quad V_B = 2.29 \text{ V}$$

Voltage at the base is the voltage across R_2.

$$\therefore \quad V_B = 10\, I_B \times R_2$$

$$\therefore \quad 2.29 = 10 \times 80 \times 10^{-6} \times R_2$$

$$\therefore \quad R_2 = 2.862 \text{ k}\Omega$$

Voltage across $R_1 = V_{CC} - V_B$

$$\therefore \quad 11\, I_B \times R_1 = V_{CC} - V_B$$

$$\therefore \quad 11 \times 80 \times 10^{-6} R_1 = 20 - 2.29$$

$$\therefore \quad R_1 = 20.125 \text{ k}\Omega$$

If $S \leq 3$, value of R_B will be,

$$3 = 51 \times \frac{1+\frac{R_B}{490}}{51+\frac{R_B}{490}}$$

Solving for R_B we get ,

$$R_B = 1041\ \Omega$$

Thus, value of R_B is reduced from 5.485 kΩ to 1.041 kΩ . As we know there are two major drawbacks of small value of R_B.

1) It draws more current from battery reducing life of battery.

2) Reducing value of R_B reduces the input impedance of the circuit.

➡ **Example 3.32 :** *For the emitter bias network of Fig 3.74, determine I_B, I_C, V_{CE}, V_B and V_o.*

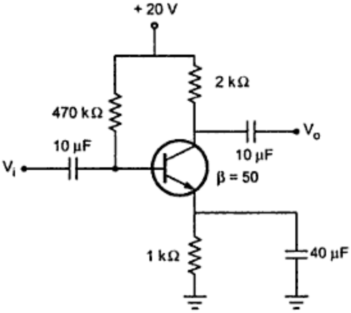

+ 20 V
2 kΩ
470 kΩ
10 µF
V_i
V_o
10 µF
β = 50
1 kΩ
40 µF

Fig. 3.74

Solution : Assuming transistor in active region.

In active region, V_{BE} = 0.7 V

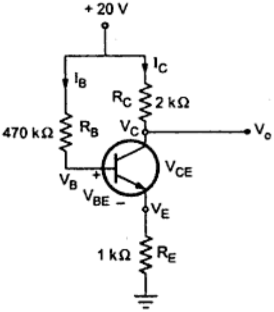

+ 20 V
I_C
I_B
R_C
2 kΩ
470 kΩ
R_B
V_C
V_o
V_{CE}
V_B
+
V_{BE}
–
V_E
1 kΩ
R_E

Fig. 3.74 (a)

Applying KVL to base circuit we have,

$$20 = I_B R_B + V_{BE} + I_E R_E = I_B R_B + V_{BE} + (\beta+1)\, I_B\, R_E$$

$$20 - V_{BE} = I_B \{ R_B + (\beta+1) R_E \}$$

$$\therefore \quad I_B = \frac{20-0.7}{R_B+(\beta+1)R_E} = \frac{20-07}{470+51\times1} = 37\ \mu A$$

$$I_C = \beta I_B = 50\times 37\mu A = 1.85\ mA$$

Applying KVL to collector circuit we have,

$$20 = I_C R_C + V_{CE} + R_E I_E$$

$$I_E = (1+\beta)I_B = 51\times 37\,\mu A = 1.887\,\mu A$$

$$20 = I_C R_C + V_{CE} + R_E\,(1+\beta)\,I_B$$

$$20 - V_{CE} = 1.85\times10^{-3}\times2\times10^3 + 1\times10^3(1+50)\times37\times10^{-6}$$

$$20 - V_{CE} = 5.587\ V$$

$$\therefore \quad V_{CE} = 14.413\ V$$

$$V_E = I_E R_E = 1.887\times10^{-3}\times1\times10^3 = 1.887\ V$$

$$V_o = V_C = V_{CC} - I_C R_C$$

$$= 20 - 1.85\times 2$$

$$= 16.3\ V$$

$$V_B = V_{BE} + V_E$$

$$= 0.7 + 1.887\ V$$

$$= 2.587\ V$$

Example 3.33 : *The circuit shown in Fig. 3.75 in CE germanium transistor amplifier, self-biased. The various parameters are :*

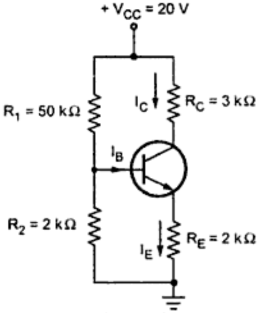


Fig. 3.75

$V_{CC} = 20\ V$, $R_C = 3\ k\Omega$, $R_E = 2\ k\Omega$

$R_1 = 50\ k\Omega$, $R_2 = 2\ k\Omega$, $\alpha = 0.985$

Find operating points and stability factor.

(Dec.- 2002)

Solution : Given $V_{CC} = 20$ V, $R_C = 3$ kΩ, $R_E = 2$ kΩ

$R_1 = 50$ kΩ, $R_2 = 2$ kΩ, $\alpha = 0.985$

$$V_{TH} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{2 \times 20}{2+50} = \frac{40}{52} = 0.769 \text{ V}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{2 \times 52}{50+2} = \frac{104}{52} = 1.923 \text{ K}$$

Applying KVL for base circuit we have,

Since I_B is very small,

$$\therefore \quad I_C \approx I_E$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E} = \frac{0.769 - 0.7}{2 \times 10^3} = 34.5\ \mu\text{A}$$

$$I_C = \alpha\, I_E = 0.985 \times 34.5 \mu\text{A}$$

$$= 34\ \mu\text{A}$$

$$\beta = \frac{\alpha}{1-\alpha} = 66$$

$$I_B = \frac{I_C}{\beta} = \frac{34\ \mu\text{A}}{66} = 0.515\ \mu\text{A}$$

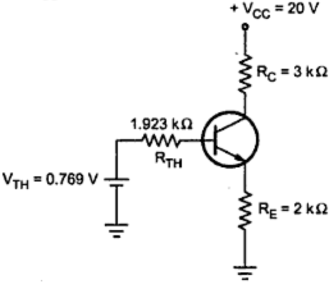


Fig. 3.75 (a)

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 20 - 34 \times 10^{-6} \times 3 \times 10^3 - 34.5 \times 10^{-6} \times 2 \times 10^3$$

$$= 19.829 \text{ V}$$

So operating point (V_{CE}, I_C) = (19.829 V, 34 μA)

ii) Stability factor : $S = \dfrac{\beta+1}{1+\beta\left(\dfrac{R_E}{R_B+R_E}\right)}$

$$\frac{66+1}{1+66\left(\dfrac{2}{1.923+2}\right)} = 1.933$$

Example 3.34 : *Find out whether the transistor, shown in Fig. 3.76 is in saturation or well with saturation.*

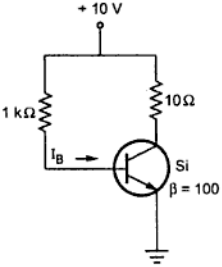


Fig. 3.76

Solution : Applying KVL to base circuit,

We have,

$$10 \text{ V} - 1000 \times I_B - V_{BE} = 0$$

Assuming V_{BE} = 0.7 V we have, $I_B = \dfrac{10-0.7}{1000} = \dfrac{9.3}{1000} = 9.3 \text{ mA}$

$$\therefore \quad I_C = \beta I_B$$

$$= 100 \times 9.3 \text{ mA} = 0.93 \text{ A}$$

We know that,

$$I_{csat} = \frac{V_{CC}}{R_C} = 1 \text{ Amp.}$$

Since $I_{csat} > I_C$

∴ Transistor is not in saturation. For a transistor to be in saturation I_C must be greater or equal to I_{csat}.

Example 3.35 : *Draw the d.c. load line and locate the operating point for the fixed biasing transistor circuit shown in Fig. 5.66. What will be its stability factor?*

Assume $V_{BE} = 0.7$ V.

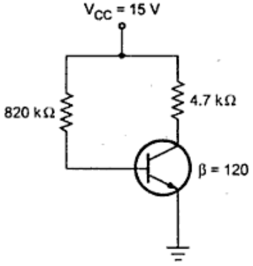


Fig. 3.77

Solution :

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$15 - I_B \times 820\ \text{k}\Omega - 0.7 = 0$$

$$I_B = \frac{14.3}{820\ \text{K}} = 17.4\ \mu\text{A}$$

$$I_C = \beta I_B = 120 \times 17.4\ \mu\text{A}$$

$$= 2.088\ \text{mA}$$

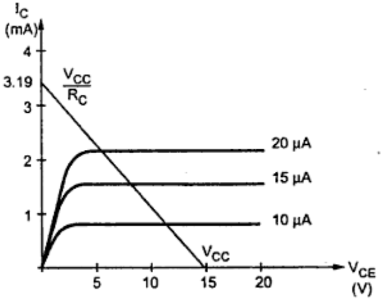


Fig. 3.77 (a)

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 15 - 2.088 \times 10^{-3} \times 4.7 \times 10^{3}$$

$$= 5.186 \text{ V}$$

$$s = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)} = \frac{1+120}{1+120\left(\frac{4.7}{4.7+820}\right)}$$

$$= 55$$

Example 3.36 : *The collector and base current of n-p-n transistor are measured as* $I_C = 5$ *mA,* $I_B = 50$ *µA and* $I_{CBO} = 1$ *µA.*

i) Determine α, β *and* I_E.

ii) Determine the new level of I_B *required to produce* $I_C = 10$ *mA.*

Solution : Here $I_C = 5$ mA, $I_B = 50$ µA, $I_{CBO} = 1$ mA.

i) α, β and $I_E = ?$

As we know that,

$$I_C = \beta I_B + I_{CBO}$$

$$5 \times 10^{-3} = \beta \times 50 \times 10^{-6} + 1 \times 10^{-6}$$

$$\beta = \frac{5 \times 10^{-3}}{51 \times 10^{-6}} = \mathbf{98}$$

$$\alpha = \frac{\beta}{1+\beta} = \frac{98}{99} = \mathbf{0.9898}$$

and

$$I_E = I_C + I_B = 5 \times 10^{-3} + 50 \times 10^{-6}$$

$$\mathbf{I_E = 5.05 \text{ mA}}$$

ii) The new level of I_B can be calculated as

$$I_C = \beta I_B + I_{CBO}$$

$$10 \times 10^{-3} = 98 \times I_B + 1 \times 10^{-6}$$

$$I_B = \frac{10 \times 10^{-3} - 1 \times 10^{-6}}{98}$$

$$I_B = 1.02 \times 10^{-4} \text{ A}$$

$$\mathbf{I_B = 102 \ \mu A}$$

Review Questions

1. *State the advantages of transistor over vacuum tube.*
2. *What is transistor ? Give its circuit symbol.*
3. *Transistor means transfer-resistor, explain this.*
4. *Explain the construction of npn and pnp transistors.*
5. *Why transistor cannot be replaced by back to back diode connection ?*
6. *Why collector region is greater than emitter region ?*
7. *Why depletion layer width at the collector junction is more than the depletion layer width at the emitter junction ?*
8. *Explain the status of unbiased transistor with the help of neat diagram.*
9. *What is the biasing status of two transistor junctions for its various operating regions ?*
10. *Explain the working of npn transistor.*
11. *Explain the working of pnp transistor.*
12. *Explain the various current components of the transistor.*
13. *Mention the different types of transistor configurations. Draw the circuit diagram of each type using NPN transistors. Explain the salient features of each type.*
14. *Distinguish between the different types of transistor configurations with necessary circuit diagrams, using PNP transistor.*
15. *Draw and explain the input and output characteristics of a transistor in CE configuration. Indicate cut-off, saturation and active regions.*
16. *Explain the input and output characteristics of a transistor in CB configuration.*
17. *Obtain the expression for the collector current of a transistor in common emitter configuration.*
18. *Describe a set up to obtain the output characteristics of a transistor in CE configuration. Indicate the various regions of operation on the output characteristics.*
19. *Define :* α_{dc} *and* β_{dc}.
20. *Give the relationship between* α_{dc}, β_{dc} *and prove it.*
21. *What is early effect ?*
22. *What is punch through effect ?*
23. *Compare CB, CE and CC transistor configurations. Which is the widely used configuration ? Why ?*
24. *Define* α_{dc} *and* β_{dc} *of a transistor. For a transistor the base current is 100* μA *and collector current is 2.9 mA. Find* α_{dc} *and* β_{dc}. **(Ans. : $\alpha_{dc} = 0.9666, \beta_{dc} = 29$)**
25. *A transistor has* $\alpha = 0.99$, *what will be the base current if the emitter current is 8 mA ?* **(Ans. : $I_B = 80 \mu A$)**
26. *If the base current in a transistor is 30* μA *when the emitter current is 7.2 mA, what are the values of* α *and* β *? Also calculate the collector current.* **(Ans. : $\alpha = 0.9958, \beta = 239, I_C = 7.17$ mA)**
27. *In a certain transistor, the emitter current is 1.04 times as large as the collector current. If the emitter current is 10 mA, find the base current.* **(Ans. : 384 μA)**

28. *In a certain transistor, 99.5% of the carriers injected into the base cross the collector-base junction. If the leakage current is 6 μA and the collector current is 10 mA, calculate (i) the value of α, (ii) the emitter current.* **(Ans. : $\alpha = 0.995$, $I_E = 10.04$ mA)**
29. *What is leakage current ?*
30. *The reverse leakage current of the transistor, when connected in common-base configuration is 0.2 μA, while it is 18 μA when the same transistor is connected in common-emitter configuration. Calculate the α and β of the transistor.* **(Ans. : $\alpha = 0.988, \beta = 82.33$)**
31. *Give the typical values of α, β.*
32. *What do you mean by transistor biasing ?*
33. *Why biasing is necessary in BJT amplifiers ?*
34. *Draw the output characteristics of a transistor in CE-configuration. Draw the DC load line and indicate the Q-point on it, if the transistor is to be in the (i) Saturation region ii) Active region and iii) Cut-off region.*
35. *What do you understand by Q-point ? What is its significance ?*
36. *What are the factors against which an amplifier needs to be stabilized ?*
37. *Define three stability factors and what is the need of this in BJT circuit ?* **[Nov./Dec.-2004 (Set 1); Dec.-2003 (Set 1); May-2003 (Set 1)]**
38. *Explain different techniques used for biasing transistor amplifiers.*
39. *Which biasing method provides more stabilization amongst the three types of biasing methods ? Why ?*
40. *Explain any one method of biasing a single stage BJT amplifier.*
41. *For the improvement of stability of the operating point what suggestions you make for self bias. Discuss with the help of stability factors.*
42. *What are the requirements of biasing circuits ?*
43. *For a collector to base bias circuit, show that :*

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

44. *Draw the circuit diagram of a collector to base bias circuit of CE amplifier and derive expression for S.* **[May/June-2004 (Set-2)]**
45. *Draw the circuit diagram of a self bias circuit and derive expression for S. Why it is widely used?* **[Nov./Dec.-2004(Set 3); May-2003 (Set 3)]**
46. *Draw the circuit diagram of a self bias BJT circuit and explain how to determine the values of R_1 & R_2.* **[May-2003 (Set 1); Dec.-2003 (Set 1); Nov./Dec.-2004 (Set 1)]**
47. *How to obtain Quiescent point graphically for a given transistor amplifier of CE configuration? Explain.* **[Nov./Dec.-2004 (Set 3); May-2003 (Set 3)]**
48. *How to obtain bias stability in CE configuration circuit?* **[Dec.-2003 (Set 3)]**

49. *For a self bias circuit show that*

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}$$

50. *Draw the circuit diagram of self bias circuit using CE configuration and explain how it stabilizes operating point.*

51. *In the circuit shown in Fig. 3.78, find I_C when V_{CB} = 8 V and V_{CB} when I_C = 2 mA.*

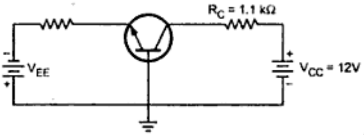


Fig. 3.78

52. *In the circuit shown in the Fig. 3.79 find*

a) V_{CE} when I_C = 1 mA, b) I_C when V_{CE} = 10 V, c) V_{CE} when I_C = 0

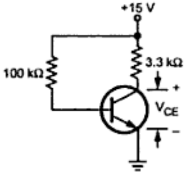


Fig. 3.79

(Ans. : a) V_{CE} = 11.7 V, b) I_C = 1.5 mA, c) V_{CE} = 15 V)

53. ***For the transistor shown in Fig. 3.80 the value of β is 120. Calculate the value of R_B that will just saturate the transistor. Assume $V_{CE\,sat}$ = 0.3 V.***

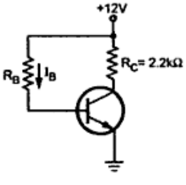


Fig. 3.80

(Ans. : R_B = 255 k Ω)

54. *A silicon transistor with* $\beta = 80$ *is used in self biasing arrangement with* $V_{CC} = 15V$, $R_C = 4.7\ k\Omega$. *The operating point Q is at* $V_{CE} = 8.2\ V$, $I_C = 1.2\ mA$. *Find values of* R_1, R_2 *and* R_E. **(Ans. : $R_1 = 93.8\ k\Omega$, $R_2 = 6.2\ k\Omega$, $R_E = 966.66\ \Omega$)**

55. *The transistor shown in Fig. 3.81 has* $V_{BE\,(active)} = 0.6\ V$ *and* $\beta = 50$. *The operating point* V_{CEQ} *required is 5 V. Calculate i)* R_E *ii) Stability factor* $S = \frac{\partial I_C}{\partial I_{CO}}$. *Assume transformer secondary resistance to be negligible.*

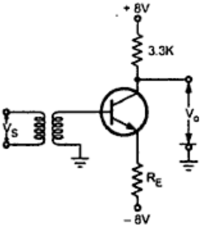


Fig. 3.81 **(Ans. : i) $R_E = 6.65\ k\Omega$, ii) S = 1)**

56. *For the fixed bias circuit* $R_B = 150\ k\Omega$ *and* $R_B = 100\ k\Omega$. *Calculate* I_B, I_C *and* V_{CE} *if* $V_{CC} = 12\ V$, $R_C = 1.1\ k\Omega$ *and* $\beta = 100$ *and also state the region of operation.*

(Ans. : a) For $R_B = 150\ k\Omega$, i) $I_B = 75.33\ \mu A$, ii) $I_C = 7.5\ mA$, iii) $V_{CE} = 3.75\ V$,)
b) For $R_B = 100\ k\Omega$, i) $I_B = 113\ \mu A$, ii) $I_C = 11.3\ mA$, iii) $V_{CE} = 0.43\ V$,
c) Region of operation = Saturation)

57. *Draw the circuit diagram of fixed bias circuit in CE configuration & obtain the expression for* I_B. *Why the circuit is not suitable if the* β *of the transistor is changed.* **[Dec.-2003; (Set-3)]**

58. *In the circuit shown in Fig. 3.82, calculate value of* R_E *so that transistor is just out off saturation.*

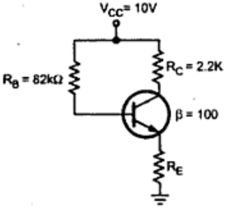


Fig. 3.82 **(Ans. : $R_E = 41.5\ k\Omega$)**

59. *For the circuit shown in Fig. 3.83, determine I_E, V_E and V_{CE}.*

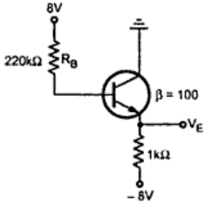

8V
220kΩ
R_B
β = 100
V_E
1kΩ
– 8V

Fig. 3.83

(Ans. : I_E = 4.81 mA, V_E = –3.186, V_{CE} = + 3.186 V)

60. *For the circuit shown in Fig. 3.84, calculate I_E, V_C and V_{CE}.*

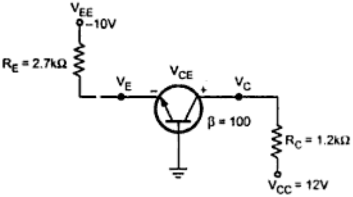

V_{EE}
–10V
R_E = 2.7kΩ
V_E
V_{CE}
–
+
V_C
β = 100
R_C = 1.2kΩ
V_{CC} = 12V

Fig. 3.84

(Ans. : I_E = 3.44 mA, V_C = 5.862 V, V_{CE} = 6.562 V)

61. *In the circuit shown in Fig. 3.85, calculate I_B, I_C, I_E and V_{CE}.*

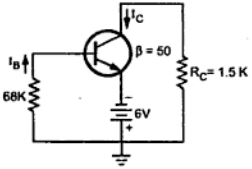

I_C
β = 50
I_B
R_C= 1.5 K
68K
–
6V
+

Fig. 3.85

(Ans. : I_B = 78 μA, I_C = 3.9 mA, I_E = 3.978 mA, $V_{CE\ (w.r.t.\ ground)}$ = – 0.15 V)

62 *For the circuit shown in Fig. 3.86, calculate I_B, I_C and V_{CE}.*

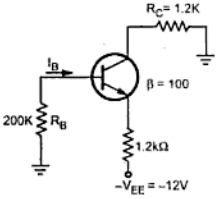


Fig. 3.86

(Ans. : $I_B = 35.18\,\mu A$, $I_C = 3.518$ mA, $V_{CE} = 3.515$ V)

63. *In the voltage divider bias circuit, if V_{CC} = 10 V, V_{CE} = 5 V, I_C = 1.2 mA, R_2 = 10 kΩ, β = 100, and R_E = 270 Ω, calculate R_1 and R_3. Assume $V_{BE(act.)}$ = 0.6 V.* **(Ans. : R_3 = 4045 Ω, R_1 = 130 kΩ)**

64. *For the voltage divider bias if I_{CO} = 1 nA, θ = 2.2×10^8 °C/W, R_C = 1.1 K, β = 100, $V_{CE(act)}$ = 6 V, V_{CC} = 12 V, and R_E = 120 Ω. Calculate the value of stability factor S to make circuit thermally stable.* **(Ans. : S < 5506)**

65. *A self bias circuit has R_E = 1.2 K, R_1 = 120 K, R_2 = 12 K. If V_{CC} and R_C are adjusted to give I_C = 1.2 mA at 20° C, calculate the variation in I_C over temperature range of 20 °C to 100 °C. The transistor used has the parameters given below :*

Parameters	20 °C	100 °C
I_{CO} μA	0.02	1.3
V_{BE} V	0.76	0.56
β	70	150

(Ans. : ΔI_C = 0.2435 mA)

66. *What are the compensation techniques used for V_{BE} & I_{CO}? Explain with the help of suitable circuits.* **[Dec.-2003 (Set 4)]**

67. *A Ge transistor used in self bias circuit has V_{CC} = 16 V, R_C = 1.2 K. The operating point is V_{CE} = 8V and I_C = 2 mA. If h_{FE} = 70, calculate R_1, R_2 and R_E if stability factor $S = \frac{\partial I_C}{\partial I_{CO}} = 10$ is desired.* **(Ans. : R_E = 2760.5 Ω, R_1 = 31.634 kΩ, R_2 = 21.206 kΩ)**

□□□

4

Transistor Amplifier

4.1 Introduction

We have seen that V-I characteristics of an active device such as BJT are non-linear. The analysis of a non-linear device is complex. Thus to simplify the analysis of the BJT, its operation is restricted to the linear V-I characteristics around the Q-point i.e. in the active region. This approximation is possible only with small input signals. The term small signal amplifier refers to the use of signal that takes up a relatively small percentage of an amplifier's operational range. With small input signals the transistor can be replaced with small signal linear model. This model is also called **small signal equivalent circuit.**

We know that the reactance of the capacitance is inversely proportional to the frequency, $Z_C = 1/2\pi f C$. Thus for low frequencies the reactances of junction capacitances of the transistor are very high. Since these junction reactances appear in parallel with junctions, their effect is ignored at low frequencies and transistor analysis is further simplified.

4.2 Graphical Analysis of CE Amplifier

An amplifier is used to increase the signal level ; i.e. the amplifier is used to get a larger signal output from a small signal input. We will assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform, with frequency same as that of the input.

To make the transistor work as an amplifier, it is to be biased to operate in the active region, i.e. base-emitter junction is to be forward biased, while base-collector junction to be reversed biased.

Let us consider the common emitter amplifier circuit using self bias or voltage divider bias as shown in the Fig. 4.1.

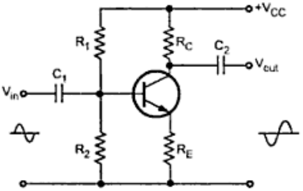


Fig. 4.1 Common emitter amplifier

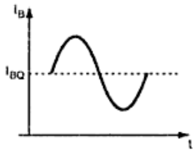
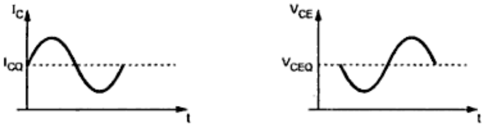


Fig. 4.2 I_{BQ} is quiescent DC base current

In the absence of input signal, only dc voltage are present in the circuit This is known as **zero-signal** or **no-signal** condition or quiescent condition for the amplifier. The dc collector-emitter voltage, V_{CE} , the dc collector current I_C and dc base current I_B is the **quiescent** operating point for the amplifier. On this dc quiescent operating point, we superimpose ac signal by application of ac sinusoidal voltage at the input. Due to this base current varies sinusoidally, as shown in Fig. 4.2.

Since the transistor is biased to operate in the active region, the output is linearly proportional to the input. The output current i.e. the collector current is β times larger than the input base current in common emitter configuration. Hence the collector current will also vary sinusoidally about its quiescent value, I_{CQ}. The output voltage will also vary sinusoidally as shown in the Fig. 4.3 (a) and 4.3 (b).



(a) (b)

Fig. 4.3

Then variations in the collector current and the voltage between collector and emitter due to change in the base current are shown graphically with the help of load line in Fig. 4.3. The collector current varies above and below its Q point value in-phase with the base current, and the collector-to-emitter voltage varies above and below its Q point value 180° out-of-phase with the base voltage, as illustrated in Fig. 4.3 (c).

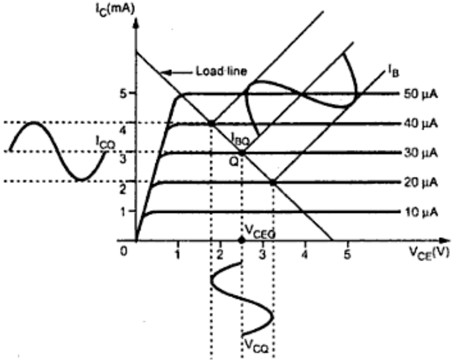


Fig. 4.3 (c) Graphical representation of base current, collector current, and collector-emitter voltage swings

When one cycle of input is completed, one cycle of output will also be completed. This means the frequency of output sinusoidal is the same as the frequency of input sinusoid. Thus in the amplification process, frequency of the output signal does not change, only the magnitude of the output is larger than that of the input.

Common Emitter Amplifier Circuit

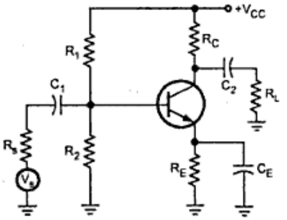


Fig. 4.4 Practical common emitter amplifier circuit

Fig. 4.4 shows the practical circuit of common emitter transistor amplifier. It consists of different circuit component. The functions of these components are as follows :

1. Biasing Circuit

The resistances R_1, R_2 and R_E forms the voltage divider biasing circuit for the CE amplifier. It sets the proper operating point for the CE amplifier.

2. Input Capacitor C_1

This capacitor couples the signal to the base of the transistor. It blocks any dc component present in the signal and passes only ac signal for amplification. Because of this biasing conditions are maintained constant.

3. Emitter Bypass Capacitor C_E

An emitter bypass capacitor C_E is connected in parallel with the emitter resistance, R_E to provide a low reactance path to the amplified ac signal. If it is not inserted, the amplified ac signal passing through R_E will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

4. Output Coupling Capacitor C_2

The coupling capacitor C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks dc and passes only ac part of the amplified signal.

Need for C_1, C_2 and C_E

We know that, the impedance of capacitor is given as

$$X_C = \frac{1}{2\pi fC}$$

Thus, at signal frequencies all the capacitors have extremely small impedance and it can be treated as an ac short circuit. For bias/dc conditions of the transistor all the capacitors act as a dc open circuit. With this knowledge we will see the importance of C_1, C_2 and C_E.

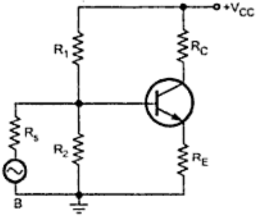


Fig. 4.5

Consider that the signal source is connected directly to the base of the transistor as shown in Fig. 4.5.

Looking at the Fig. 4.5 we can immediately notice that source resistance R_s is in parallel with R_2. This will reduce the bias voltage at the transistor base and, consequently alter the collector current, which is not desired. Similarly, by connecting R_L directly, the dc levels of V_C and V_{CE} will change. To avoid this and maintain the stability of bias condition coupling capacitors are connected. As mentioned earlier, coupling capacitors act as open circuits to dc, maintain stable biasing conditions even after connection of R_s and R_L. Another advantage of connecting C_1 is that any dc component in the signal is opposed and only ac signal is routed to the transistor amplifier.

The emitter resistance R_E is one of the component which provides bias stabilization. But it also reduces the voltage swing at the output. The emitter bypass capacitor C_E provides a low reactance path to the amplified a.c. signal increasing the output voltage swing.

For the proper operation of the circuit, polarities of the capacitors must be connected correctly. The curve bar which indicates negative terminal must always be connected at a dc voltage level lower than (or equal to) the dc level of the positive terminal (straight bar). For example, C_1 in Fig. 4.4 has its negative terminal at dc ground level, because it is grounded through the signal source resistance R_s. The positive terminal of C_1 is at + V_B with respect to ground.

Phase Reversal

The phase relationship between the input and output voltages can be determined by considering the effect of a positive half cycle and negative half cycle separately. Consider the positive half cycle of input signal in which terminal A is positive w.r.t. B. Due to this, two voltages, ac and dc will be adding each other, increasing forward bias on base emitter junction. This increases base current. The collector current is β times the base current, hence the collector current will also increase. This increases the voltage drop across R_C. Since $V_C = V_{CC} - I_C R_C$, the increase in I_C results in a drop in collector voltage V_C, as V_{CC} is constant. Thus, as V_i increases in a positive direction, V_o goes in a negative direction and we get negative half cycle of output voltage for positive half cycle at the input.

In the negative half cycle of input, in which terminal A becomes negative w.r.t. terminal B, the ac and dc voltages will oppose each other, reducing forward bias on base-emitter p-n junction. This reduces base current. Accordingly collector current and drop across R_C both reduce, increasing the output voltage. Thus, we get positive half cycle at the output for negative half cycle at the input. Therefore, we can say that there is a phase shift of 180° between input and output voltages for a common emitter amplifier.

4.3 H-Parameter Model

Let us consider transistor amplifier as a black box as shown in the Fig. 4.6.

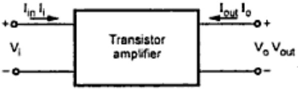


Fig. 4.6 Transistor amplifier

Here, I_i : is the input current to the amplifier

V_i : is the input voltage to the amplifier

I_o : is the output current of the amplifier and

V_o : is the output voltage of the amplifier

As we know transistor is a current operated device, input current is an independent variable. The input current, I_i and output voltage V_o devices the input voltage V_i as well as the output current I_o. Hence input voltage V_i and output current I_o are the dependent variables, whereas input current I_i and output voltage V_o are independent variables. Thus we can write

$$V_i = f_1 (I_i , V_o) \quad \text{... (1)}$$

$$I_o = f_2 (I_i , V_o) \quad \text{... (2)}$$

This can be written in the equation form as follows

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{... (3)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{... (4)}$$

The above equations can also be written using alphabetic notations,

$$V_i = h_i . I_i + h_r . V_o \quad \text{... (5)}$$

$$I_o = h_f . I_i + h_o . V_o \quad \text{... (6)}$$

Definitions of h-parameter

The parameters in the above equation are defined as follows :

$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$ = Input resistance with output short-circuited, in ohms.

$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}$ = Fraction of output voltage at input with input open circuited.

This parameter is ratio of similar quantities, hence unitless

$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$ = Forward current transfer ratio or current gain with output short circuited.

This parameter is a ratio of similar quantities, hence unitless.

$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}$ = Output admittance with input open-circuited, in mhos.

From the above discussion we can say that, these four parameters are not same. They have different units. In other words, they are mixture of different units and hence referred to as **hybrid parameters.** As we use small letter for ac analysis, these are commonly known as **h-parameters.** The standard notations can be given as

i = 11 = input

o = 22 = output

f = 21 = forward transfer

r = 12 = reverse transfer

Thus we can write h-parameters as follows.

a) With output short circuited :

$h_{11} = h_i$: Input resistance

$h_{21} = h_f$: Short circuit current gain

b) With input open circuited :

$h_{12} = h_r$: Reverse voltage transfer ratio

$h_{22} = h_o$: Output admittance

H-parameter equivalent circuit for transistor

In order to analyze transistorized amplifier circuit and calculate its input impedance, output impedance, current gain and voltage gain, it is necessary to replace transistor circuit with its equivalent. The equivalent circuit can be drawn with the help of two equations, as shown in Fig. 4.7.

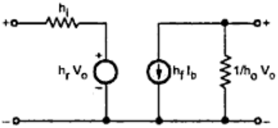


Fig. 4.7 Hybrid model or equivalent circuit for transistor

$$V_i = h_i I_i + h_r V_o \qquad I_o = h_f I_i + h_o V_o$$

Many transistor models have been proposed, each one having its advantages and disadvantages. The transistor model used in this text is in terms of h-parameters.

Benefits of h-parameters

1. Real numbers at audio frequencies.
2. Easy to measure.
3. Can be obtained from the transistor static characteristic curves.
4. Convenient to use in circuit analysis and design.
5. Most of the transistor manufacturers specify the h-parameters.

H-parameter equivalent circuit for CE configuration

To see how we can derive a hybrid model for a transistor, let us consider the common emitter configuration shown in Fig. 4.8. The variables I_b, I_c, V_b and V_c represent total instantaneous currents and voltages.

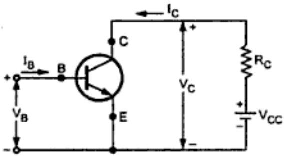


Fig. 4.8 Simple common emitter configuration

I_b = input current

I_c = output current

V_{be} = input voltage

V_{ce} = output voltage

Fig. 4.9 shows the h-parameter equivalent circuit for the common emitter configuration.

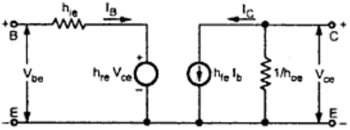


Fig. 4.9 h-parameter equivalent circuit for the common emitter configuration

From the h-parameter equivalent circuit of the common emitter configuration we can write,

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \qquad \dots (7)$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \qquad \dots (8)$$

where

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} \text{ constant}} \qquad \dots (9)$$

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B \text{ constant}} \qquad \dots (10)$$

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} \text{ constant}} \qquad \dots (11)$$

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_C}\right|_{I_B \text{ constant}} \qquad \dots (12)$$

The quantities ΔV_{BE} (V_{be}), ΔV_{CE} (V_{ce}), ΔI_B (I_b) and ΔI_C (I_c) represent the small change in base and collector voltages and currents.

H-parameters for all three configurations

As mentioned earlier, transistor can be represented as a two port network by making any one terminal common between input and output. Since there are three possible configurations in which a transistor can be used, there is a change in terminal voltage and current for different transistor configurations. For different configurations the relation between input parameters and output parameters also differs. Therefore, one needs to define different set of h-parameters for different configurations. To designate the type of configuration another subscript is added to the h-parameters.

For example :

$h_{ie} = h_{11e}$ = input resistance in common emitter configuration.

$h_{fb} = h_{21b}$ = short-circuit current gain in common base configuration.

The Table 4.1 summarizes the h-parameters for all the three configurations.

Parameter	CB	CE	CC
Input resistance	h_{ib}	h_{ie}	h_{ic}
Reverse voltage gain	h_{rb}	h_{re}	h_{rc}
Forward transfer current gain	h_{fb}	h_{fe}	h_{fc}
Output admittance	h_{ob}	h_{oe}	h_{oc}

Table 4.1

The basic circuit of hybrid model is same for all the three configurations, only parameters are different. The Fig. 4.10 shows the transistor configurations and their hybrid models.

The circuits and equations in Fig. 4.10 are valid for either an n-p-n or p-n-p transistor and are independent of the type of load or method of biasing.

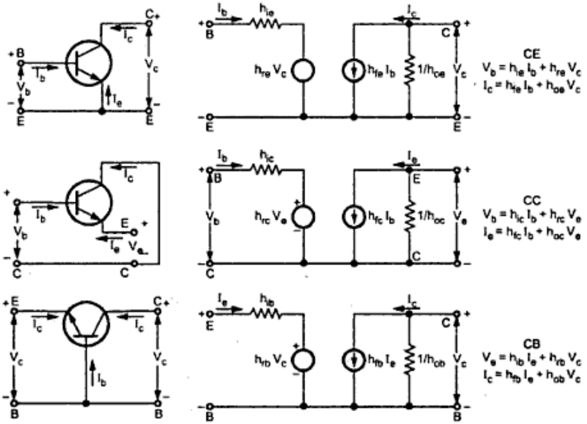

CE
$V_b = h_{ie} I_b + h_{re} V_c$
$I_c = h_{fe} I_b + h_{oe} V_c$
CC
$V_b = h_{ic} I_b + h_{rc} V_e$
$I_e = h_{fc} I_b + h_{oc} V_e$
CB
$V_e = h_{ib} I_e + h_{rb} V_c$
$I_c = h_{fb} I_e + h_{ob} V_c$
B
C
E
I_b
I_c
I_e
V_b
V_c
V_e
h_{ie}
h_{ic}
h_{ib}
$h_{re} V_c$
$h_{rc} V_e$
$h_{rb} V_c$
$h_{fe} I_b$
$h_{fc} I_b$
$h_{fb} I_e$
$1/h_{oe}$
$1/h_{oc}$
$1/h_{ob}$

Fig. 4.10 Transistor configurations and their hybrid models

4.4 Analysis of Single Stage Transistor Amplifier using h-Parameters

The Fig. 4.11 shows basic amplifier circuit. From the Fig. 4.11 we can notice that to form a transistor amplifier only it is necessary to connect an external load and signal source, along with proper biasing. Fig. 4.11 represents a transistor in any one of the three possible configurations.

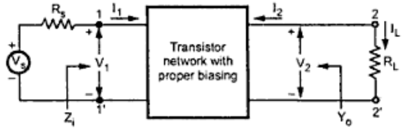


Fig. 4.11 Basic transistor amplifier

We can replace transistor circuit shown in Fig. 4.11 with its small signal hybrid model as shown in Fig. 4.12.

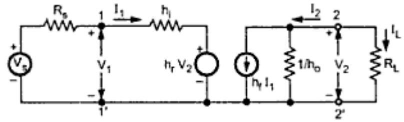


Fig. 4.12 Transistor amplifier in its h-parameter model

Let us analyze hybrid model to find the current gain, the input resistance, the voltage gain, and the output resistance.

Current Gain (A_i) :

For transistor amplifier A_i is defined as the ratio of output to input currents. It is given by,

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1} \qquad \text{... (1)}$$

Here I_L and I_2 are equal in magnitude but opposite in sign, i.e. $I_L = -I_2$

From the circuit of Fig. 4.12 We have,

$$I_2 = h_f I_1 + h_o V_2 \qquad \text{... (2)}$$

Substituting $V_2 = -I_2 R_L$ in the equation we obtain

$$I_2 = h_f I_1 + h_o(-I_2 R_L)$$

$$\therefore \quad I_2 + h_o I_2 R_L = h_f I_1$$

$$\therefore \quad (1 + h_o R_L) I_2 = h_f I_1$$

$$\therefore \qquad \frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

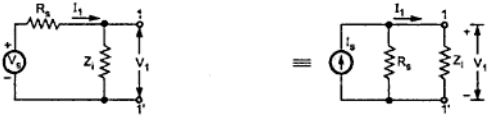
$$\therefore \qquad \boxed{A_i = -\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o R_L}} \qquad \text{... (3)}$$

Current Gain (A_{Is}) :

It is the current gain taking into account the source resistance, R_S if the model is driven by the current source instead of voltage source. It is given by

$$A_{is} = -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \cdot \frac{I_1}{I_s} \qquad \text{... (4)}$$

$$= A_i \cdot \frac{I_1}{I_s}$$



(a) Input section of hybrid model **(b) Input section of hybrid model with current source instead of voltage source**

Fig. 4.13

Looking at Fig. 4.13 (b) and using current divider equation we get

$$I_1 = \frac{I_s R_s}{Z_i + R_s}$$

$$\therefore \qquad \frac{I_1}{I_s} = \frac{R_s}{Z_i + R_s}$$

and hence $$A_{is} = \frac{A_i R_s}{Z_i + R_s} \qquad \text{... (5)}$$

Input Impedance (Z_i)

As shown in the Fig. 4.11, R_i is the input resistance looking into the amplifier input terminals (1, 1′). It is given by,

$$R_i = \frac{V_1}{I_1} \qquad \text{... (6)}$$

From the input circuit of Fig. 4.12, we have

$$V_1 = h_i I_1 + h_r V_2 \qquad \text{... (7)}$$

Hence $$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$\therefore \quad Z_i = h_i + h_r \frac{V_2}{I_1} \qquad \text{... (8)}$$

Substituting $$V_2 = -I_2 R_L = A_i I_1 R_L \qquad \text{... (9)}$$

In the above equation we get,

$$Z_i = h_i + \frac{h_r A_i I_1 R_L}{I_1} = h_i + h_r A_i R_L \qquad \text{... (10)}$$

Substituting $$A_i = -\frac{h_f}{1 + h_o R_L}$$

We get, $$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L} \qquad \text{... (11)}$$

Dividing numerator and denominator by R_L we get

$$Z_i = h_i - \frac{h_r h_f}{1/R_L + h_o}$$

$$\therefore \quad \boxed{Z_i = h_i - \frac{h_r h_f}{Y_L + h_o}} \quad \text{where } Y_L = \frac{1}{R_L} \qquad \text{... (12)}$$

From this equation we can note that input impedance is a function of the load impedance.

Voltage Gain (A_v) :

It is the ratio of output voltage V_2 to the input voltage V_1. It is given by

$$A_v = \frac{V_2}{V_1} \qquad \text{... (13)}$$

From equation (9) we have,

$$\boxed{A_v = \frac{A_i I_1 R_L}{V_1} = \frac{A_i R_L}{Z_i}} \qquad \text{... (14)}$$

Since, $$\frac{I_1}{V_1} = \frac{1}{Z_i}$$

Voltage Gain (A_{vs}) : It is voltage gain including the source. It is given by,

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \times \frac{V_1}{V_s} \qquad \text{... (15)}$$

$$\therefore \quad A_{vs} = A_v \times \frac{V_1}{V_s} \qquad \text{... (16)}$$

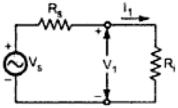


Fig. 4.14

Looking at Fig. 4.14 and applying potential divider theorem we can write,

$$V_1 = \frac{Z_i}{R_s + Z_i} V_s$$

$$\therefore \quad \frac{V_1}{V_s} = \frac{Z_i}{R_s + Z_i}$$

Substituting value of $\frac{V_1}{V_s}$ in equation (16) We get,

$$\therefore \quad \boxed{A_{vs} = A_v \cdot \frac{Z_i}{R_s + Z_i}} \qquad \text{... (17)}$$

$$= \frac{A_i R_L}{R_s + R_i} \quad \because A_v = \frac{A_i R_L}{Z_i} \qquad \text{... (18)}$$

Output Admittance Y_o :

It is the ratio of output current I_2 to the output voltage V_2. It is given by,

$$Y_o = \frac{I_2}{V_2} \text{ with } V_s = 0 \qquad \text{... (19)}$$

From equation (2), we have, $I_2 = h_f I_1 + h_o V_2$

Dividing above equation by V_2 we get,

$$\frac{I_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

$$\therefore \quad Y_o = h_f \frac{I_1}{V_2} + h_o \qquad \text{... (20)}$$

From Fig. 4.12, with $V_s = 0$ we can write,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \qquad \text{... (21)}$$

$$\therefore \quad (R_s + h_i) I_1 = -h_r V_2$$

$$\therefore \quad \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \qquad \text{... (22)}$$

Substituting value of $\frac{I_1}{V_2}$ from equation (22) in equation (20), we obtain,

$$\therefore \quad \boxed{Y_o = h_o - \frac{h_f h_r}{h_i + R_s}} \qquad \text{... (23)}$$

From this equation we can note that output admittance is a function of the source resistance.

Power Gain (A_P) : It is the ratio of average power delivered to the load R_L, to the input power. Output power is given as

$$P_2 = V_2 \; I_L = -V_2 I_2 \qquad \text{... (24)}$$

Since the input power is $P_i = V_1 I_1$ the operating power gain A_P of the transistor is defined as

$$\therefore \quad \boxed{A_P = \frac{P_2}{P_1} = -\frac{V_2 I_2}{V_1 I_1} = A_v \, A_i = A_i^2 \frac{R_L}{Z_i}} \quad \because A_v = \frac{A_i \, R_L}{Z_i} \qquad \text{... (25)}$$

Relation Between A_{VS} and A_{IS} :

From equations (18) and equation (5) we have

$$A_{vs} = \frac{A_i \, R_L}{Z_i + R_s}$$

and $$A_{is} = \frac{A_i \, R_s}{Z_i + R_s}$$

Taking ratio of above two equations we get,

$$\frac{A_{vs}}{A_{is}} = \frac{R_L}{R_s}$$

$$\therefore \quad \boxed{A_{vs} = A_{is} \cdot \frac{R_L}{R_s}} \qquad \text{... (26)}$$

Table 4.2 summarizes small-signal analysis of a transistor amplifier

$A_i = -\frac{h_f}{1+h_o R_L}$
$A_{is} = \frac{A_i R_s}{Z_i + R_s}$
$Z_i = h_i + h_r A_i R_L = h_i - \frac{h_f h_r}{h_o + Y_L}$
$A_v = \frac{A_i R_L}{Z_i}$
$A_{vs} = \frac{A_v R_i}{Z_i + R_s} = \frac{A_i R_L}{Z_i + R_s} = \frac{A_{is} R_L}{R_s}$
$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} = \frac{1}{Z_o}$
$A_P = A_v A_i = A_i^2 \frac{R_L}{Z_i}$

Table 4.2

Key Point : *The above formulae is applicable to all transistor configuration. Only we have added the appropriate subscript to h-parameters corresponding to the transistor configuration in the expression of* A_i, A_v, Z_i *and* Y_o.

Table 4.3 shows the typical values of h parameters for three different configurations at normal room temperature and at quiescent operating point I_{EQ} = 7.3 mA

Parameter	CE	CC	CB
$h_{11} = h_i$	1100 Ω	1100 Ω	21.6 Ω
$h_{12} = h_r$	2.5×10^{-4}	− 1	29×10^{-4}
$h_{21} = h_f$	50	− 51	− 0.98
$h_{22} = h_o$	25 μA/V	25 μA/V	0.49 μA/V

Table 4.3

4.5 Guidelines for Analysis of a Transistor Circuit

In the previous section we have seen generalized transistor circuit analysis using h-parameters. There are many transistor circuits. Circuits may consist of different biasing techniques, different configurations and so on. The analysis of such transistor circuits for its small signal behaviour can be made by following simple guidelines. These guidelines are :

1. Draw the actual circuit diagram.
2. Replace coupling capacitors and emitter bypass capacitor by short circuit.
3. Replace dc source by a short circuit. In other words, short V_{CC} and ground lines.
4. Mark the points B(base), C(collector), E(emitter) on the circuit diagram and locate these points as the start of the equivalent circuit.
5. Replace the transistor by its h-parameter model.

Following example explains us how to use guidelines for the analysis of a transistor circuit.

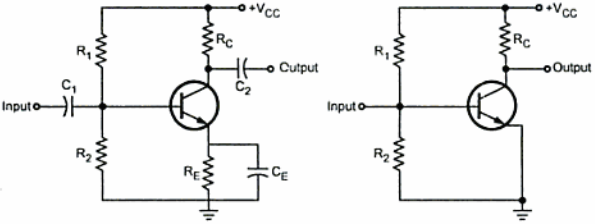
Consider a common emitter amplifier with voltage divider bias circuit as shown in the Fig. 4.15 (a)

Guideline 1 : Draw actual circuit diagram (See Fig. 4.15 (a) and (b) on next page)

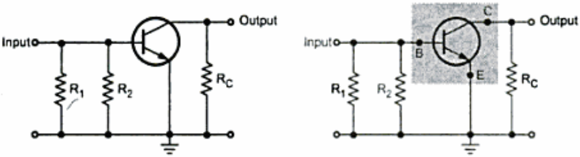
Guideline 2 : Short coupling and bypass capacitors

Guideline 3 : Short V_{CC} and ground lines

Guideline 4 : Mark points B, C, E and locate these points as the start of the equivalent circuit


+V_CC
R_1
R_C
Output
C_1
C_2
Input
R_2
R_E
C_E
+V_CC
R_1
R_C
Output
Input
R_2

(a) Actual circuit diagram **(b) Circuit with capacitors as a short circuit**


Output
Input
R_1
R_2
R_C
C
Output
Input
B
E
R_1
R_2
R_C

(c) Circuit with V_{CC} and ground short circuit **(d) Circuit with B, C and E points located**

Fig. 4.15

Guideline 5 : Replace transistor by its h-parameter model

and calculate effective R_i (R'_i) and effective R_o (R'_o).

For example, in above circuit $R'_i = R_1 \parallel R_2 \parallel R_i$

and $R'_o = R_o \parallel R_C$.

With these guidelines we will analyze CE,CB and CC amplifier circuits in coming sections.

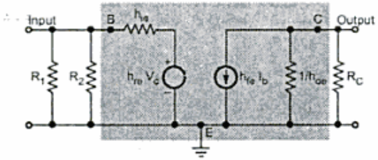

Input
B
h_ie
C
Output
R_1
R_2
h_re V_c
h_fe I_b
1/h_oe
R_C
E

Fig. 4.15 (e) Circuit with transistor replaced by h-parameter equivalent

➡ **Example 4.1 :** *Consider a single stage CE amplifier with $R_s = 1\ k\Omega$, $R_1 = 50\ K$, $R_2 = 2\ K$, $R_C = 1\ K$, $R_L = 1.2\ K$, $h_{fe} = 50$, $h_{ie} = 1.1\ K$, $h_{oe} = 25\ \mu A/V$ and $h_{re} = 2.5 \times 10^{-4}$, as shown in Fig. 4.16.*

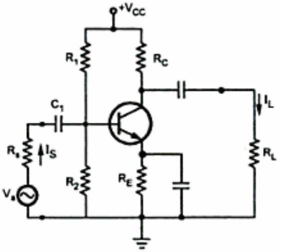

+V_CC
R₁
R_C
C₁
I_L
R_s
I_S
R_L
R₂
R_E
V_s

Fig. 4.16

Find A_i, R_i, A_v, $A_i = \dfrac{I_L}{I_s}$, $A_{vs} = \dfrac{V_o}{V_s}$ *and* R_o.

Solution :

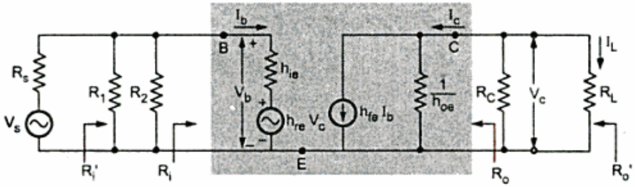

I_b
I_c
B
C
+
h_ie
V_b
+
–
h_re V_c
h_fe I_b
1/h_oe
R_C
V_c
R_L
I_L
R_s
V_s
R₁
R₂
R_i'
R_i
E
R_o
R_o'

Fig. 4.17

a) Current gain $A_i = \dfrac{-I_c}{I_b} = \dfrac{-h_{fe}}{1+h_{oe}R'_L}$

where $R'_L = R_C \parallel R_L = 1\text{ K} \parallel 1.2\text{ K} = \mathbf{545.45\ \Omega}$

$\therefore$ $A_i = \dfrac{-50}{1+25\mu\text{ A / V}(545.45)} = \mathbf{-49.32}$

b) Input resistance $R_i = h_{ie} + h_{re}\, A_i\, R'_L$

$= 1.1\text{ K} + 2.5\times10^{-4} \times(-49.32)\times545.45$

$= \mathbf{1093\ \Omega}$

c) Voltage gain $A_v = \dfrac{V_c}{V_b} = \dfrac{A_i\, R'_L}{R_i} = \dfrac{-49.32\times545.45}{1093} = \mathbf{-24.61}$

d) Overall input resistance $R'_i = R_i \parallel R_1 \parallel R_2 = 1093 \parallel 50\text{ K} \parallel 2\text{ K} = \mathbf{696.9\ \Omega}$

e) Overall voltage gain $A_{vs} = \frac{V_c}{V_s} = \frac{V_c}{V_b} \times \frac{V_b}{V_s}$

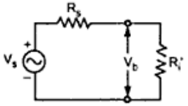


Fig. 4.18

Looking at Fig. 4.18 and voltage divider equation we get,

$$V_b = \frac{V_s\,R_i'}{R_s + R_i'} \qquad \therefore \qquad \frac{V_b}{V_s} = \frac{R_i'}{R_s + R_i'}$$

$$\therefore\ A_{vs} = \frac{V_c}{V_b} \times \frac{V_b}{V_s} = A_v \times \frac{R_i'}{R_s + R_i'}$$

$$= 24.61 \times \frac{696.9}{1\,K + 696.9} = \mathbf{10.1}$$

f) $A_{i(\text{for circuit})} = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$

Looking at Fig. 4.19 and 4.20 and using current divider equation we have,

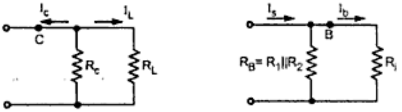


Fig. 4.19 and 4.20

$$I_L = \frac{-I_c R_C}{R_C + R_L}$$

$$\therefore \qquad \frac{I_L}{I_c} = \frac{-R_C}{R_C + R_L}$$

and $$I_b = \frac{I_s R_B}{R_B + R_i}$$

where $R_B = R_1 \parallel R_2 = 50\ K \parallel 2\ K = 1.923\ K$

$$\therefore \qquad \frac{I_b}{I_s} = \frac{R_B}{R_B + R_i}$$

$$\therefore\ A_{i\,(\text{for circuit})} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s} = \frac{-R_C}{R_C + R_L} \times 49.32 \times \frac{R_B}{R_B + R_i}$$

$$= \frac{-1\,K}{1K + 1.2\,K} \times 49.32 \times \frac{1.923\,K}{1.923\,K + 1.093\,K} = \mathbf{-\ 14.29}$$

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s'}$$

where $R_s' = R_s \parallel R_1 \parallel R_2$
$= 1\,K \parallel 50\,K \parallel 2\,K$

$$= 25\times10^{-6} - \frac{50\times2.5\times10^{-4}}{1.1\times10^{3}+657.9} = 1.7889\times10^{-5}$$

$$R_o = Z_o = \frac{1}{Y_o} = 55.899\ k\Omega$$

$$R'_o = R_o \| R'_L$$

$$= 55.899\ k\Omega \| 545.45$$

$$= 540\ \Omega$$

Example 4.2 : *In the common collector in Fig. 4.21, the transistor parameters are* $h_{ic} = 1.2K$, $h_{fc} = -101$, $h_{rc} = 1$ *and* $h_{oc} = 25\ \mu A / V$. *Calculate the* R_i, $A_i = \frac{I_L}{I_s}$, A_v, $A_{vs} = \frac{V_o}{V_s}$, R_o *for the circuit.*

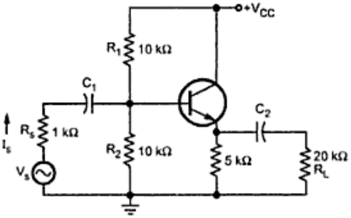

+V_CC
R_1 10 kΩ
C_1
C_2
R_s 1 kΩ
I_s
R_2 10 kΩ
V_s
5 kΩ
20 kΩ R_L

Fig. 4.21

Solution : Fig. 4.22 shows the h-parameters equivalent model for the given circuit.

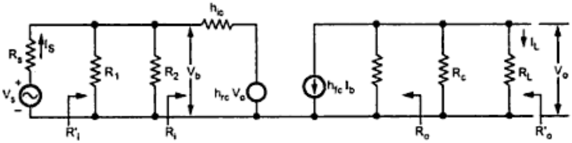

h_ic
R_s
I_s
+
V_s
−
R_1
R_2
V_b
h_rc V_o
h_fc I_b
R_e
R_L
I_L
V_o
R'_i
R_i
R_o
R'_o

Fig. 4.22 h-parameter equivalent model

a) Current Gain $$(A_i) = -\frac{I_e}{I_b} = \frac{-hf_c}{1+h_{oc}R'_L} \text{ where } R'_L = R_E \| R_L$$

$$= \frac{-(-101)}{1+25\times10^{-6}(5\ K\|20\ K)} = \mathbf{91.81}$$

b) Input Resistance $(R_i) = h_{ic} + h_{rc} A_i R'_L$

$= 1.2\text{ K} + 1 \times 91.81 \times (5\text{ K} \parallel 20\text{ K}) = \mathbf{368.44\text{ K}}$

c) Overall Input Resistance $R'_i = R_i \parallel R_1 \parallel R_2 = 368.44\text{ K} \parallel 10\text{ K} \parallel 10\text{ K}$

$= \mathbf{4.933\text{ K}}$

d) Voltage Gain $$(A_v) = \frac{A_i R'_L}{R_i} = \frac{91.81 \times (5\text{ K} \parallel 20\text{ K})}{368.44\text{ K}} = \mathbf{0.996}$$

e) Overall voltage Gain $$(A_{vs}) = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s}$$

where $\frac{V_o}{V_b} = A_v$ and $\frac{V_o}{V_s} = \frac{R'_i}{R'_i + R_s}$

$$\therefore \quad A_{vs} = A_v \cdot \frac{R'_i}{R'_i + R_s} = 0.996 \times \frac{4.933\text{ K}}{4.933\text{ K} + 1\text{K}} = \mathbf{0.828}$$

f) Overall Current Gain $$(A_{is}) = \frac{I_L}{I_s} = \frac{I_L}{I_e} \times \frac{I_e}{I_b} \times \frac{I_b}{I_s}$$

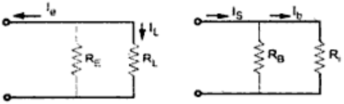


Fig.4.23 & 4.24

where $$\frac{I_L}{I_e} = \frac{-R_E}{R_E + R_L}$$

$$= \frac{-5\text{ K}}{5\text{ K} + 20\text{ K}} = -0.2$$

$$\frac{I_e}{I_b} = -A_i = -91.81$$

$$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(101110)}{(101110) + 368.44} = 0.0134$$

$$\therefore \quad A_{i(\text{for circuit})} = \frac{I_L}{I_s} = (-0.2) \times (-91.81) \times (0.0134) = \mathbf{0.246}$$

g) Output Resistance $$R_o = \frac{1}{h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R'_s}}$$ where $R'_s = R_s \parallel R_1 \parallel R_2 = \mathbf{833.33\ \Omega}$

$$\therefore \quad R_o = \frac{1}{25 \times 10^{-6} - \left(\frac{-101 \times 1}{1.2\text{ K} + 833.33}\right)} = \mathbf{20.12\ \Omega}$$

$$R'_o = R_o \parallel R'_L = 20.12 \parallel (5\text{ K} \parallel 20\text{ K}) = \mathbf{20\ \Omega}$$

From Table 4.2 we can write the generalized formulae for common emitter, common collector and common base configurations. However, in most of the times h-parameters are specified for common emitter configuration, therefore, for analysis of common collector and common base configurations we have to first convert given h-parameters for common emitter configuration into the desired configuration by using conversion formulae given in Table 4.4.

Symbol	Common emitter	Common collector	Common base	T equivalent circuit
h_{ie}	1,100 Ω	h_{ic} *	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{re}	2.5×10^{-4}	$1 - h_{rc}$ *	$\frac{h_{ib}\,h_{ob}}{1+h_{fb}} - h_{rb}$	$\frac{r_b}{(1-a)\,r_c}$
h_{fe}	50	$-(1+h_{fc})$ *	$-\frac{h_{fb}}{1+h_{fb}}$	$\frac{a}{1-a}$
h_{oe}	25 µA/V	h_{oc} *	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a)\,r_c}$
h_{ib}	$\frac{h_{ie}}{1+h_{fe}}$	$-\frac{h_{ic}}{h_{fc}}$	21.6 Ω	$r_e + (1-a)\,r_b$
h_{rb}	$\frac{h_{ie}\,h_{oe}}{1+h_{fe}} - h_{re}$	$h_{fc} - \frac{h_{ic}\,h_{oc}}{h_{fc}} - 1$	2.9×10^{-4}	$\frac{r_b}{r_c}$
h_{fb}	$-\frac{h_{fe}}{1+h_{fe}}$	$-\frac{1+h_{fc}}{h_{fc}}$	-0.98	$-a$
h_{ob}	$\frac{h_{oe}}{1+h_{fe}}$	$-\frac{h_{oc}}{h_{fc}}$	0.49 µA/V	$\frac{1}{r_c}$
h_{ic}	h_{ie} *	1,100 Ω	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{rc}	$1 - h_{re} \approx 1$ *	1	1	$1 - \frac{r_e}{(1-a)\,r_c}$
h_{fc}	$-(1+h_{fe})$ *	-51	$-\frac{1}{1+h_{fb}}$	$-\frac{1}{1-a}$
h_{oc}	h_{oe} *	25 µA/V	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a)\,r_c}$
a	$\frac{h_{fe}}{1+h_{fe}}$	$\frac{1+h_{fc}}{h_{fc}}$	$-h_{fb}$	0.980
r_c	$\frac{1+h_{fe}}{h_{oe}}$ *	$-\frac{h_{fc}}{h_{oc}}$ *	$\frac{1}{h_{ob}}$	2.04 M
r_e	$\frac{h_{re}}{h_{oe}}$ *	$\frac{1-h_{rc}}{h_{oc}}$ *	$h_{ib} + \frac{h_{rb}}{h_{ob}}(1+h_{fb})$ *	10 Ω
r_b	$h_{ie} + \frac{h_{re}}{h_{oe}}(1+h_{fe})$ *	$h_{ic} + \frac{h_{fc}}{h_{oc}}(1+h_{rc})$ *	$\frac{h_{rb}}{h_{ob}}$ *	590 Ω

Table 4.4 h-parameter conversion table

* Exact.

4.6 Analysis of Transistor Amplifier using Simplified Hybrid-Model

So far we have seen the exact calculations of current gain, voltage gain, input and output impedances of transistor amplifier circuits. In most practical cases it is appropriate to obtain approximate values of current gain, voltage gain, input and output impedances rather than to carry out more lengthy exact calculations. We can justify this statement with the fact that h-parameter themselves usually vary widely for the same type of transistor. But now the question is when to use approximate analysis ? To solve this question there is a generalized rule. This rule says that if $h_{oe} \cdot R_L < 0.1$ then we can proceed for approximate analysis; otherwise do the exact analysis. In this section we see how to analyze transistor with approximate model.

4.6.1 Analysis of Common Emitter Circuit using Simplified Hybrid Model

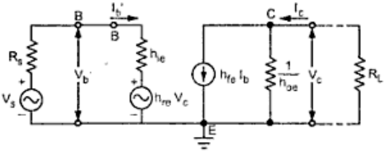


Fig. 4.25

Let us consider the h-parameter equivalent circuit for the amplifier, as shown in the Fig. 4.25.

Now, see how can we modify this model so as to make the analysis simple without greatly sacrificing accuracy ?

Since $1/h_{oe}$ is in parallel with R_L and R_C if $1/h_{oe} >> R_L \parallel R_C$, then h_{oe} may be neglected. If we neglect h_{oe}, the collector current I_c is given by $I_c = h_{fe} I_b$. Under these conditions the magnitude of the voltage of the generator in the emitter circuit is,

$$h_{re}\,|V_{ce}| = h_{re}\,I_c\,(R_L \parallel R_C) = h_{re} h_{fe}\,I_b\,(R_L \parallel R_C)$$

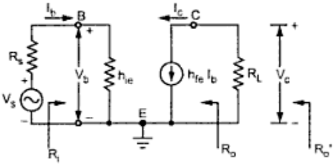


Fig. 4.26 Approximate CE model

Since $h_{re} h_{fe} \approx 0.01$, this voltage may be neglected in comparison with the $h_{ie} I_b$ drop across h_{ie}, provided that $R_L \parallel R_C$ is not too large. We therefore conclude that if the load resistance $R_L \parallel R_C$ is small, it is possible to neglect the parameters h_{re} and h_{oe} in the h-parameter equivalent circuit. Fig. 4.26 shows the approximate h-parameter equivalent circuit.

Current Gain : From Table 4.2 the CE current gain is given as

$$\boxed{A_i = \frac{-I_c}{I_b} = \frac{-h_{fe}}{1 + h_{oe} R_L}}$$

By neglecting h_{oe} we have, $A_i \approx - h_{fe}$ ...(1)

Input Impedance : From Table 4.2 the CE input impedance is given as

$$\boxed{R_i = h_{ie} + h_{re} A_i R_L}$$

By neglecting h_{re} we have,

$$R_i = h_{ie} \qquad \text{...(2)}$$

Voltage Gain : From Table 4.2 the voltage gain is given as

$$\boxed{A_v = \frac{A_i R_L}{R_i} = \frac{A_i R_L}{h_{ie}}} \qquad \text{...(3)}$$

Output Impedance : From Table 4.2 the CE output impedance is given as

$$\boxed{Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}} \qquad \text{...(3)}$$

By neglecting h_{oe} and h_{re}

$$Y_o = 0$$

$$\therefore \qquad R_o = \frac{1}{Y_o} = \infty \qquad \text{...(4)}$$

$$\boxed{R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L} \qquad \text{...(5)}$$

➡ **Example 4.3 :** *Consider a single stage CE amplifier with* $R_s = 1$ *K,* $R_1 = 50$ *K,* $R_2 = 2$ *K,* $R_C = 2$ *K,* $R_L = 2$ *K,* $h_{fe} = 50$*,* $h_{ie} = 1.1$ *K,* $h_{oe} = 25$ *μA/V and* $h_{re} = 2.5 \times 10^{-4}$*, as shown in Fig. 4.27.*

Find A_i, R_i, A_v, $A_i = \frac{I_L}{I_s}$, $A_{vs} = \frac{V_o}{V_s}$ *and* R_o.

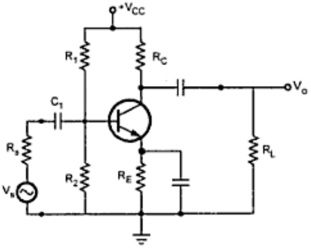


Fig. 4.27

Solution : Since $h_{oe}\, R'_L = 25 \times 10^{-6} \times (2\text{ K} \parallel 2\text{ K}) = 0.025$, which is less than 0.1, we use approximate analysis.

Fig. 4.28 shows the simplified hybrid model for the given circuit.

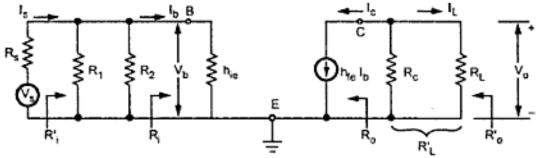


Fig. 4.28 Simplified hybrid model

a) Current gain $(A_i) = -h_{fe} = -50$

b) Input impedance $(R_i) = h_{ie} = 1.1\text{ K}$

$$R'_i = h_{ie} \parallel R_1 \parallel R_2 = 1.1\text{ K} \parallel 50\text{ K} \parallel 2\text{ K} = 700\ \Omega$$

c) Voltage gain $$(A_v) = \frac{A_i R_L}{R_i} = \frac{-50 \times (2\text{ K} \parallel 2\text{ K})}{1.1\text{ K}} = -45.45$$

d) Output impedance $$(R_o) = \frac{1}{Y_o} = \infty$$

$$R'_o = R_o \parallel R'_L = \infty \parallel 2\text{ K} \parallel 2\text{ K} = 1\text{ K}$$

e) Overall voltage gain $$(A_{vs}) = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s}$$

where $\frac{V_o}{V_b} = A_v$ and $\frac{V_b}{V_s} = \frac{R'_i}{R'_i + R_s}$

$$\therefore \quad A_{vs} = \frac{A_v\, R'_i}{R'_i + R_s} = \frac{-45.45 \times 700}{700 + 1\text{ K}} = -18.71$$

f) Overall current gain $$A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

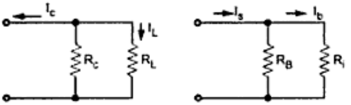


Fig. 4.29 & 4.30

$$\frac{I_L}{I_c} = -\frac{R_C}{R_C + R_L} = \frac{-1\text{ K}}{1\text{ K} + 1\text{ K}} = -0.5$$

$$\frac{I_c}{I_b} = h_{fe} = 50$$

Looking at Fig. 4.30 $$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{(50 \parallel 2)}{(50 \parallel 2)+1.1} = 0.636$$

$\therefore$ $$A_{i\ (\text{for circuit})} = \frac{I_L}{I_s} = -\ 0.5 \times 50 \times 0.636 = \mathbf{-\ 15.9}$$

4.6.2 Analysis of Common Collector Circuit using Simplified Hybrid Model

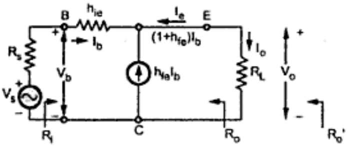


Fig. 4.31 Simplified CC model

We have seen the simplified CE model, in which input is applied to base and output is taken from collector, and emitter is common between input and output. The same simplified model can be modified to get simplified CC model. For simplified CC model, we have to make collector common and take the output from emitter, as shown in the Fig. 4.31. The h_{fe} I_b current direction is now exactly opposite that of CE model because the current h_{fe} I_b always points towards emitter.

Current Gain : It is defined as the ratio of output to input currents

$$\boxed{A_i = \frac{I_o}{I_b} = \frac{-I_e}{I_b} = 1 + h_{fe}} \qquad \ldots(6)$$

Input Resistance :

From Fig. 4.31 we obtain $$R_i = \frac{V_b}{I_b}$$

Applying KVL we have

$$V_b - I_b h_{ie} - I_o R_L = 0$$

$$\therefore \quad V_b = I_b h_{ie} + I_o R_L$$

$$\therefore \quad \frac{V_b}{I_b} = h_{ie} + \frac{I_o}{I_b} R_L$$

$$\therefore \quad \boxed{R_i = \frac{V_b}{I_b} = h_{ie} + (1 + h_{fe}) R_L} \quad \because \frac{I_o}{I_b} = \frac{-I_e}{I_b} = 1 + h_{fe} \qquad \ldots(7)$$

The above equation shows that input impedance of CC is higher than the CE configuration.

Voltage Gain (A_v) :

It is given as $A_v = \frac{V_o}{V_b} = \frac{I_o R_L}{I_b R_i} = \frac{A_i R_L}{R_i} \because A_i = \frac{I_o}{I_b} = \frac{-I_e}{I_b}$ ...(8)

Substituting values of A_i and R_i we get

$$\boxed{A_v = \frac{(1+h_{fe})R_L}{h_{ie}+(1+h_{fe})R_L} \cong 1}$$ but always less than 1 $\because$ $(1 + h_{fe})R_L >> h_{ie}$ ...(9)

Output Resistance R_o :

It is the ratio of output voltage V_o to output current I_e with $V_s = 0$

$$R_o = \left.\frac{V_o}{I_e}\right|_{V_s=0}$$

Applying KVL we have,

$V_s - I_b R_s - I_b h_{ie} - V_o = 0$

$$\therefore \quad V_o = -I_b R_s - I_b h_{ie} \quad \because V_s = 0 = -I_b(R_s + h_{ie})$$

$$I_e = -(1 + h_{fe}) I_b$$

$$\therefore \quad \frac{V_o}{I_e} = \frac{-I_b(R_s+h_{ie})}{-(1+h_{fe})I_b}$$

$$\therefore \quad \boxed{R_o = \frac{V_o}{I_e} = \frac{R_s+h_{ie}}{1+h_{fe}}} \qquad ...(10)$$

The output resistance R'_o of the stage, taking the load into account is given as

$$\boxed{R'_o = R_o \parallel R_L} \qquad ...(11)$$

➠ **Example 4.4 :** *A common collector circuit as shown in Fig. 4.32 has the following components : $R_1 = 27\ k\Omega$, $R_2 = 27\ k\Omega$, $R_E = 5.6\ k\Omega$, $R_L = 47\ k\Omega$, $R_s = 600\ \Omega$. The transistor parameters are $h_{ie} = 1\ k\Omega$, $h_{fe} = 85$ and $h_{oe} = 2\ \mu A/V$. Calculate A_i, R_i, A_v, R_o, $A_{vs} = \frac{Vo}{V_s}$ and $A_i = \frac{I_o}{I_s}$.*

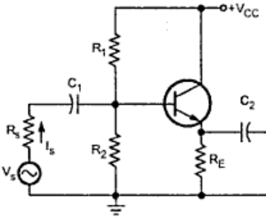

+V_CC
R_1
C_1
C_2
R_s
I_s
R_2
I_o
R_E
R_L
V_s

Fig. 4.32

Solution : Here, $h_{oe} \times R'_L = 2 \times 10^{-6} \times (5.6 || 47\ K) = 0.01$, which is less than 0.1. Thus we analyse the circuit with approximate method.

Fig. 4.33 shows the simplified hybrid model for the given circuit.

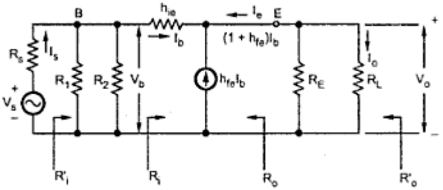

B
h_ie
I_e
E
I_b
(1 + h_fe)I_b
R_s
I_s
R_1
R_2
V_b
h_fe I_b
R_E
I_o
R_L
V_o
+
V_s
–
+
–
R'_i
R_i
R_o
R'_o

Fig. 4.33 Simplified hybrid model

a) Current gain $(A_i) = 1 + h_{fe} = 1 + 85 = 86$

b) Input resistance $(R_i) = h_{ie} + (1 + h_{fe})\, R'_L = h_{ie} + (1 + h_{fe})\, (R_E \parallel R_L)$

$$= 1K + (1 + 85)\,(5.6\ K \parallel 47\ K) = \mathbf{431.33\ k\Omega}$$

$$R'_i = R_i \parallel R_1 \parallel R_2 = 431.33\ K \parallel 27\ K \parallel 27\ K$$

$$= \mathbf{13.09\ K}$$

c) Voltage gain

$$(A_v) = \frac{(1+h_{fe})R_L'}{h_{ie}+(1+h_{fe})R_L'}$$

$$= \frac{(1+85)(5.6\text{ K} \parallel 47\text{ K})}{1\text{ K}+(1+85)(5.6\text{ K} \parallel 47\text{ K})} = \mathbf{0.997}$$

d) Output resistance

Looking Fig. 4.33 the output resistance

$$R_o = \frac{R_s'+h_{ie}}{1+h_{fe}} = \frac{(R_1 \parallel R_2 \parallel R_s)+h_{ie}}{1+h_{fe}}$$

$$= \frac{(27\text{ K} \parallel 27\text{ K} \parallel 600)+1\text{ K}}{1+85} = \mathbf{18.3\ \Omega}$$

$$R_o' = R_o \parallel R_E \parallel R_L = 18.3 \parallel 5.6\text{ K} \parallel 47\text{ K} = \mathbf{18.23\ \Omega}$$

e) Overall voltage gain $A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s},$

where $\frac{V_o}{V_b} = A_v$ and $\frac{V_b}{V_s} = \frac{R_i'}{R_i'+R_s}$

$$\therefore \quad A_{vs} = \frac{A_v\ R_i'}{R_i'+R_s} = \frac{0.997 \times 13.09\text{ K}}{13.09\text{ K}+600} = \mathbf{0.953}$$

f) Overall current gain $A_i = \frac{I_o}{I_s} = \frac{I_o}{I_e} \times \frac{I_e}{I_b} \times \frac{I_b}{I_s}$

where $\frac{I_o}{I_e} = \frac{-R_E}{R_E+R_L} = -\frac{5.6\text{ K}}{5.6\text{ K}+47\text{ K}} = -0.106$

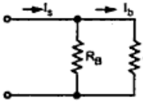


Fig. 4.34

$$\frac{I_e}{I_b} = -(1+h_{fe}) = -86$$

Looking at Fig. 4.34

$$\frac{I_b}{I_s} = \frac{R_B}{R_B+R_i} = \frac{(27\text{ K} \parallel 27\text{ K})}{(27\text{ K} \parallel 27\text{ K})+431.33\text{ K}} = 0.03$$

$$\therefore \quad A_{i(\text{for circuit})} = \frac{I_o}{I_s} = (-0.106)\times(-86)\times(0.03) = \mathbf{0.273}$$

e) Voltage gain A_{vs}

$$= \frac{A_v R_i'}{R_i' + R_s} = \frac{-382.13 \times 343.44}{343.44 + 10 \times 10^3} = -\mathbf{12.69}$$

f) Current Gain A_i (for circuit) $= \frac{I_2}{I_1} = \frac{I_2}{I_c} \frac{I_c}{I_b} \frac{I_b}{I_1}$

Looking at Fig. 4.42 and 4.43 and using current divider equation we get,

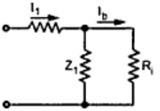
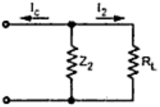


Fig. 4.42



4.43

$$I_b = \frac{I_1 Z_1}{Z_1 + R_i}$$

$$\therefore \quad \frac{I_b}{I_1} = \frac{Z_1}{Z_1 + R_i}$$

and $$I_2 = \frac{-I_C Z_2}{Z_2 + R_L}$$

$$\therefore \quad \frac{I_2}{I_c} = -\frac{Z_2}{Z_2 + R_L}$$

$$\therefore \quad A_i = \frac{I_2}{I_c} \frac{I_c}{I_b} \frac{I_b}{I_1} \; -\frac{Z_2}{Z_2 + R_L} \times (40.3) \times \frac{Z_1}{Z_1 + R_i}$$

$$= -\frac{200 \times 10^3}{200 \times 10^3 + 10\text{ K}} \times 40.3 \times \frac{522}{522 + 1004} = -\mathbf{13.13}$$

4.8 Analysis of Common-Emitter Amplifier with an Emitter Resistance

Whenever the gain provided by a single stage amplifier is not sufficient, it is necessary to cascade the number of stages of the amplifier. In such situations, it becomes important to stabilize the voltage amplification of each stage, because instability of the first stage is amplified in the second stage and it is further amplified in the next. This is not desired. The simple and effective way to obtain voltage gain stabilization is to add an emitter resistance R_E to a CE stage as shown in Fig. 4.44. The presence of emitter resistance has number of better effects on the amplifier performance. These effects can be analysed with the help of h-parameter equivalent circuit.

Current Gain (A_i) : The current gain can be given as

$$\boxed{A_i = \frac{-I_c}{I_b} = \frac{-h_{fe}I_b}{I_b} = -h_{fe}} \qquad \text{...(1)}$$

Input Resistance (R_i) : Look at Fig. 4.46 we can write input resistance as

$$\boxed{R_i = \frac{V_i}{I_b} = h_{ie} + (1 + h_{fe})\, R_E} \qquad \text{...(2)}$$

The input resistance due to factor $(1 + h_{fe})\, R_E$ may be very much larger than h_{ie}. Hence an emitter resistance greatly increases the input resistance.

Voltage Gain (A_v) : It is given as

$$\boxed{A_v = \frac{A_i R_L}{R_i} = \frac{-h_{fe}R_L}{h_{ie}+(1+h_{fe})R_E}} \qquad \text{...(3)}$$

Output Resistance (R_o) : It is the resistance of an amplifier without considering the source and load (i.e. $V_s = 0$ and $R_L = \infty$). It is defined as a ratio of output voltage V_o to output current with $V_s = 0$.

$$R_o = \left.\frac{V_o}{I_o}\right|_{V_s=0}$$

When $V_s = 0$, the current through the input loop $I_b = 0$, hence I_c and I_o both are zero. Therefore, $R_o = \infty$. The output resistance R'_o of the stage, taking the load into account is given as

$$\boxed{R'_o = R_o \parallel R_L = \infty \parallel R_L = R_L} \qquad \text{...(4)}$$

Example 4.7 : *Fig. 4.47 shows a single stage CE amplifier with unbypassed emitter resistance find current gain, input resistance, voltage gain and output resistance. Use typical values of h-parameter*

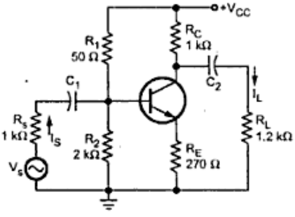


Fig. 4.47

Solution : Typical values for h-parameters are $h_{fe} = 50$, $h_{ie} = 1.1$ K, $h_{oe} = 25\ \mu A/V$, $h_{re} = 2.5 \times 10^{-4}$. Since $h_{oe} R_L = 25 \times 10^{-6} \times (1 \text{ K} \parallel 1.2 \text{ K}) = 0.0136$, which is less than 0.1, we use approximate analysis.

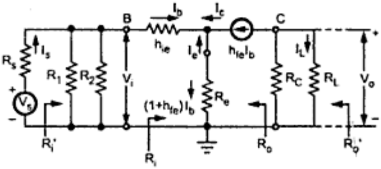


Fig. 4.48 (a) Approximate h-parameter equivalent circuit

a) Current Gain $(A_i) = \frac{-I_c}{I_b} = -h_{fe} = -50$

b) Input Resistance $(R_i) = \frac{V_i}{I_b} = h_{ie} + (1 + h_{fe}) R_E$

$$= 1.1 \text{ K} + (1 + 50) \times 270 = \mathbf{14.87\ K}$$

c) Voltage Gain $(A_v) = \frac{A_i R_L}{R_i} = \frac{-50 \times (1.2 \text{ K} \| 1 \text{ K})}{14.87 \text{ K}} = \mathbf{-1.834}$

d) Overall Input Resistance $(R_i') = R_i \parallel R_1 \parallel R_2 = 14.87 \text{ K} \parallel 50 \text{ K} \parallel 2 \text{ K} = \mathbf{1.7\ K}$

e) Output Resistance $(R_o') = R_o \parallel R_c \parallel R_L = \infty \parallel 1 \text{ K} \parallel 1.2 \text{ K} = \mathbf{545.45\ \Omega}$

f) Overall Voltage Gain $(A_{vs}) = \frac{A_v R_i'}{R_i' + R_s} = \frac{-1.834 \times 1.7 \text{ K}}{1.7 \text{ K} + 1 \text{ K}} = \mathbf{-1.15}$

g) Overall current gain $A_i = \frac{I_L}{I_s} = \frac{I_L}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$

where $\frac{I_L}{I_c} = \frac{-R_C}{R_C + R_L} = \frac{-1 \text{ K}}{1 \text{ K} + 1.2 \text{ K}} = \mathbf{-0.454}$

Looking at Fig. 4.48 (b) we can write

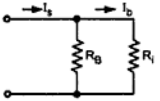


Fig. 4.48 (b)

$$Z_2 = R' = 40\text{ K}$$

$$A_i = \frac{-h_{fe}}{1+h_{oe}R'_L} \qquad \text{where } R'_L = Z_2 \parallel R_C$$

$$= 40\text{ K} \parallel 4\text{ K}$$

$$= 3.636\text{ K}$$

$$= \frac{-50}{1+\frac{1}{40\times10^3}\times3.636\times10^3}$$

$$= \mathbf{-45.83}$$

$$R_i = h_{ie} = \mathbf{1.11\ K}$$

$$A_v = \frac{A_i R'_L}{R_i} = \frac{-45.83\times3.636\times10^3}{1.11\times10^3}$$

$$= \mathbf{-150.12}$$

$$R_{if} = Z_1 \parallel R_i \qquad \text{where } Z_1 = \frac{R'}{1-A_v} = \frac{40\text{ K}}{1-(-150.12)}$$

$$= 264.69\ \Omega$$

$$\therefore \quad R_{if} = 264.69 \parallel 1.11\times10^3$$

$$= \mathbf{213.72\ \Omega}$$

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\times\frac{V_i}{V_s} \qquad \text{where } \frac{V_i}{V_s} = \frac{R_{if}}{R_{if}+R_s}$$

$$= \frac{213.72}{213.72+10\times10^3}$$

$$= 0.02$$

$$= A_v \times 0.02$$

$$= -150.12\times0.02$$

$$= \mathbf{-3.14}$$

Example 4.9 : *Determine A_v, A_I, R_i, R_o for a CE amplifier using npn transistor with $h_{ie} = 1200\ \Omega$, $h_{re} = 0$, $h_{fe} = 36$, $h_{oe} = 2\times10^{-6}$ mhos. $R_L = 2.5\ k\Omega$, $R_s = 500\ \Omega$ (neglect the effect of biasing circuit).*

Solution : h-parameter equivalent circuit for given circuit is as given below.

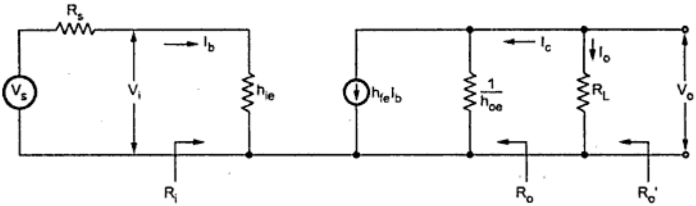


Fig. 4.51

$$A_i = \frac{-h_{fe}}{1+h_{oe}R_L} = \frac{-36}{1+2\times10^{-6}\times2.5\times10^3}$$

$$= \mathbf{-35.82}$$

$$R_i = h_{ie} = \mathbf{1.2\ K}$$

$$A_v = \frac{A_i R_L}{R_i} = \frac{-35.82\times2.5\times10^3}{1.2\times10^3} = \mathbf{-74.625}$$

$$Y_0 = h_{oe} \qquad \therefore\ R_o = \frac{1}{h_{oe}} = \frac{1}{2\times10^{-6}} = 500\ K$$

$$\therefore \quad R_o' = R_o \parallel R_L = 500\,K \parallel 2.5\,K = \mathbf{2.487\ K}$$

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\times\frac{V_i}{V_s} \qquad \text{where } V_i = \frac{V_s\times R_i}{R_i\times R_s}$$

$$\therefore\ \frac{V_i}{V_s} = \frac{R_i}{R_i+R_s} = \frac{1200}{1200+500} = 0.70588$$

$$\therefore A_{vs} = A_v\times0.70588$$

$$= -74.625\times0.70588$$

$$= \mathbf{-52.676}$$

Example 4.10 : *For the given circuit $h_{fe} = 100$, $h_{ie} = 1\ K$, $h_{re} = h_{oe} = 0$. Determine with $R_e = 0$*

i) $R_i' = \frac{V_o}{I_s}$ where $I_s = \frac{V_s}{R_s}$ ii) $A_{vs} = \frac{V_o}{V_s}$ iii) R_i iv) R_o'

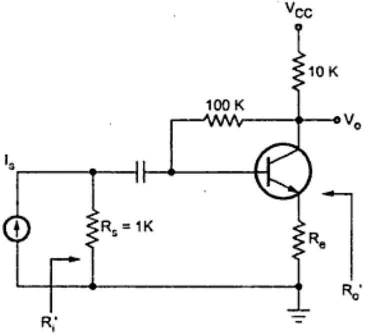

V_{CC}
10 K
100 K
V_o
I_s
R_s = 1K
R_e
R_o'
R_i'

Fig. 4.52

Solution : The h-parameter equivalent circuit for given circuit is as shown in Fig. 4.53.

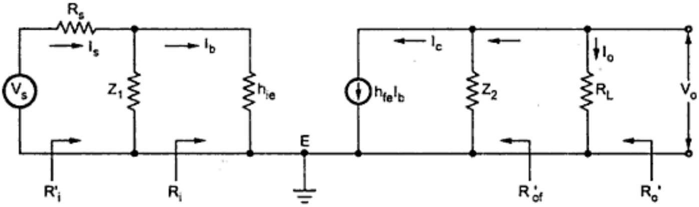

R_s
I_s
I_b
V_s
Z_1
h_{ie}
E
I_c
$h_{fe}I_b$
Z_2
I_o
R_L
V_o
R'_i
R_i
R'_{of}
R_o'

Fig. 4.53

Here, current source is converted into voltage source and resistance 100 K is splited using Millers theorem.

$$Z_2 = \frac{100\text{ K} \times A}{A-1} = 100\text{ K} \qquad \because A >> 1$$

$$A_i = \frac{-I_C}{I_b} = -h_{fe} = -100$$

$$R_i = -h_{ie} = 1000\ \Omega$$

$$A_v = \frac{V_o}{V_i} = \frac{A_i R'_L}{R_i} \qquad \text{where } R'_L = Z_2 \parallel R_L$$

$$= 100\text{ K} \parallel 10\text{ K}$$

$$= 9.09\text{ k}\Omega$$

$$= \frac{-100\times 9.09\times 10^{3}}{1000} = -\,909$$

$$R_i' = Z_1 \parallel R_i \quad \text{where } Z_1 = \frac{100\,\text{K}}{1-A} = \frac{100\,\text{K}}{1+909} = 109.89$$

$$= 109.89 \parallel 1000 = 99\ \Omega$$

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\times\frac{V_i}{V_s} \qquad \text{where } \frac{V_i}{V_s} = \frac{R_i'}{R_i'+R_s}$$

$$= -\,909\times 0.09 \qquad = \frac{99}{99+1000}$$

$$= \mathbf{-\,81.81} \qquad = 0.09$$

$$A_{is} = \frac{I_o}{I_s} = \frac{I_o}{I_c}\times\frac{I_c}{I_b}\times\frac{I_b}{I_s}$$

where

$$\frac{I_o}{I_c} = \frac{-Z_2}{Z_2+R_L} = \frac{-100\ \text{K}}{100\ \text{K}+10\ \text{K}} = -\,0.909$$

$$\frac{I_b}{I_s} = \frac{Z_1}{Z_1+R_i} = \frac{109.89}{109.89+1000} = 0.099$$

$$\therefore \quad A_{is} = \frac{I_o}{I_s} = -\,0.909\times 100\times 0.099 = -\,9$$

$$R_o = \infty$$

$$R_o' = \infty \parallel R_L' = \mathbf{9.09\ K}$$

Example 4.11 : *A transistor with* h_{ie} = *1.1 kΩ,* h_{fe} = *50,* h_{re} = 205×10^{-4}, h_{oe} = *25 μA/V is connected in C.E. configuration given in Fig. 4.54.*
Calculate : $A_i = \frac{I_o}{I_i}$, $A_{is} = \frac{I_o}{I_s}$, A_v, A_{vs}, R_i *and* R_o.

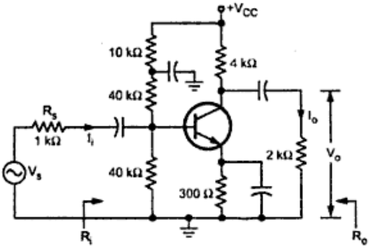


Fig. 4.54

Solution : Since $h_{oe} R_L = 25 \times 10^{-6}$ (2 K $\|$ 4 K) = 0.033, which is less than 0.1, we use approximate analysis. The Fig. 4.54(a) shows the approximate equivalent model for the given circuit.

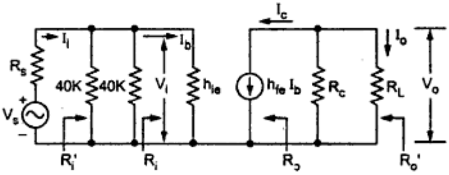


Fig. 4.54(a)

a) Current Gain $(A_i) = \frac{-I_c}{I_b} = -h_{fe} = -50$

b) Input Resistance $(R_i) = h_{ie} = 1.1\ k\Omega$

c) Overall input resistance $R_i' = R_i \| R_1 \| R_2$

$= 1.1\ K \| 40\ K \| 40\ K = 1.042\ K$

d) Voltage Gain $(A_v) = \frac{V_o}{V_i} = \frac{A_i R_L}{R_i} = \frac{-50 \times (2\ K \| 4\ K)}{1.1\ K} = -60.6$

e) Overall voltage gain $A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_v \times \frac{R_i'}{R_i' + R_s}$

$$= -60.6 \times \frac{1.042\ K}{1.042\ K + 1\ K} = -30.92$$

f) Overall current gain $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_i}$

where $\frac{I_o}{I_c} = \frac{-R_c}{R_c + R_L} = \frac{4\ K}{4\ K + 2\ K} = -0.666$

$$\frac{I_c}{I_b} = h_{fe} = 50$$

Looking at Fig. 4.54(b) $\frac{I_b}{I_i} = \frac{R_1 \| R_2}{R_1 \| R_2 + R_i} = \frac{40\ K \| 40\ K}{40\ K \| 40\ K + 1.1\ K} = 0.947$

$\therefore$ $A_i = \frac{I_o}{I_i} = (-0.666) \times 50 \times 0.947 = -31.53$

If transistor is driven by current source instead of voltage source, A_{is} is given by,

$$A_{is} = \frac{I_o}{I_s} = \frac{I_o}{I_c} \times \frac{I_c}{I_b} \times \frac{I_b}{I_s}$$

where $$\frac{I_o}{I_e} = -1$$

$$\frac{I_e}{I_b} = -A_i = -101$$

$$\frac{I_b}{I_i} = \frac{R}{R+R_i} = \frac{390}{390+568.97} = 0.406$$

$$\therefore \quad A_{i(\text{for circuit})} = \frac{I_o}{I_i} = (-1) \times (-101) \times (0.406) = 41$$

Example 4.14 : *Given* $I_E = 1.2$ *mA,* $\beta = h_{fe} = 120$*,* $r_o = \frac{1}{R_0} = 40$ *kΩ. Sketch the :*

i) Common-Emitter hybrid equivalent model.

ii) Common-Base hybrid equivalent model. **(Dec. - 2002)**

Solution : Now first calculate

$$I_B = \frac{I_E}{1+\beta} = \frac{1.2 \text{ mA}}{121} = 9.9 \ \mu\text{A}$$

$$I_C = \beta \, I_B = 1.19 \text{ mA}$$

(i) CE-hybrid equation model

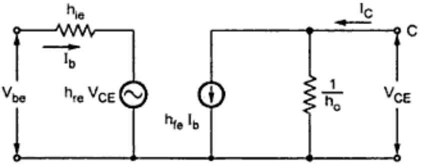
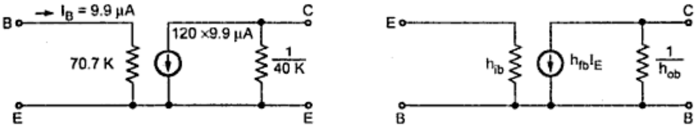

h_{ie}
I_b
I_C
C
V_{be}
h_{re} V_{CE}
h_{fe} I_b
$\frac{1}{h_o}$
V_{CE}

Fig. 4.57 (a)

Neglecting, h_{re} V_{CE}


B
$I_B = 9.9$ μA
C
70.7 K
120 ×9.9 μA
$\frac{1}{40 \text{ K}}$
E
E
E
C
h_{ib}
$h_{fb}I_E$
$\frac{1}{h_{ob}}$
B
B

(b) (c)

Fig. 4.57

We have $$\frac{1}{h_{oe}} >> R_L \; r_o = \frac{1}{h_{oe}}$$

$$h_{ie} = \frac{V_{be}}{I_b} = \frac{0.7\text{ V}}{9.9\ \mu\text{A}} = 70.7\text{ K}$$

$$h_{fe}I_b = 120 \times 9.9\ \mu\text{A}$$

(ii) By similar argument

where $$h_{ib} = \frac{0.7\text{ V}}{I_E}$$

$$h_{ob} = \frac{1}{r_o}.$$

Example 4.15 : *A CE amplifier has the following h-parameters :*

$h_{ie} = 1.1$ *kΩ,* $h_{re} = 0.25 \times 10^{-3}$, $h_{fe} = 50$, $h_{oe} = 25\ \mu$ *mho*

If the load resistance is 1 kΩ and source resistance is also 1 kΩ, find

(i) Current gain (ii) voltage gain

Solution :

Given CE-Parameter

$h_{ie} = 1.1\text{ k}\Omega$

$h_{re} = 0.25 \times 10^{-3}$ $R_L = 1\text{ k}\Omega$

$h_{fe} = 50$ $R_S = 1\text{ k}\Omega$

$h_{oe} = 25\ \mu\text{ mho}$

(i) Current gain

$$A_i = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

$$= \frac{-50}{1 + 25 \times 10^{-6} \times 1 \times 10^3}$$

$$= \frac{-50}{1 + 25 \times 10^{-3}}$$

$$= \frac{-50}{1 + .025} = \frac{-50}{1.025}$$

$$= \mathbf{-48.78}$$

(ii) Voltage gain

$$A_v = A_i \times \frac{R_L}{R_i}$$

where $$R_i = h_{ie} + h_{re}A_iR_L$$

Review Questions

1. *Write a short note on 'transistor as an amplifier '.*
2. *Draw a typical common emitter amplifier and explain the function of each component in it.*
3. *Explain the single stage CE amplifier.*
4. *Explain the need of* C_1, C_2 *and CE.*
5. *What do you understand by the term 'equivalent circuit' of a transistor ? Draw the equivalent circuit of the generalized transistor amplifier and explain the significance of each parameter.*
6. *For the three configurations of a BJT, we required three different sets of 'h' parameters justify.*
7. *List the benefits of h-parameters.*
8. *Draw the 'h' parameter equivalent circuit for a typical common emitter amplifier and derive expression for* A_i, R_i, A_v *and* R_o'.
9. *Compare common collector and common emitter configuration with regards to* R_I, R_O, A_I, A_v.
10. *Give the general guidelines for analysis of a transistor circuit*
11. *The transistor amplifier shown in Fig. 4.59 uses a transistor whose h-parameters are as follows :* $h_{ie} = 1.2$ *K,* $h_{fe} = 75$, $h_{re} = 2.4 \times 10^{-4}$, $h_{oe} = 25 \times 10^{-6}$ *A/V. Calculate* I_o / I_i, A_v, A_{vs}, R_o' *and* R_i'.

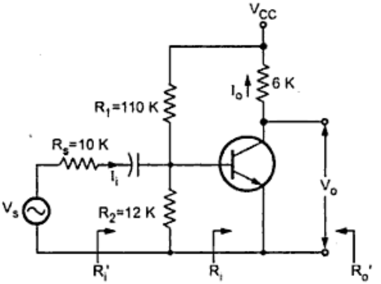


Fig. 4.59

(Ans. : i) $I_o / I_i = -58.24$, **ii)** $A_v = -302.36$,
iii) $A_{vs} = -30.22$, **iv)** $R_o' = 5.217$ **kΩ, v)** $R_i' = 1.155$ **K)**

12. *The small signal h-parameter a.c. equivalent circuit of a certain transistor connected in CE configuration is shown in Fig. 4.60.*

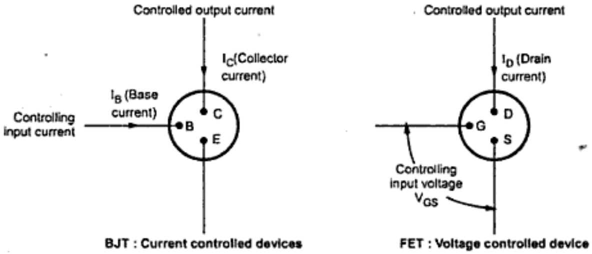
5

Field Effect Transistor

5.1 Introduction

The Field Effect Transistor abbreviated as **FET** is an another semiconductor device like a BJT which can be used as an amplifier or switch. Like BJT, FET is also a three terminal device; however, the principle of operation of FET is completely different from that of BJT.

The three terminals of FET are named as Drain (D), Source (S) and Gate (G), as shown in the Fig. 5.1. Out of these three terminals gate terminal acts as a controlling terminal.



Controlled output current
I_C(Collector current)
I_B (Base current)
Controlling input current
C
B
E
BJT : Current controlled devices
Controlled output current
I_D (Drain current)
D
G
S
Controlling input voltage V_{GS}
FET : Voltage controlled device

Fig. 5.1 Controlling element for BJT and FET

FET : Voltage Controlled Device

As shown in the Fig.5.1, in BJT the output current, I_C is controlled by the base current I_B. Hence BJT is a current controlled device. On the other hand, in FET, the voltage applied between gate and source (V_{GS}) controls the drain current I_D. Therefore, FET is a voltage controlled device. The name "**field effect**" is derived from the fact that the output current flow is controlled by an electric field set up in the device by an externally applied voltage between gate and source terminals.

FET : Unipolar Device

We know that in BJT, the current is carried by both electrons and holes, and hence the name **"bipolar"** junction transistor. However in FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called **unipolar device.**

FET : Other Important Features

- Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is **more temperature stable** as compared to the BJT.
- FET has very high input impedance. Typically, it is in the range of one to several megaohms. Because FETs have higher input impedance than BJT they are preferred in amplifiers where high input impedance is required.
- FETs require less space than that for BJTs, hence they are preferred in integrated circuits.

FET : Different Types and Application Areas

The FETs are categorised as :

- Junction Field Effect Transistors (JFETs),
- Metal Semiconductor Field Effect Transistors (MESFETs)
- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

The JFETs and MESFETs are further classified into two types as, n-channel JFET/MESFET and p-channel JFET/MESFET and MOSFETs are further classified into two types as, depletion MOSFET and enhancement MOSFET. The Fig. 5.2 shows the different types of FETs.

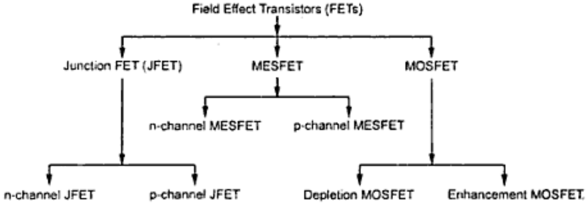

Field Effect Transistors (FETs)
Junction FET (JFET)
MESFET
MOSFET
n-channel MESFET
p-channel MESFET
n-channel JFET
p-channel JFET
Depletion MOSFET
Enhancement MOSFET

Fig. 5.2 Different types of FETs

In the junction FET, the gate junction may be a pn junction, which forms a pn JFET or simply JFET, or a Schottky barrier junction, which forms a metal semiconductor FET or MESFET.

In general, like BJTs the FETs can be used in switch, digital and linear amplifier applications. Because of Schottky barrier junction MESFETs have smaller transit time and faster response. Hence they are used in very high speed or high frequency applications, such as microwave amplifiers.

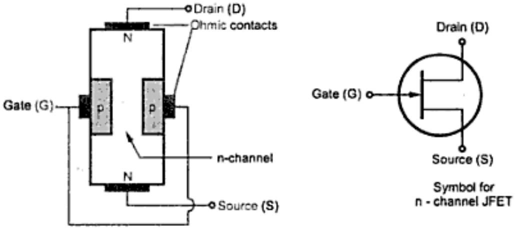
In JFET, there is a direct electrical connection between the gate terminal and the channel of a JFET. On the other hand, in MOSFETs, the gate is insulated from the channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, in MOSFETs, there is no direct electrical connection between the gate terminal and the channel. Due to this extra layer the input resistance of MOSFET is very very high.

The MOSFETs can be used in place of resistors in a circuit, so that circuits containing only MOSFETs can be designed. The MOSFET, compared to BJTs, can be made very small (that is, it occupies a very small area on an IC). Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high-density VLSI circuits, including microprocessors and memories, can be fabricated using MOSFETs. The MOSFET has made possible the hand-held calculator and the powerful personal computer. MOSFETs can also be used in analog circuits.

5.2 Basic Construction

5.2.1 Construction of n-channel JFET and Symbol

The Fig. 5.3 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and at its two ends, two ohmic contacts are made which are the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the **channel**. Since this channel is in the n type bar, the FET is known as **n-channel JFET.**



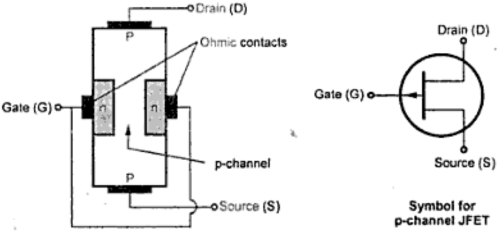
Symbol for n - channel JFET

Fig. 5.3 Structure and symbol for n-channel JFET

The electrons enter the channel through the terminal called **source** and leave through the terminal called **drain**. The terminals taken out from heavily doped electrodes of p type material are called **gates**. Usually, these electrodes are connected together and only one terminal is taken out, which is called **gate**, as shown in the Fig. 5.3.

5.2.2 Construction of p-channel JFET and Symbol

The device could be made of p type bar with two n type gates as shown in the Fig. 5.4. Then this will be **p-channel** JFET. The principle of working of n-channel JFET and p-channel JFET is similar; the only difference being that in **n-channel** JFET the current is carried by electrons while in **p-channel JFET**, it is carried by holes.


Drain (D)
P
Ohmic contacts
Gate (G)
n
n
p-channel
P
Source (S)
Drain (D)
Gate (G)
Source (S)

Symbol for p-channel JFET

Fig. 5.4 Structure and symbol for p-channel JFET

5.3 Transistor Action

5.3.1 Unbiased JFET

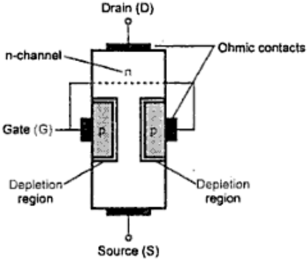

Drain (D)
n-channel
n
Ohmic contacts
Gate (G)
p
p
Depletion region
Depletion region
Source (S)

Fig. 5.5 Junction field effect transistor

In the absence of any applied voltage, JFET has gate channel junctions under no bias conditions. The result is a depletion region at each junction, as shown in Fig. 5.5.

This represents same depletion region of a diode under no bias conditions. Recall also that depletion region is that region which does not have any free carriers and therefore is unable to support conduction through the region.

5.3.2 Principle of Operation of JFET

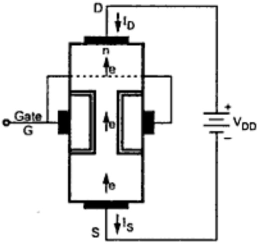
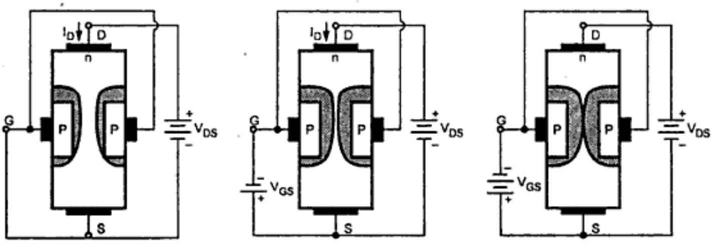


Fig. 5.6 n- channel JFET with gate open and V_{DD} is applied between drain and source

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero; the gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit shown in Fig. 5.6. As shown in Fig. 5.6, voltage V_{DD} is applied between drain and source. Gate terminal is kept open. The bar is of n-type material. Due to the polarities of applied voltage as shown in Fig. 5.6, the majority carriers i.e. the electrons start flowing from the source to the drain. This flow of electrons makes the drain current, I_D.

The majority carriers (electrons in n-channel JFET and holes in p-channel JFET) move from source to drain through the space between the gate regions. This space is commonly known as **channel**. The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel- width and on drain current I_D, consider the diagram shown in Fig. 5.7.



(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

Fig. 5.7

Fig. 5.7 (a) shows that an n-channel JFET with the gate directly connected to the source terminal. When drain voltage V_{DS} is applied, a drain current I_D flows in the direction shown. Since the n-material is resistive, the drain current causes a voltage drop along the channel. This voltage drop reverse biases the pn junctions, and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will mainly be spread in the channel shown in the Fig. 5.7(a). This penetration depends on the reverse bias voltage. Looking at Fig. 5.7(a) we can observe that depletion region width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction; it gradually increases from source side to drain side.

JFET as Voltage Controlled Current Source

As we know, depletion region does not contain charge carriers, the space between two depletion regions is available for the conducting portion of the channel. If we externally apply reverse bias voltage to the gate, the reverse bias will further increase and hence increase the penetration of the depletion region, which reduces the width of the conducting portion of the channel. As width of the conducting portion of the channel reduces, the number of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces. If we go on increasing the reverse bias voltage to the gate as shown in Fig. 5.7(b) and 5.7(c), depletion regions will increase more and more, and stage will come when the width of the depletion regions will be equal to the original width of the channel, leaving zero width for conducting portion of the channel, as shown in the Fig. 5.7(c). This will prevent any current flow from drain to source and this will cut off the drain current. The gate to source voltage that produces cutoff is known as **cutoff voltage** and it is denoted by $V_{GS(off)}$.

When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by I_{DSS} and this is the maximum possible drain current in JFET. From above discussion it is cleared that the gate to source voltage controls the current flowing through channel and hence FET is also called **voltage controlled current source.**

Key Point : *The JFET is always operated with gate - source pn junction reverse-biased.*

5.4 JFET V-I Characteristics

To understand electrical behaviour of a JFET, it is necessary to study the interrelation of the current and voltages in JFET. These relationships can be plotted graphically which are commonly known as the **characteristics of JFET**. The important characteristics of JFET are drain characteristics and transfer characteristics. The following section explains these characteristics in detail.

5.4.1 Drain V-I Characteristics for n-channel JFET

Fig. 5.8 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current I_D and drain to source voltage V_{DS} for different values of V_{GS}. Fig. 5.9 shows the experimental setup required to plot this characteristics.

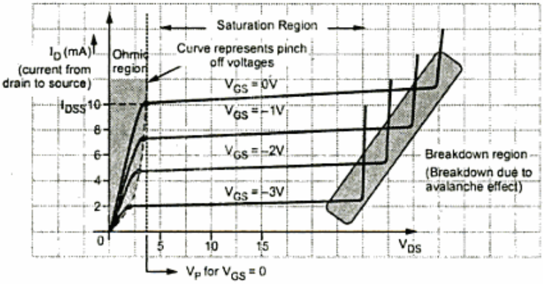


Fig. 5.8 Drain V-I characteristics of n-channel JFET

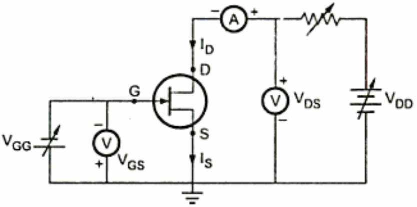


Fig. 5.9 Experimental setup to plot JFET characteristics

From this characteristics we observe following points :

1. V_{GS} and V_{DS} both = 0 :

When V_{GS} = 0 the channel is entirely open. But V_{DS} = 0, so there is no attractive force for the majority carriers (electrons in n-channel JFET) and hence drain current does not flow.

Key Point: *The curves are identical except that votlage V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.*

5.4.3 Transfer Characteristics for n-channel JFET

Fig. 5.12 shows the transfer characteristics of n-channel JFET. The curves represents relationship between the drain current I_D and gate to source voltage V_{GS}.

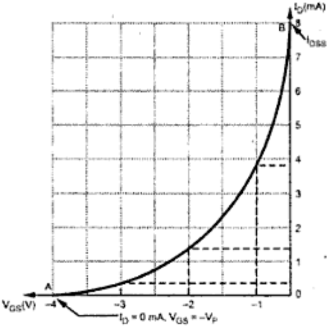


Fig. 5.12 Transfer characteristics of n-channel JFET

From this characteristics we observe following points :

1. The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear. This relationship is defined by **Shockley's** equation

$$\boxed{I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2} \qquad \dots (1)$$

The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From equation we can also write,

$$\boxed{V_{GS} = V_P\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)} \qquad \dots (2)$$

In the equation values of I_{DSS} and V_P are constants, value of V_{GS} controls I_D .

2. A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS\,(off)}$, and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at V_{GS} =0). Thus, this curve shows the operating limits of a JFET.

These are : $I_D = 0$ when $V_{GS} = V_{GS\,(off)}$

$I_D = I_{DSS}$ when $V_{GS} = 0$

Example 5.1 : *Data sheet for a JFET indicates that $I_{DSS} = 10$ mA and $V_{GS(off)} = -4$ V. Determine the drain current for $V_{GS} = 0$ V, -1 V and -4 V.*

Solution : For $V_{GS} = 0$ V, $I_D = I_{DSS} = 10$ mA

For $V_{GS} = -1$, using equation (1) we have

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = 10\text{ mA}\left(1-\frac{-1}{-4}\right)^2$$

$$= 10\times10^{-3}\,[1-0.25]^2 = 10\times10^{-3}\times\ 0.5625 = \mathbf{5.625\ mA}$$

For $V_{GS} = -4$ V

$$I_D = 10\text{ mA}\left(1-\frac{-4\text{V}}{-4\text{V}}\right)^2 = 10\times10^{-3}\,(1-1)^2$$

$$= 10\times10^{-3}\,(0)^2 = \mathbf{0\ mA}$$

Obtaining the Transfer Characteristics from Drain Characteristics

The transfer characteristic curve can be developed from the drain characteristics curves by plotting values of I_D for the values of V_{GS} taken from the set of drain curves in the pinch off region. This is illustrated in Fig. 5.13. Each point on the transfer characteristics curve corresponds to specific values of V_{GS} and I_D on the drain curves. For example, when $V_{GS} = -2$ V, $I_D = 4.32$ mA.

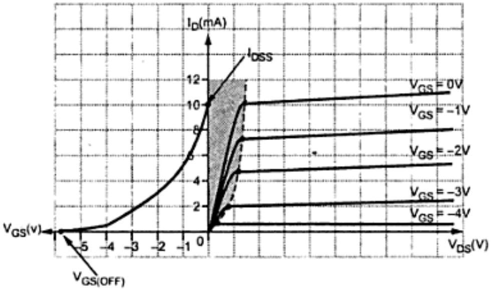


Fig. 5.13 Obtaining the transfer characteristics from drain characteristics

5.4.4 Transfer Characteristics for p-channel JFET

The Fig. 5.14 shows the transfer characteristics of p-channel JFET. It is identical to transfer characteristics of n-channel JFET except that the polarities of V_{GS} and I_D are reversed.

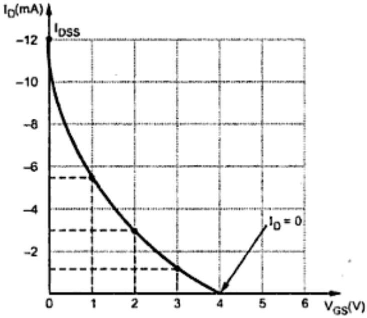


Fig. 5.14 Transfer characteristics of p-channel JFET

Key Point: *Polarities of V_{GS} and I_D are reversed than that of the characteristics of n-channel JFET.*

5.5 JFET Parameters

The important parameters of JFET are as follows :

- Transconductance (g_m)
- Input reistance and capacitance
- Drain to source resistance (r_d)
- Amplification factor (μ)

5.5.1 Transconductance

The transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant as shown in Fig. 5.15.

Looking at Fig. 5.15, we can say that it is the slope of the transfer characteristic. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS\ \text{constant}}} \qquad \text{... (1)}$$

The transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS (millisiemen) or mA/V. For given g_m, we can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation

$$\boxed{g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]} \qquad \text{... (2)}$$

where g_{mo} is the value of g_m for $V_{GS} = 0$, and is given by,

$$\boxed{g_{mo} = \frac{-2\,I_{DSS}}{V_P}} \qquad \text{... (3)}$$

This can be proved as given below. We know that,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Differentiating this equation with respect to V_{GS} we get,

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2\,I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

$$= g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right] \qquad \text{where} \quad g_{mo} = \frac{-2\,I_{DSS}}{V_P}$$

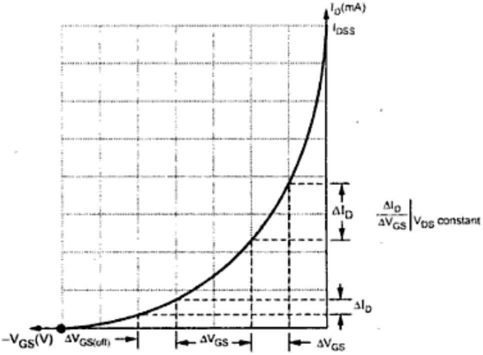


Fig. 5.15 Transconductance g_m varies depending on the bias point (V_{GS})

Example 5.2 : *For JFET, if I_{DSS} = 20 mA, $V_{GS(off)}$ = –5 V, and g_{mo} = 4 mS or mA/V. Determine the transconductance for V_{GS} = – 4 V, and find I_D at this point.*

Solution : From equation (2) we have,

$$g_m = g_{mo}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right] = 4\times10^{-3}\left[1-\frac{-4V}{-5V}\right]$$

$$= 4\times10^{-3}\times\ 0.2 = \mathbf{0.8\ mS}$$

We have,

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2 = 20\times10^{-3}\left[1-\frac{-4V}{-5V}\right]^2$$

$$= 20\times10^{-3}\times0.04$$

$$= \mathbf{0.8\ mA}$$

5.5.2 Input Resistance and Capacitance

We know that a JFET operates with its gate source junction reverse-biased. Therefore, the input resistance at the gate is very high. This high input resistance is one advatnage of the JFET over the bipolar transistor. (Recall that a BJT operates with a forward biased base-emitter junction.) JFET data sheets often specify the input resistance by giving a value of the gate reverse current, I_{GSS}, at a cetain gate to surce voltage, V_{GS}. The input resistance can then be determined using the following equation, where the vertical lines indicate an absolute value.

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

For example, the 2N3909 data sheet lists a maximum I_{GSS} of 10 nA for V_{GS} = 10 V at 25 °C. Therefore,

$$R_{IN} = \left|\frac{10\ V}{10\ nA}\right| = 1000\ M\Omega$$

From data sheet we can also observe that I_{GSS} is 1.0 μA for V_{GS} = 10 V at 100 °C. This shows that I_{GSS} increases with temperature. Here,

$$R_{IN} = \left|\frac{10\ V}{1\ \mu A}\right| = 10\ M\Omega$$

Key Point : *The input resistance decreases with increase in temperature.*

The input capacitance, C_{iss}, is a result of the JFET operating with a reverse biased pn junction. Recall that a reverse biased pn junction acts as a capacitor whose capacitance depends on the amount of reverse voltage. For example, the 2N3909 has a maximum C_{iss} of 32 pF for V_{GS} = 0.

5.6 Biasing of JFET

5.6.1 Fixed Bias Circuit

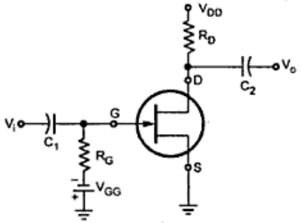


Fig. 5.17 Fixed bias circuit for n-channel circuit

Fig. 5.17 shows the fixed bias circuit for the n-channel JFET. This is the simplest biasing arrangement. To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

DC Analysis

For the dc analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero. This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit as shown in the Fig. 5.18.

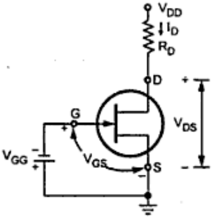


Fig. 5.18 Simplified fixed bias circuit

We know for dc analysis

$$I_G = 0 \text{ A}$$

and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore \; V_{GS} = -V_{GG} \qquad \text{... (1)}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, and hence the name fixed bias circuit.

For fixed bias circuit the drain current I_D can be calculated using equation.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

The drain to source voltage of output circuit can be determined by applying KVL.

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D \qquad \text{... (2)}$$

The **Q** point of the JFET amplifier with fixed bias circuit is given by :

$$\mathbf{I_{DQ}} = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

$$\mathbf{V_{DSQ}} = V_{DD} - I_{DQ} R_D$$

Example 5.3 : *For the circuit shown in the Fig. 5.19. Calculate*

a) V_{GSQ}, *b)* I_{DQ}, *c)* V_{DSQ}, *d)* V_D

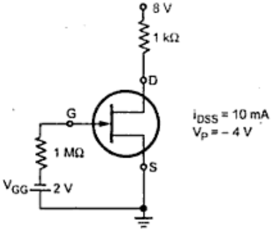


Fig. 5.19

Solution :

a) $V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$

b) $I_{DQ} = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 10\times10^{-3}\left(1-\frac{-2\text{ V}}{-4\text{ V}}\right)^2$

$= 10\times10^{-3}\,(1-05)^2 = 10\times10^{-3}\,(0.25) = \mathbf{2.5\ mA}$

c) $V_{DSQ} = V_{DD} - I_{DQ}R_D = 8\text{ V} - 2.5\times10^{-3}\,(1\times10^{3}) = \mathbf{5.5\ V}$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = \mathbf{5.5\ V}$

5.6.2 Voltage Divider Bias Circuit

The Fig. 5.20 shows n-channel JFET with voltage divider bias. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased. The source voltage is,

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula :

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \qquad \because I_G = 0$$

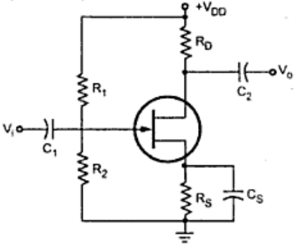


Fig. 5.20 Voltage divider bias for n-channel JFET

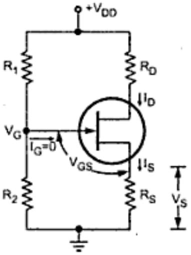


Fig. 5.21 Simplified voltage divider circuit for dc analysis

DC Analysis :

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$= V_G - I_D R_S \qquad \because I_D = I_S$$

$$\therefore V_{GS} = V_G - I_D R_S \qquad \dots (3)$$

Applying KVL to the output circuit we get,

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$= 12\times10^{-3}\left(1-\frac{(4-I_D\times2\times10^3)}{-4}\right)^2$$

$$= 12\times10^{-3}\ (1-[(-1)+500I_D])^2$$

$$= 12\times10^{-3}\ (2-500I_D)^2$$

$$= 12\times10^{-3}(4-2000I_D+250000I_D^2)$$

$$I_D = (0.048-24I_D+3000I_D^2)$$

$$\therefore\ 3000I_D^2-25I_D+0.048 = 0$$

Solving quadratic equation using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we get,

$$= \frac{-(-25)\pm\sqrt{(-25)^2-4(3000)(0.048)}}{2(3000)}$$

$$= \frac{25\pm\sqrt{625-576}}{6000} = \frac{25\pm\sqrt{49}}{6000} = \frac{25\pm7}{6000}$$

$$= 5.33\text{ mA or }3\text{ mA}$$

If we calculate value of V_{DS} taking $I_D = 5.33$ mA we get,

$$V_{DS} = V_{DD}-I_D(R_D+R_S)$$

$$= 12-5.33\times10^{-3}(1.2K+2K) = 12-17.07$$

$$= -5.07$$

Practically, the value of V_{DS} must be positive, hence $I_D = 5.33$ mA is invalid.

$$\therefore I_D = \mathbf{3\ mA,}$$

$$V_{DS} = 12-3\times10^{-3}(1.2\times10^3+2\times10^3)$$

$$= 12-9.6 = 2.4\text{ V}$$

$$\therefore V_{DS} = \mathbf{2.4\ V}$$

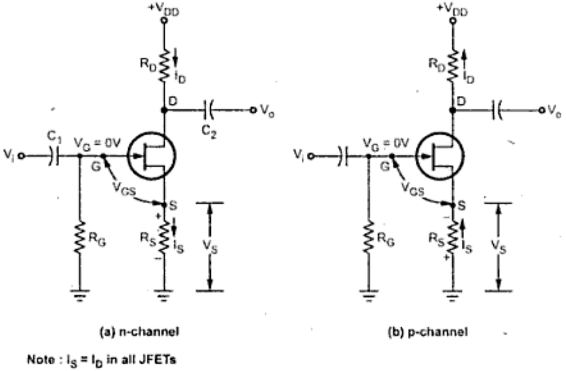
$$V_{GS} = 4-I_DR_S = 4-3\times10^{-3}\times2\times10^3 = 4-6$$

$$= \mathbf{-2\ V}$$

$$V_S = I_D\,R_S = 3\times10^{-3}\times2\times10^3 = \mathbf{6\ V}$$

5.6.3 Self Bias Circuit

Self bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. 5.23. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor, R_S makes gate source junction reverse biased.



(a) n-channel

(b) p-channel

Note : $I_S = I_D$ in all JFETs

Fig. 5.23 Self bias circuits for JFET

For the n-channel FET in Fig. 5.23 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For the p-channel FET in Fig. 5.23 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = -I_S R_S = -I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = +I_D R_S$$

$$V_{GS} = -V_S$$

$$\therefore V_{GS} = -I_D R_S$$

These equations can be used with a transfer characteristics (transconductance curve) to find the Q point of a self-bias line.

Drawing the Self Bias Line

Fig. 5.26 shows a typical transfer characteristics (transconductance curve) for a self biased JFET. The maximum drain current is 6 mA, and the gate-source cut-off voltage is –3 V. This means the gate voltage has to be between 0 and – 3 V.

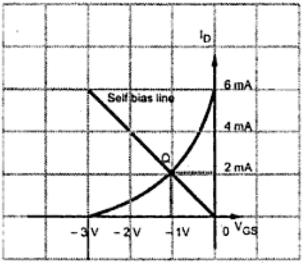


Fig. 5.26 Transfer characteristics

Now using equation $V_{GS} = -I_D R_S$ and assuming R_S of any suitable value we can draw the self bias line.

Let us assume, $R_S = 500\ \Omega$.

With this R_S we can plot two convenient points corresponding to $I_D = 0$ and $I_D = I_{DSS}$. At first point, $I_D = 0$

$$\therefore V_{GS} = -0\ (500\ \Omega) = 0 \text{ V and}$$

At second point, $I_D = 6$ mA

$$\therefore V_{GS} = -(6 \text{ mA})(500\ \Omega) = -3 \text{ V}$$

This gives the coordinates of two points as (0, 0) and (6 mA, –3 V) respectively. By plotting these two points, we can draw the straight line through the points as shown in the Fig. 5.26. This line will intersect the transconductance curve and it is known as **self bias line**. The intersection point gives the operating point of the self-bias JFET for this circuit. At operating point the drain current is slightly greater than 2 mA and the gate source voltage is slightly greater than –1 V.

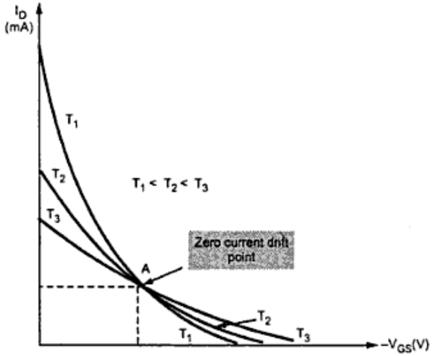


Fig. 5.29 Transfer characteristics for an n-channel FET as a function of temperature T

Derivation of condition for zero drift

Since a change in gate voltage ΔV_{GS} causes a change in drain current of $g_m \Delta V_{GS}$ i.e. $\Delta I_D = g_m \Delta V_{GS}$, then the condition for zero drift is

$$0.007\,|I_D| = 0.0022\,g_m$$

In above equation we have substituted the change in I_D and change in V_{GS} for 1°C.

$$\therefore \qquad \frac{|I_D|}{g_m} = 0.314\text{V}$$

By substituting,

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2 \text{ and } g_m = \frac{-2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V_P}\right]$$

we get,

$$\frac{I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2}{\frac{-2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V_P}\right]} = \frac{|V_P|-|V_{GS}|}{-2} = 0.314\text{V}$$

$$\therefore \qquad \boxed{|V_P|-|V_{GS}| = -0.628\text{ V} \approx -0.63\text{V}} \qquad \cdots (7)$$

From the above equation, if we know value of V_P, we can obtain the value of V_{GS} for zero drift current.

Assume that it is necessary to bias the JFET at a drain current I_D which will not drift outside of $I_D = I_A$ and $I_D = I_B$ i.e. I_D should be in between I_A and I_B. Then the bias line $V_{GS} = - I_D R_S$ must intersect the transfer characteristics between the points A and B, as indicated in Fig. 5.30 (a). The source of the bias line is decided by the source resistance R_S. The current I_Q always have value between I_A and I_B such that

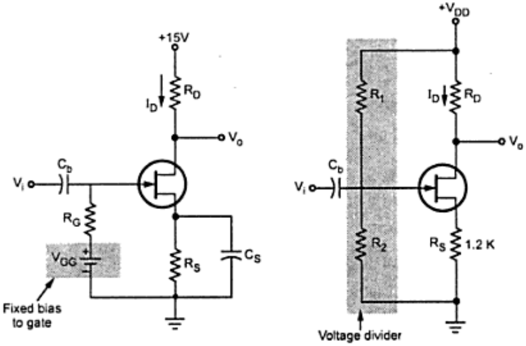
$$I_A < I_Q < I_B$$

Practical Way to Achieve Biasing Against Device Variation

Consider the physical situation indicated in Fig. 5.30 (b). Here a line drawn to pass between points A and B does not pass through the origin. This practical bias line is represented mathematically as,

$$V_{GS} = V_{GG} - I_D R_S$$

Such a bias relationship may be obtained by adding a fixed bias to the gate in addition to the self bias, as shown in the fig. 5.31(a). The circuit shown in Fig. 5.31(a) requires two power supplies. The self bias circuit with additional voltage divider requires only one power supply as shown in Fig. 5.31 (b).



(a) Biasing a FET with a fixed bias V_{GG} in addition to self bias through R_S

(b) Biasing a FET with a single power supply

Fig. 5.31

For the circuit shown in Fig. 5.31(b)

$$V_{GG} = \frac{R_2 V_{DD}}{R_1 + R_2} \quad R_g = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

5.7 MOSFETs

The MOSFET differs from the JFET in that it has no pn junction structure ; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called **IGFETs**. In the following sections we examine depletion type and enhancement type MOSFET with their basic constructions, operations, characteristics.

5.7.1 Depletion MOSFET (D-MOSFET)

5.7.1.1 Construction of n-channel MOSFET

The Fig. 5.35 shows the basic construction of n channel depletion type MOSFET. Two highly doped n regions are diffused into a lightly doped p type substrate. These two highly doped n regions represent source and drain. In some cases substrate is internally connected to the source terminal.

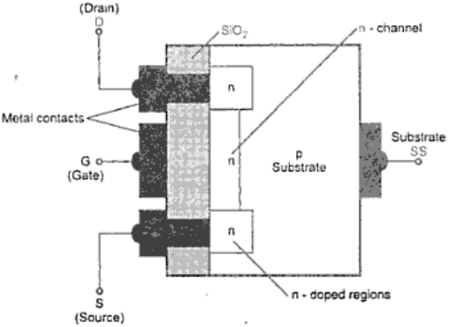


Fig. 5.35 n-channel depletion-type MOSFET

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the Fig. 5.35. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, there is no direct electrical connection between the gate terminal and the channel of a MOSFET, increasing the input impedance of the device.

5.7.1.2 Operation, Characteristics and Parameters of n-channel MOSFET

On the application of drain to source voltage, V_{DS} and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0$ V, as shown in the Fig. 5.36.

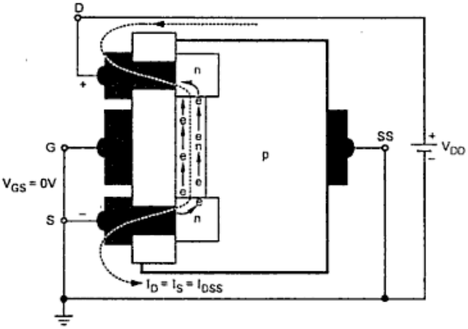

D
+
G
$V_{GS} = 0V$
S
−
n
n
p
e
SS
+
−
V_{DD}
$I_D = I_S = I_{DSS}$

Fig. 5.36 n-channel depletion-type MOSFET with V_{GS} = 0 V and an applied voltage V_{DD}

If we apply negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, and attract holes from the p type substrate. This initiates recombination of repelled electrons and attracted holes as shown in the Fig. 5.37.

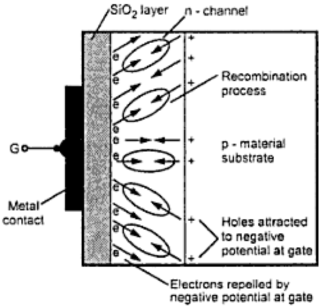

SiO_2 layer
n - channel
Recombination process
p - material substrate
Holes attracted to negative potential at gate
G
Metal contact
e
+
Electrons repelled by negative potential at gate

Fig. 5.37 Reduction in free electrons in the n-channel due to negative potential at the gate terminal

The level of recombination between electrons and holes depends on the magnitude of the negative voltage applied at the gate. This recombination reduces the number of free electrons in the n-channel for the conduction, reducing the drain current.

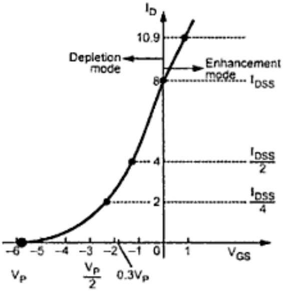


Fig. 5.38 Transfer characteristics for an n-channel depletion type MOSFET

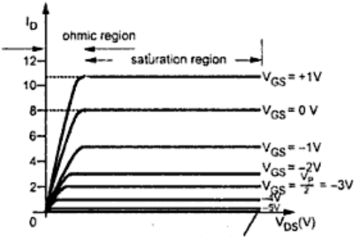


Fig. 5.39 Drain characteristics for an n-channel depletion type MOSFET

In other words we can say that, due to recombinations, n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of n-channel electrons. The level of drain current will reduce with increasing negative bias for V_{GS} as shown in the transfer characteristics of depletion type MOSFET (Fig. 5.38).

For positive values of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current and establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases as shown in the Fig. 5.38

The application of a positive gate to source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0V$. For this reason the region of positive gate voltages on the drain or transfer characteristics is referred to as enhancement region and the region between cutoff and the saturation levels of I_{DSS} referred to as depletion region. Fig. 5.39 shows drain characteristics for an n-channel depletion type MOSFET. It is similar to that of JFET. The only difference is that it has positive part of V_{GS} .

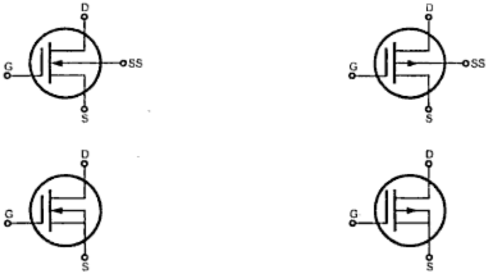
Key Points :

1. *$I_D = 0$ corresponds to $V_{GS(off)}$, $V_{GS(off)} = -V_P$.*

2. *$V_{GS} = 0$ corresponds to I_{DSS}.*

3. *Both positive and negative values of V_{GS} can be used to bias D-MOSFET.*

are given for each type of channel to reflect the fact that, in some cases it is internally shorted to source terminal.



(a) Symbols for n-channel deplection type MOSFETs

(b) Symbols for p-channel deplection type MOSFETs

Fig. 5.41

5.7.2 Enhancement MOSFET (E-MOSFET)

This type of MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the depletion MOSFET in that it has no physical channel.

5.7.2.1 Construction of n-channel E-MOSFET

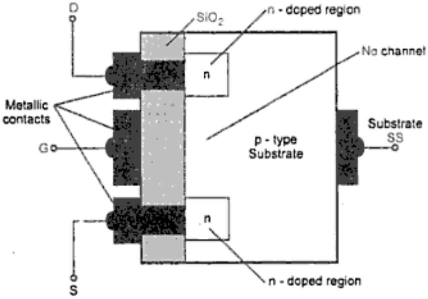


Fig. 5.42 n-channel enhancement type MOSFET

The Fig. 5.42 shows the basic construction of n channel enhancement type MOSFET.

Like, depletion type MOSFET, two highly doped n regions are diffused into a lightly doped p type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in the Fig. 5.42. But the channel between two n-regions is absent in the enhancement type MOSFET. The SiO$_2$ layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

5.7.2.2 Operation, Characteristics and Parameters of n-channel E-MOSFET

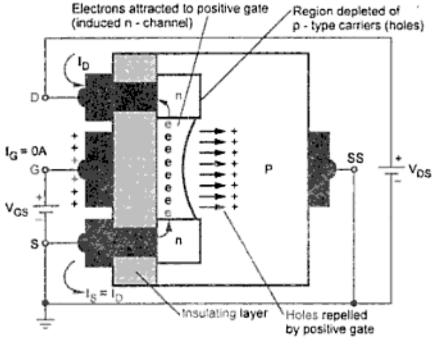

Electrons attracted to positive gate (induced n - channel)
Region depleted of p - type carriers (holes)
I_D
D
n
I_G = 0A
G
V_{GS}
S
n
e
P
SS
V_{DS}
$I_S = I_D$
Insulating layer
Holes repelled by positive gate

Fig. 5.43 Channel formation in the n-channel enhancement type MOSFET

On application of drain to source voltage V_{DS} and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows-quite different from the depletion type MOSFET and JFET. If we increase magnitude of V_{GS} in the positive direction, the concentration of electrons near the SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called threshold voltage denoted by V_T. Thus we can say that in an enhancement type n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in the Fig. 5.43. The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. For any voltage below the threshold value, there is no channel.

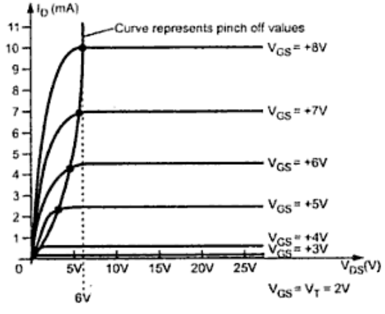


Fig. 5.44 Drain characteristics of an n-channel enhancement type MOSFET

Since the channel does not exist with V_{GS} = 0 V and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement type MOSFET.

Fig. 5.44 shows the drain characteristics of an n-channel enhancement type MOSFET. Looking at Fig.5.44 we can say that as V_{GS} increases beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The levelling off of I_D is due to a pinch-off process, is as described earlier for the JFET. Fig. 5.45 shows pinch off process for n-channel enhancement type MOSFET.

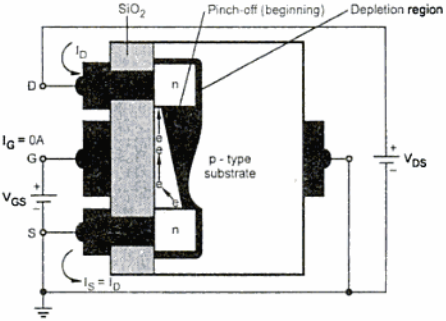


Fig. 5.45 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

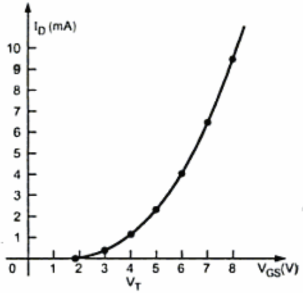


Fig. 5.46 Transfer characteristic for n-channel enhancement type MOSFET

Fig. 5.46 shows the transfer characteristic for n-channel enhancement type MOSFET. This characteristic is quite different from characteristic that we obtained for JFET and depletion type MOSFET. For an n-channel enhancement type MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow until $V_{GS} = V_T$.

For $V_{GS} > V_T$ the relationship between drain current and V_{GS} is nonlinear and it is given as

$$\boxed{I_D = K(V_{GS} - V_T)^2} \qquad \ldots (1)$$

The K term is a constant that is a function of the construction of the device. The value of K can be determined from equation,

$$\boxed{K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}} \qquad \ldots (2)$$

5.7.2.3 P-channel Enhancement Type MOSFET

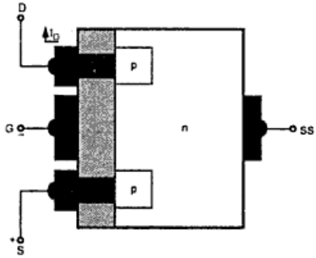


Fig. 5.47 Construction of p-channel enhancement type MOSFET

The construction of the p-channel enhancement type MOSFET is exactly opposite to that of n-channel enhancement type MOSFET. Here, the substrate is of n-type and regions are of p-type as shown in the Fig. 5.47.

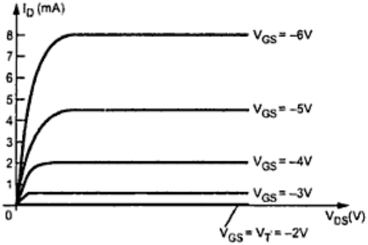


Fig. 5.48 Drain characteristics of p channel enhancement MOSFET

As shown in the Fig. 5.48 voltage polarities and current directions are reversed. The drain characteristics appear exactly as in the Fig. 5.48 but with V_{DS} with negative values, I_D in opposite direction and V_{GS} having opposite polarities as shown in the Fig. 5.48.

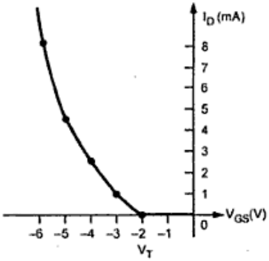
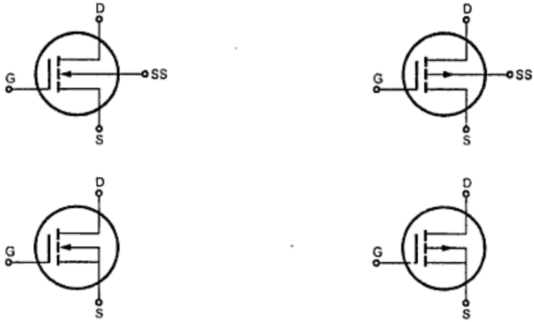


Fig. 5.49 Transfer characteristics of p-channel enhancement type MOSFET

Fig. 5.49 shows the transfer characteristics of p-channel enhancement type MOSFET. In the p-channel enhancement type MOSFET, the transfer characteristic is a mirror image about the I_D axis (y axis) of the transfer characteristics of n-channel depletion type MOSFET, since the V_{GS} is negative.

E-MOSFET symbols

Fig. 5.50 shows graphic symbols for an n and p channel enhancement type MOSFET. The dashed line between drain and source represents the fact that a channel does not exists between the two under no-bias conditions. It is the only difference between the symbols for the depletion type and enhancement type .



(a) Symbols for n-channel type MOSFETs enhancement

(b) Symbols for p-channel type MOSFETs enhancement

Fig. 5.50 Symbols

5.8 JFET Amplifiers

JFET amplifiers provide an excellent voltage gain with the added advantages of a high input impedance. Because of their high input impedance and other characteristics JFETs are often preferred over BJTs for certain types of applications.

Many of the concepts that relate to amplifiers using BJTs apply equally to FET amplifiers. There are three basic FET circuit configurations :

- Common source
- Common drain and
- Common gate

These are similar to the bipolar transistor common emitter, common collector and common base circuits, respectively. The only difference is that BJT controls a large output (collector) current by means of a relative small input (base current), whereas, FET controls an output (drain) current by means of small input (gate) voltage. It is important to note that in both the cases the output current is the controlled variable.

Field-effect transistor amplifier circuits use the voltage-controlled nature of the JFET. In the pinch-off region, I_D depends (approximately) only on V_{GS}.

Let us discuss the use of the JFET as an amplifier by considering the common-source circuit, shown in the Fig. 5.51.

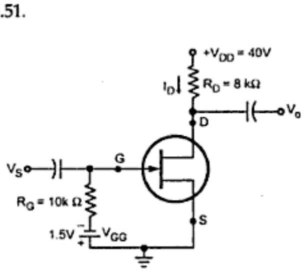


Fig. 5.51 Common source circuit

The voltage V_{GG} provides the necessary reverse-bias between gate and source of the JFET. The signal to be amplified is V_s. The V-I characteristics of the JFET is as shown in Fig. 5.52.

On the output characteristics, a load line corresponding to $V_{DD} = 40$ V and $R_D = 8\ k\Omega$ is constructed. The transistor is biased at point Q and results in $V_{DSQ} = 20$ V and $I_{DQ} = 2.70$ mA.

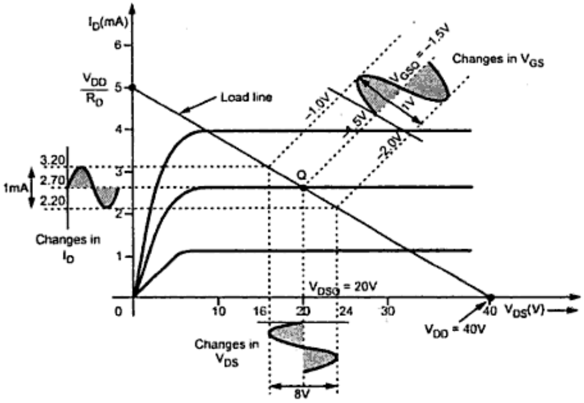


Fig. 5.52 V-I characteristics of JFET

The another important parameter of JFET is drain resistance r_d . It is given by

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{constant}} \qquad \text{... (2)}$$

It determines the output impedance Z_0 of the JFET amplifier.

JFET Low Frequency ac Equivalent Circuit

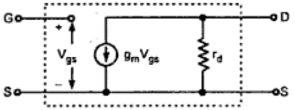


Fig. 5.53 JFET low frequency ac equivalent circuit for n-channel JFET

Fig. 5.53 shows the small signal low frequency ac equivalent circuit for n-channel JFET. The relation of I_d by V_{gs} is included as a current source g_mV_{gs} connected from drain to source. The input impedance is represented by the open circuit at its input terminals, since gate current I_G is zero. The output impedance is represented by r_d from drain to source.

Key Point: *The lower case subscripts represent ac levels.*

Approximate ac Equivalent Circuit

When the value of external drain resistance R_D is very small as compared to the value of output impedance represented by r_d, it is possible to replace r_d by open circuit. This gives us approximate ac equivalent circuit of JFET amplifier, as shown in Fig. 5.54.

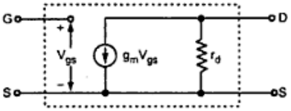


Fig. 5.54 Approximate ac equivalent circuit for JFET amplifier

5.8.2 Common Source (CS) Amplifier

In common source amplifier circuit input is applied between gate and source and output is taken from drain and source. In the following sections we see the low frequency equivalent circuits for common source configuration with different biasing techniques.

5.8.2.1 JFET with Fixed Bias

Fig. 5.54 shows common source amplifier with fixed bias. The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for the ac analysis.

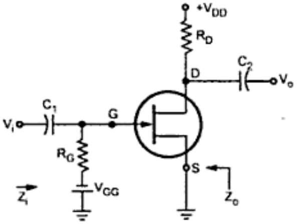


Fig. 5.55 Common source JFET amplifier with fixed bias

Fig. 5.55 shows the low frequency equivalent model for the common source amplifier circuit with fixed bias. It is drawn by replacing :

- All capacitors and dc supply voltages with short circuits and
- JFET with its low frequency equivalent circuit.

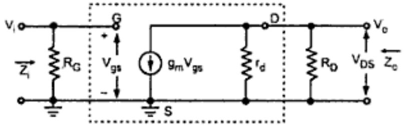


Fig. 5.56 AC equivalent model for the common source amplifier circuit with fixed bias

Now, we see the input impedance output impedance and voltage gain of the above model.

Input impedance Z_i :

Looking into Fig. 5.55 we can say that,

$$\boxed{Z_i = R_G} \quad \dots (3)$$

Output impedance Z_o :

The output impedance Z_o is the impedance measured looking from the output side with input voltage (V_i) equal to 0. As $V_i = 0$,

$$V_{gs} = 0 \text{ and hence } g_m V_{gs} = 0.$$

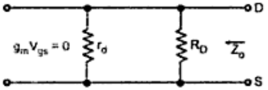


Fig. 5.57

The $g_m V_{gs} = 0$ allows current source to be replaced by an open circuit, as shown in the Fig. 5.57 Therefore the output impedance is

$$\boxed{Z_o = R_D \,||\, r_d} \quad \dots (4)$$

If the resistance r_d is sufficiently large compared to R_D, then we say that the output impedance is approximately equal to R_D.

$$\boxed{Z_o \approx R_D} \quad \because r_d >> R_D \qquad \dots (5)$$

Voltage Gain A_v :

The voltage gain $A_v = \dfrac{V_{ds}}{V_{gs}} = \dfrac{V_o}{V_i}$

Looking at Fig. 5.55 we can write

$$V_o = -g_m V_{gs} (r_d \| R_D) \qquad \dots (6)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i (r_d \| R_D) \qquad \dots (7)$$

$$\therefore \quad \boxed{A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)} \qquad \dots (8)$$

and if $r_d >> R_D$,

$$\therefore \quad \boxed{A_v \approx -g_m R_D} \qquad \dots (9)$$

Key Point: *The negative sign in the equation for A_v clearly indicates there is a phase shift of 180° between input and output voltages.*

Table 5.1 summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d >> R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m (R_D \| r_d)$	$-g_m R_D$

Table 5.1

Example 5.11 : *For the circuit shown in Fig. 5.58. Determine i) Input impedance ii) Output impedance and iii) Voltage gain.*

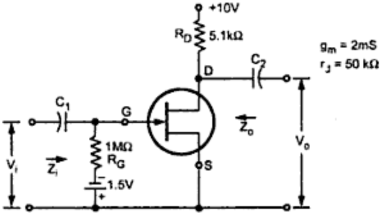


Fig. 5.58

iv) Z_o : We have,

$$Z_o = r_d \,||\, R_D = 50\text{ K} \,||\, 5.1\text{ K} = \mathbf{4628\ \Omega}$$

v) A_v : We have,

$$A_v = \frac{V_o}{V_i} = -g_m\,(r_d \,||\, R_D) = -1.5\text{ mS }(50\text{ K}||5.1\text{ K}) = -1.5\text{ mS}(4628)$$

$$= \mathbf{-\,6.942}$$

5.8.2.2 JFET with Self Bias (Bypassed R_s)

Fig. 5.60 shows common source amplifier with self bias.

The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for the low frequency analysis. Bypass capacitor C_s also acts as a short circuit for the low frequency analysis.

Fig. 5.61 shows the low frequency equivalent model for the common source amplifier circuit with self bias. It is drawn by replacing

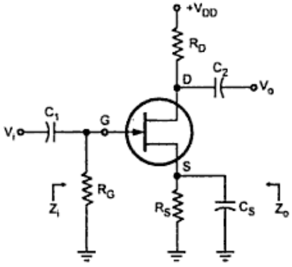


Fig. 5.60 Common source JFET amplifier with self bias

- All capacitors and dc supply V_{DD} with short circuits and,
- JFET with its low frequency equivalent circuit.

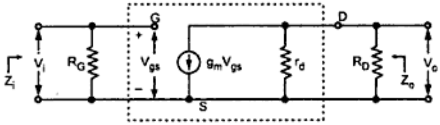


Fig. 5.61 ac equivalent model for the common source amplifier circuit with self bias

Since the resulting low frequency equivalent circuit is same as ac equivalent circuit in Fig. 5.56, the equation for Z_i, Z_o and A_v will also be same.

i) Input impedance Z_i : $\boxed{Z_i = R_G}$ ... (10)

ii) Output impedance Z_o : $\boxed{Z_o = r_d \| R_D}$ ... (11)

if $r_d \gg R_D$ $\boxed{Z_o \approx R_D}$ ... (12)

iii) Voltage gain A_v : $\boxed{A_v = -g_m (r_d \| R_D)}$ ... (13)

If $r_d \gg R_D$ $\boxed{A_v = -g_m R_D}$ ... (14)

The negative sign in the equation (13) and (14) again indicates there is a phase shift of 180° between input and output voltages.

5.8.2.3 JFET with Self Bias (Unbypassed R_S)

Fig. 5.62 shows common source amplifier with self biasing having unbypassed R_S.

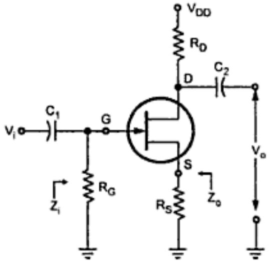


Fig. 5.62 Common source JFET amplifier with self bias having unbypassed R_S

Now R_S will be the part of low frequency equivalent model as shown in the Fig. 5.63.

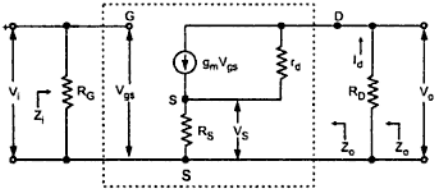


Fig. 5.63 Low frequency equivalent model for the common source amplifier circuit with self bias having unbypassed R_S

Voltage Gain A_v :

It is given by,

$$A_v = \frac{V_o}{V_i} \qquad \dots (25)$$

We know that,

$$V_o = -I_d R_D \qquad \dots (26)$$

Applying KVL to the output circuit as shown in Fig. 5.64 we have,

$$(I_d - g_m V_{gs}) r_d + I_d R_S + I_d R_D = 0 \qquad \dots (27)$$

We know that, $V_{gs} = V_{in} - I_d R_S$

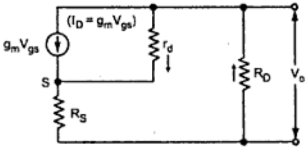


Fig. 5.64

Substituting value of V_{gs} in equation (27) we get,

$$[I_d - g_m (V_i - I_d R_S)] r_d + I_d R_S + I_d R_D = 0 \qquad \dots (28)$$

$$\therefore I_d r_d - g_m V_i r_d + g_m I_d R_S r_d + I_d R_S + I_d R_D = 0 \qquad \dots (29)$$

$$\therefore \quad I_d (r_d + R_S + R_D + g_m R_S r_d) = g_m V_i r_d \qquad \dots (30)$$

$$\therefore \quad I_d = \frac{g_m V_i r_d}{r_d + R_S + R_D + g_m R_S r_d} \qquad \dots (31)$$

From equation (26) we know that,

$$V_o = -I_d R_D \qquad \dots (32)$$

Substituting value of I_d from equation (31) we get,

$$V_o = \frac{-g_m V_i r_d R_D}{r_d + R_S + R_D + g_m R_S r_d} \qquad \dots (33)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m r_d R_D}{r_d + R_S + R_D + g_m R_S r_d} \qquad \dots (34)$$

Dividing numerator and denominator by r_d we get,

$$\therefore \qquad A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_S + R_D}{r_d}} \qquad \text{... (35)}$$

If $r_d >> R_S + R_D$

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}} \qquad \text{... (36)}$$

Key Point: *With unbypassed* R_S *voltage gain reduces.*

Table 5.2 summarizes performance of common source amplifier with self bias.

Parameter	**Bypassed R_S**		**Unbypassed R_S**	
	Exact	$r_d >> R_D$	Exact	$r_d >> R_D$
Z_i	R_G	R_G	R_G	R_G
Z_o	$R_D \parallel r_d$	R_D	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S (\mu + 1)] \parallel R_D$	$[r_d + R_S (g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S (\mu + 1)] \parallel R_D$
A_v	$-g_m(R_D \parallel r_d)$	$-g_m R_D$	$\dfrac{-g_m R_D}{1 + g_m R_S + \dfrac{R_S + R_D}{r_d}}$	$\dfrac{-g_m R_D}{1 + g_m R_S}$

Table 5.2

➡ **Example 5.13 :** *For common source amplifier as shown in Fig. 5.65 operating point is defined by* $V_{GSQ} = -2.5$ V, $V_P = -6$ V *and* $I_{dQ} = 2.5$ mA *with* $I_{dSS} = 8$ mA. *Calculate* g_m, r_d, Z_i, Z_o *and voltage gain* A_v.

Solution :

i) g_m : We have,

$$g_{mo} = \frac{2\, I_{DSS}}{|V_P|} = \frac{2(8 \times 10^{-3})}{6} = \mathbf{2.67\ mS}$$

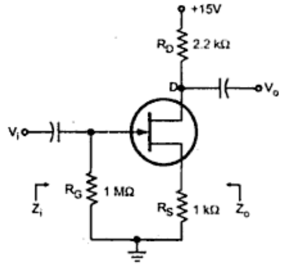


Fig. 5.65

$$g_m = g_{mo}\left(1-\frac{V_{GSQ}}{V_P}\right) = 2.67\text{ mS}\left(1-\frac{(-2.5\text{V})}{(-6\text{V})}\right) = \mathbf{1.58\text{ mS}}$$

ii) r_d :

$$r_d = \frac{1}{Y_{os}} = \frac{1}{20\text{mS}} = \mathbf{50\text{ k}\Omega}$$

iii) Z_i : From equation (13) we have,

$$Z_i = R_G = \mathbf{1\text{ M}\Omega}$$

iv) Z_o : We have,

$$Z_o = [\,r_d + R_S\,(g_m\,r_d + 1)\,]\,||\,R_D$$

$$= [50\text{K} + 1\text{K}\,(1.58\text{ mS}\times 50\text{ K} + 1)]\,||\,2.2\text{ K} = \mathbf{2163.4\ \Omega}$$

v) A_v : We have,

$$A_v = \frac{-g_m\,R_D}{1+g_m\,R_S+\dfrac{R_s+R_D}{r_d}} = \frac{-1.58\text{ mS}\times 2.2\text{ K}}{1+1.58\text{ m S}\times\ 1\text{K}+\dfrac{1\text{ K}+2.2\text{ K}}{50\text{ K}}}$$

$$= \frac{-3.476}{2.644} = \mathbf{-1.315}$$

5.8.2.4 JFET with Voltage Divider Bias (Bypassed R_S)

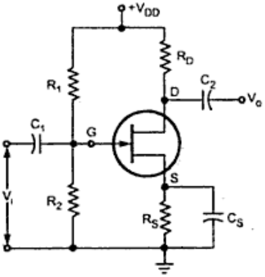


Fig. 5.66 Common source JFET amplifier with voltage divider bias

Fig. 5.66 shows common source amplifier with voltage divider biasing.

The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for the low frequency analysis. Bypass capacitor C_S also acts as short circuit for the low frequency analysis.

Fig. 5.66 shows the low frequency equivalent model for the common source amplifier circuit with voltage divider bias. It is drawn by replacing :

- All capacitors and dc supply V_{DD} with short circuits and,
- JFET with its low frequency equivalent circuit

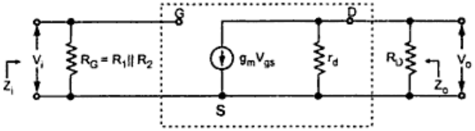


Fig. 5.67 Low frequency equivalent model for the common source amplifier circuit with voltage divider bias

Since the resulting low frequency equivalent circuit is the same as ac equivalent circuit in Fig. 5.61, the equation for Z_i , Z_o and A_v will be the same.

It is important to note that, here,

$$R_G = R_1 || R_2 .$$

$$\boxed{Z_i = R_G}$$

$$= R_1 || R_2 \quad \text{... (37)}$$

$$\boxed{Z_o = r_d || R_D} \quad \text{... (38)}$$

if $r_d >> R_D$

$$\boxed{Z_o \approx R_D} \quad \text{... (39)}$$

$$Z_i = R_G = R_1 \parallel R_2 \qquad \text{... (42)}$$

$$Z'_o = r_d + g_m R_S r_d + R_S \qquad \text{... (43)}$$

or $$Z'_o = r_d + R_S (\mu + 1) \qquad \text{... (44)}$$

$$Z_o = [r_d + g_m R_S r_d + R_S] \parallel R_D \qquad \text{... (45)}$$

or $$Z_o = [r_d + R_S (\mu + 1)] \parallel R_D \qquad \text{... (46)}$$

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_S + R_D}{r_d}} \qquad \text{... (47)}$$

or $$A_v = \frac{-g_m R_D}{1 + g_m R_S} \qquad \text{... (48)}$$

➡ Example 5.14 : *For the amplifier shown in Fig. 5.70, calculate :*

i) $A_v = \dfrac{V_o}{V_i}$ *ii)* Z_i *iii)* Z_o *iv)* Z'_o.

Assume for FET $g_m = 2$ mA/V, $r_d = 10$ kΩ.

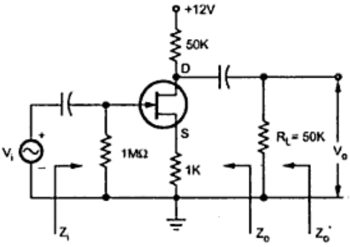


Fig. 5.70

Solution : The equivalent circuit for given circuit can be drawn as follows

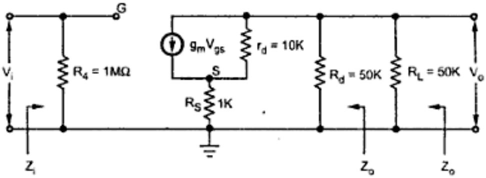


Fig. 5.71

i)
$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}}$$

where $R_D = 50\ K \,||\, 50\ K = 25\ K$

$$= \frac{-2\times 25}{1 + 2\times 1 + \frac{1+25}{10}} = -\mathbf{8.928}$$

ii) $Z_i = R_G = \mathbf{1\ M\Omega}$

iii) $Z_o = [r_d + g_m R_s r_d + R_S] \,||\, R_D = [10\,K + 2ms \times 1\times 10^3 \times 10\times 10^3 + 1\times 10^3] \,||\, 50\ K$

$= \mathbf{19.135\ k\Omega}$

iv) $Z'_o = Z_o \,||\, R_L = 19.135\ K \,||\, 50\ K = \mathbf{13.838\ k\Omega}$

Table 5.3 summarizes the performance of common source amplifier with voltage divider bias.

	Bypassed R_S		**Unbypassed R_S**	
	Exact	**$r_d >> R_D$**	**Exact**	**$r_d >> R_D$**
Z_i	$R_1 \| R_2$	$R_1 \| R_2$	$R_1 \| R_2$	$R_1 \| R_2$
Z_o	$r_d \| R_D$	R_D	$[r_d + g_mR_S r_d + R_S] \| R_D$ or $[r_d + R_S (\mu + 1)] \| R_D$	$[r_d + g_mR_S r_d + R_S)] \| R_D$ or $[r_d + R_S (\mu + 1)] \| R_D$
A_v	$-g_m(r_d \| R_D)$	$-g_m R_D$	$\frac{-g_m R_D}{1+g_m R_S + \frac{R_S + R_D}{r_d}}$	$\frac{-g_m R_D}{1 + g_m R_S}$

Table 5.3

5.8.3 Common Drain (CD) Amplifier

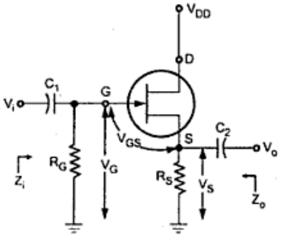


Fig. 5.72 Common drain amplifier circuit

In common drain amplifier circuit input is applied between gate and source and output is taken between source and drain.

Fig. 5.72 shows common drain configuration.

It shows that the output is taken from source and when the dc supply is replaced by its short circuit equivalent the drain is grounded and thus common between input and output.

In the common drain circuit the source voltage V_S is given as,

$$V_S = V_G + V_{GS}$$

When a signal is applied to the JFET gate via C_1, V_G varies with the signal. As V_{GS} is fairly constant and $V_S = V_G + V_{GS}$, V_S varies with V_i. For example, if V_i increases by 0.25 V, V_S also approximately increases by 0.25 V. Because the output voltage at the source (V_S) follows changes in the signal voltage applied to the gate, this circuit is also called as source follower.

Fig. 5.73 shows the low frequency equivalent model for the common drain amplifier circuit shown in Fig. 5.72.

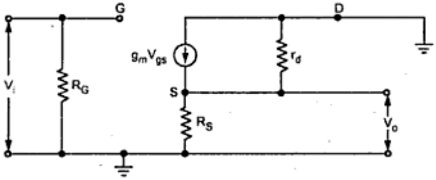


Fig. 5.73 Simplified low frequency equivalent model for common drain circuit

This low frequency equivalent circuit can be simplified as shown in the Fig. 5.73.

Input Impedance Z_i :

Looking at Fig. 5.74, Z_i can written as,

$$\boxed{Z_i = R_G} \quad \text{... (49)}$$

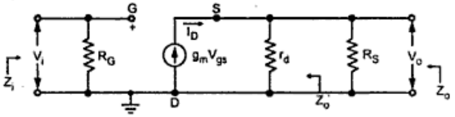


Fig. 5.74 Simplified low frequency equivalent model for common drain circuit

Output Impedance Z_o :

It is given by,

$$Z_o = Z_o' \| R_S \quad \text{... (50)}$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i=0} \quad \text{... (51)}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0 \quad \text{... (52)}$$

As $$V_i = 0,$$

$$V_{gs} = V_o \quad \text{... (53)}$$

Looking at Fig. 5.74 we can write that,

$$g_m V_{gs} = I_d \quad \text{... (54)}$$

Substituting value of V_{gs} from equation (53) in equation we get,

$$g_m V_o = I_d \quad \text{... (55)}$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m} \quad \text{... (56)}$$

$$\therefore \quad \boxed{Z_o = \frac{1}{g_m} \| R_S} \quad \text{... (57)}$$

Voltage Gain A_v :

It is given by,

$$A_v = \frac{V_o}{V_i} \quad \text{... (58)}$$

Looking at Fig. 5.74 we can write that,

$$V_o = -I_d (r_d \| R_S) \quad \text{... (59)}$$

and $$I_d = g_m V_{gs} \quad \text{... (60)}$$

$$\therefore \quad V_o = -g_m V_{gs} (r_d \| R_S) \quad \text{... (61)}$$

Again from equation (52) we have,

$$V_i = -V_{gs} + V_o$$

$$= -V_{gs} + [-g_m V_{gs} (r_d \| R_S)] \qquad \dots (62)$$

Substituting values of V_o and V_i from equations (61) and (62) respectively in above equation (58) we get,

$$A_v = \frac{-g_m V_{gs} (r_d \| R_S)}{-V_{gs} (1 + g_m (r_d \| R_S))} = \frac{g_m (r_d \| R_S)}{1 + g_m (r_d \| R_S)} \qquad \dots (63)$$

if $r_d >> R_S$

$$\boxed{A_v = \frac{g_m R_S}{1 + g_m R_S}} \qquad \dots (64)$$

if $g_m R_S >> 1$

$$A_v \approx 1, \text{ but it is always less than one.} \qquad \dots (65)$$

Key Point :

1 . *We observe that the common drain circuit does not provide voltage gain.*

2. *The positive sign in equation (64) also indicates that there is no phase shift between input and output voltages.*

Table 5.4 summarizes the performance of common drain amplifier.

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \| R_S$	$\frac{1}{g_m} \| R_S$
A_v	$\frac{g_m (r_d \| R_S)}{1 + g_m (r_d \| R_S)}$	$\frac{g_m R_S}{1 + g_m R_S}$

Table 5.4

Example 5.15 : *For common drain amplifier as shown in Fig. 5.75,* g_m = 2.5 mS, $r_d = 25\ k\Omega$. *Calculate* Z_i , Z_o *and* A_v .

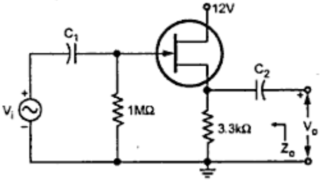


Fig. 5.75

$$V_i + I_d r_d + g_m r_d V_i + I_d R_D = 0$$

$$\therefore \quad V_i + g_m r_d V_i = -I_d (r_d + R_D)$$

$$\therefore \quad V_i = \frac{-I_d (r_d + R_D)}{1 + g_m r_d} \qquad \text{... (79)}$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-I_d + R_D}{\dfrac{-I_d (r_d + R_D)}{1 + g_m r_d}}$$

$$\therefore \quad \boxed{A_v = \frac{R_D (1 + g_m r_d)}{r_d + R_D}} \qquad \text{... (80)}$$

If $r_d >> R_D$ and $g_m r_d >> 1$

$$\boxed{A_v = \frac{R_D (g_m r_d)}{r_d} = R_D g_m} \qquad \text{... (81)}$$

Key Point : *From equation (81) we observe that there is no phase shift between input and output in common gate amplifier.*

Table 5.5 summarizes the performance of common gate amplifier.

	Exact	$r_d >> R_D$
Z_i	$R_s \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$	$R_s \parallel \frac{1}{g_m}$
Z_o	$r_d \parallel R_D$	R_D
A_v	$\frac{R_D (1 + g_m r_d)}{r_d + R_D}$	$g_m R_D$

Table 5.5

Example 5.16 : *For common gate amplifier as shown in the Fig. 5.80, g_m = 2.8 mS, $r_d = 50\,k\Omega$. Calculate Z_i, Z_o and A_v.*

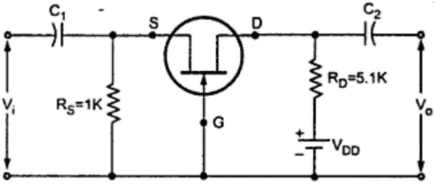


Fig. 5.80

Solution :

i) Z_i : We have,

$$Z_i = R_S \parallel \frac{r_d + R_D}{1+g_m\, r_d}$$

$$= 1\text{K} \parallel \frac{50\,\text{K}+5.1\,\text{K}}{1+2.8\text{mS}\times 50\,\text{K}} = 1\text{K} \parallel 390.8 = \mathbf{281\ \Omega}$$

ii) Z_o : We have,

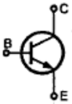
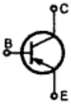
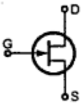
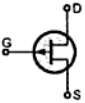
$$Z_o = r_d \parallel R_D = 50\ \text{K} \parallel 5.1\ \text{K} = \mathbf{4.628\ K}$$

iii) A_v : We have

$$A_v = \frac{R_D(1+g_m\, r_d)}{r_d + R_D} = \frac{5.1\,\text{K}(1+2.8\,\text{mS}\times 50\,\text{K})}{50\,\text{K}+5.1\,\text{K}} = \mathbf{13.05}$$

5.9 Comparison between BJT, JFET and MOSFET

5.9.1 Comparison of BJT and FET

Sr. No.	Parameter	BJT	FET
1	**Control element**	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	**Device type**	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3	**Types**	npn and pnp	n-channel and p-channel.
4	**Symbols**	 npn  pnp	 n-channel  p-channel
5	**Configurations**	CE, CB, CC	CS, CG, CD
6 .	**Input resistance**	Less compare to JFET.	High compare to BJT.

7	**Size**	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	**Sensitivity**	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	**Thermal stability**	Less	More
10	**Thermal runaway**	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temeperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	**Relation between input and output**	Linear	Non-linear
12	**Ratio of o/p to i/p**	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13	**Thermal noise**	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	**Gain bandwidth product**	High	Low

5.9.2 Comparison of JFET and MOSFET

Sr. No.	Parameter	JFET	MOSFET
1	**Types**	a) n-channel b) p-channel	A) n-channel depletion type MOSFET B) p-channel depletion type MOSFET C) n-channel enhancement type MOSFET D) p-channel enhancement type MOSFET

4	**Current flow**	Drain current flows on application of drain to source voltage, at $V_{GS} = 0$.	Practically no current flows on application of drain to source, at $V_{GS} = 0$. Current flows only when V_{GS} is above threshold level.

Review Questions

1. *Why FET is called a voltage operated device ?*
2. *Why FET is called unipolar device ?*
3. *List the important features of FET.*
4. *Explain how FET works as voltage variable resistor ?*

5 *Give the classification of FETs and their applications areas.*

6. *State true or false with reasons :*
    a) In JFET, the p-n junction between gate and source is always kept in reverse biased condition.
    b) FET has very high input impedance.
    c) Gate current in FET is always neglected.
7. *Explain construction of n channel JFET with neat diagram and symbol.*
8. *With the help of neat diagram, explain the operation of an n-channel JFET. Show the internal depletion regions and explain their shape.*
9. *Draw the structure of an n-channel JFET and explain its principle of operation. Why is the name field effect used for the device ? Show the circuit symbol of JFET.*
10. *Draw the static characteristics curves of an n-channel JFET and explain the different portions of the characteristics. Define the pinch-off voltage and indicate its location on drain characteristics.*
11. *What do you understand by 'pinch off voltages' and 'cutoff voltages' ?*
12. *Draw a circuit for obtaining drain and transfer characteristics for an n-channel JFET, and explain how to get values to plot the said characteristics.*
13. *Sketch a typical drain characteristic for an n-channel JFET. Explain the shape of the characteristic and identify the regions.*
14. *Sketch a typical transfer characteristic for an n-channel JFET and show how the transconductance g_m can be derived from the transfer characteristic.*
15. *Define R_d, g_m and μ of JFET.*
16. *State true or false with reasons : the relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear.*
17. *Explain how MOSFET differs from JFET.*
18. *With the help of neat diagrams explain the operation and drain characteristics of n-channel depletion type MOSFET. Explain clearly the mechanism of "Pinch-off Condition". Sketch the drain characteristics and define r_d.*
19. *Explain the constructional features of a depletion mode MOSFET and explain its basic operation.*

20. *Draw the drain charcteristics of depletion type MOSFET. Explain clearly different operating regions in characteristics with proper reasoning.*
21. *With the help of neat diagram explain the operation of an n-channel enhancement type MOSFET.*
22. *What is the significance of the threshold voltage V_T in (i) enhancement mode (ii) depletion mode MOSFETs.*
23. *For a MOSFET of V_{GS} varies from negative to positive voltage draw the transfer characteristics and mention modes of operation.*
24. *Sketch the drain characteristics of MOSFET for different values of V_{GS} and mark different region of operation.*
25. *Draw and explain the drain characteristics of n-channel enhancement type MOSFET.*
26. *Sketch the graphic symbols for : n-channel JFET, p-channel JFET, n-channel enhancement type MOSFET, p-channel enhancement type MOSFET, n-channel depletion type MOSFET and p-channel depletion type MOSFET.*
27. *Give the comparison between BJT and JFET.*
28. *Give the comparison between JFET and MOSFET.*
29. *Compare D-MOSFET and E-MOSFET.*

□□□

6

Operational Amplifiers

6.1 Introduction

The operational amplifier, most commonly referred as '**op-amp**' was introduced in 1940s. The first operational amplifier was designed in 1948 using vacuum tubes. In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc. Due to its use in performing mathematical operations it has been given a name operational amplifier. Due to the use of vacuum tubes, the early op-amps were bulky, power consuming and expensive.

Robert J. Widlar at Fairchild brought out the popular 741 integrated circuit (IC) op-amp between 1964 to 1968. The IC version of op-amp uses BJTs and FETs which are fabricated along with the other supporting components, on a single semiconductor chip or wafer which is of a pinhead size. With the help of IC op-amp, the circuit design becomes very simple. The variety of useful circuits can be built without the necessity of knowing about the complex internal circuitry. Moreover, IC op-amps are inexpensive, take up less space and consume less power. The IC op-amp has become an integral part of almost every electronic circuit which uses linear integrated circuit. The modern linear IC op-amp works at **lower voltages**. It is so **low in cost** that millions are now in use, annually. Because of their **low cost**, **small size**, **versatility**, **flexibility**, and **dependability**, op-amps are used in the fields of process control, communications, computers, power and signal sources, displays and measuring systems. The op-amp is basically an excellent high gain d.c. amplifier.

This chapter explains the characteristics of ideal and practical operational amplifier and some of its widely used applications.

6.2 Op-Amp Symbol and Terminals

The symbol for an op-amp along with its various terminals, is shown in the Fig. 6.1.

The op-amp is indicated basically by a triangle which points in the direction of the signal flow.

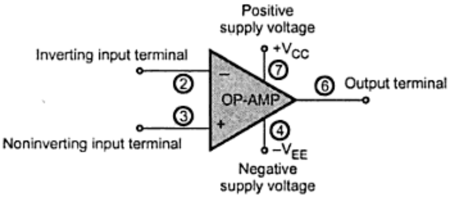
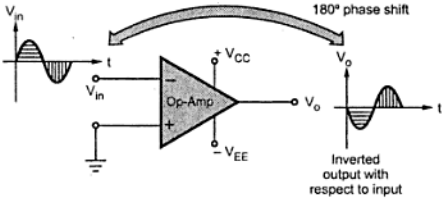

Positive
supply voltage
+V_{CC}
⑦
Inverting input terminal
②
③
Noninverting input terminal
–
OP-AMP
+
⑥ Output terminal
④
–V_{EE}
Negative
supply voltage

Fig. 6.1 Op-amp symbol

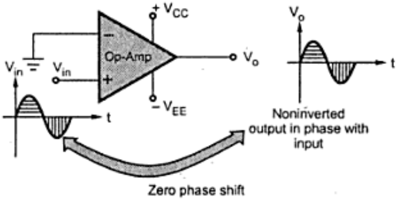
All the op-amps have atleast following five terminals :

i. The positive supply voltage terminal V_{CC} or + V.
ii. The negative supply voltage terminal – V_{EE} or – V.
iii. The output terminal.
iv. The inverting input terminal, marked as negative.
v. The noninverting input terminal, marked as positive.

The input at inverting input terminal results in opposite polarity (antiphase) output. While the input at noninverting input terminal results in the same polarity (phase) output. This is shown in the Fig. 6.2 (a) and (b). The input and output are in antiphase means


V_{in}
180° phase shift
t
+ V_{CC}
V_o
V_{in}
Op-Amp
V_o
t
– V_{EE}
Inverted
output with
respect to input

(a) Input applied to inverting terminal


+ V_{CC}
V_o
Op-Amp
V_o
t
V_{in}
V_{in}
t
– V_{EE}
Noninverted
output in phase with
input
Zero phase shift

(b) Input applied to noninverting terminal

Fig. 6.2

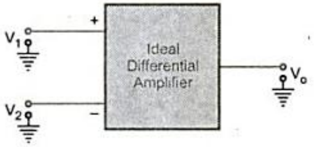


Fig. 6.4 Ideal differential amplifier

V_1 and V_2 are the two input signals while V_0 is the single ended output. Each signal is measured with respect to the ground.

In an ideal differential amplifier, the output voltage V_o is proportional to the difference between the two input signals. Hence we can write,

$$V_o \propto (V_1 - V_2) \qquad \text{... (1)}$$

6.3.2 Differential Gain A_d

From the equation (1) we can write,

$$V_o = A_d (V_1 - V_2)$$

where A_d is the constant of proportionality. The A_d is the gain with which differential amplifier amplifies the difference between two input signals. Hence it is called **differential gain** of the differential amplifier.

Thus, A_d = Differential gain

The difference between the two inputs $(V_1 - V_2)$ is generally called **difference voltage** and denoted as V_d.

$$\therefore \quad \boxed{V_o = A_d V_d}$$

Hence the differential gain can be expressed as,

$$\boxed{A_d = \frac{V_o}{V_d}}$$

Generally the differential gain is expressed in its decibel (dB) value as,

$$\boxed{A_d = 20 \operatorname{Log}_{10} (A_d) \text{ in dB}}$$

6.3.3 Common Mode Gain A_c

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. $V_1 = V_2$ then ideally the output voltage $V_o = (V_1 - V_2)A_d$, must be zero.

But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs. Such an average level of the two input signals is called **common mode signal** denoted as V_c.

$$\therefore \quad \boxed{V_c = \frac{V_1 + V_2}{2}}$$

Many a times, CMRR is also expressed in dB, as

$$\therefore \quad \boxed{\text{CMRR in dB} = 20 \log \left|\frac{A_d}{A_c}\right| \ \text{dB}}$$

Example 6.1 : *Determine the output voltage of a differential amplifier for the input voltages of 300 μV and 240 μV. The differential gain of the amplifier is 5000 and the value of the CMRR is i) 100 and ii) 10^5.*

Solution : The differential amplifier is represented as shown in the Fig. 6.5.

i) CMRR = 100

$$V_d = V_1 - V_2 = 300 - 240$$
$$= 60 \ \mu V$$

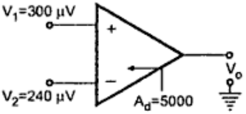


Fig. 6.5

$$V_c = \frac{V_1 + V_2}{2} = \frac{300+240}{2} = 270 \ \mu V$$

$$\text{CMRR} = \frac{A_d}{A_c}$$

$$\therefore \quad 100 = \frac{5000}{A_c}$$

$$\therefore \quad A_c = 50$$

$$\therefore \quad V_o = A_d \ V_d + A_c \ V_c = 5000 \times 60 + 50 \times 270$$
$$= 313500 \ \mu V = \mathbf{313.5 \ mV}$$

ii) CMRR = 10^5

$$\therefore \quad A_c = \frac{A_d}{\text{CMRR}} = \frac{5000}{10^5} = 0.05$$

$$\therefore \quad V_o = A_d V_d + A_c V_c = 5000 \times 60 + 0.05 \times 270$$
$$= 300013.5 \ \mu V = \mathbf{300.0135 \ mV}$$

Ideally A_c must be zero and output should be only $A_d \ V_d$ which is $5000 \times 60 \times 10^{-6}$ i.e. 300 mV. It can be seen that higher the value of CMRR, the output is almost proportional

e) Infinite bandwidth :

The range of frequency over which the amplifier performance is satisfactory is called its **bandwidth**. The bandwidth of an ideal op-amp is infinite. This means the operating frequency range is from 0 to ∞. This ensures that the gain of the op-amp will be constant over the frequency range from d.c. (zero frequency) to infinite frequency. So op-amp can amplify d.c. as well as a.c. signals.

f) Infinite CMRR : ($\rho = \infty$)

The ratio of differential gain and common mode gain is defined as CMRR. Thus infinite CMRR of an ideal op-amp ensures zero common mode gain. Due to this common mode noise output voltage is zero for an ideal op-amp.

g) Infinite slew rate : ($S = \infty$)

This ensures that the changes in the output voltage occur simultaneously with the changes in the input voltage.

The slew rate is important parameter of op-amp. When the input voltage applied is step type which changes instantaneously then the output also must change rapidly as input changes. If output does not change with the same rate as input then there occurs distortion in the output. Such a distortion is not desirable. **Infinite slew rate indicates that output changes simultaneously with the changes in the input voltage.**

The parameter slew rate is actually defined as the maximum rate of change of output voltage with time and expressed in V/μs.

$$\boxed{\text{Slew rate} = S = \left.\frac{dV_o}{dt}\right|_{\text{maximum}}}$$

Its ideal value is infinite for the op-amp.

h) No effect of temperature :

The characteristics of op-amp do not change with temperature.

i) Power Supply Rejection Ratio : (PSRR = 0)

The power supply rejection ratio is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called **power supply sensitivity.**

So if V_{EE} is constant and due to change in V_{CC}, there is change in input offset voltage then PSRR is expressed as,

$$\boxed{\text{PSRR} = \left.\frac{\Delta V_{ios}}{\Delta V_{CC}}\right|_{V_{EE}\ \text{Constant}}}$$

For a fixed V_{CC}, if there is change in V_{EE} causing change in input offset voltage then,

$$\boxed{\text{PSRR} = \left.\frac{\Delta V_{ios}}{\Delta V_{EE}}\right|_{V_{EE}\ \text{Constant}}}$$

It is expressed in mV/V or μV/V and its ideal value is zero.

These ideal characteristics of op-amp are summarized in the Table 6.1.

Characteristics	Symbol	Values
Open loop voltage gain	A_{OL}	∞
Input impedance	R_{in}	∞
Output impedance	R_o	0
Offset voltage	V_{oo}	0
Bandwidth	B.W.	∞
C.M.R.R	ρ	∞
Slew rate	S	∞
Power supply rejection ratio	PSRR	0

Table 6.1 Ideal op-amp characteristics

6.5 Saturable Property of Op-Amp

The open loop gain of op-amp is very high. While every op-amp has a property that its output can swing between two levels decided by the supply voltages i.e. $+V_{CC}$ and $-V_{EE}$. Thus if output tries to rise more than $+V_{CC}$ or less than $-V_{EE}$ then it gets clipped and gets saturated at the levels almost equal to $+V_{CC}$ and $-V_{EE}$, on positive and negative side respectively.

Key Point : *The property by which op-amp output saturates at the two saturation levels* $(\pm V_{sat})$*, decided by the supply voltages, is called saturable property of an op-amp.*

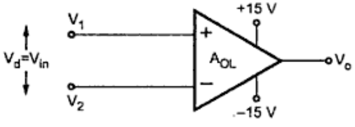


Fig. 6.7

Consider an op-amp shown in the Fig. 6.7. The value of A_{OL} is very high. Let it be 10^5. And supply voltages are ±15 V.

$$\text{Now } V_o = V_d \times A_{OL}$$

$$\therefore \quad V_d = \frac{V_o}{A_{OL}}$$

In such a case, when V_1 becomes more than or less than V_{ref} by the difference of the order of few μV, due to high A_{OL} the output is either $+V_{sat}$ or $-V_{sat}$ i.e. saturated.

The V_1 thus gets compared with V_{ref} and change in the output state from $+V_{sat}$ to $-V_{sat}$ or vice versa indicates that V_1 has crossed the V_{ref} value. The waveforms are shown in the Fig. 6.10.

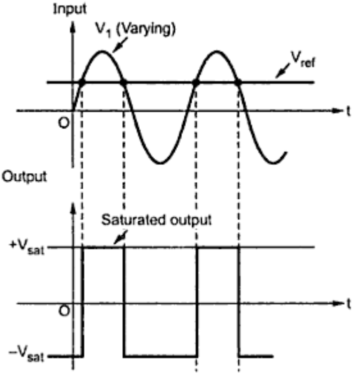


Fig. 6.10 Comparator waveforms

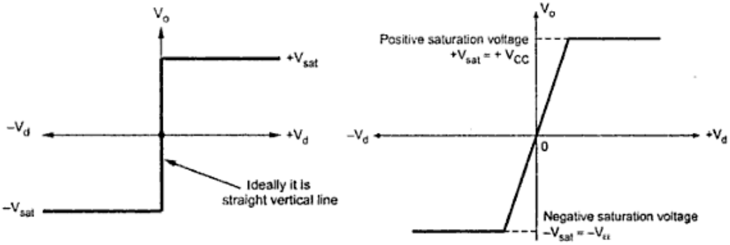
Key Point : *The circuit thus works as a comparator, comparing an unknown voltage with the reference voltage.*

6.6 Ideal Voltage Transfer Curve

The ideal op-amp produces the output proportional to the difference between the two input voltages. The graphical representation of this statement gives the voltage transfer curve. It is the graph of output voltage V_0 plotted against the difference input voltage V_d, assuming gain constant. This graph is called **transfer characteristics** of the op-amp.

Now the output voltage is proportional to difference input voltage but only upto the positive and negative saturation voltages of op-amp. These saturation voltages are specified by the manufacturer in terms of output voltage swing rating of an op-amp, for given value of supply voltages. These saturation voltages are slightly less than the supply voltages.

Thus, the voltage transfer curve is a straight line till output reaches saturation voltage level. Thereafter output remains constant. The ideal voltage transfer curve is shown in the Fig. 6.11 (a) while practical curve is shown in the Fig. 6.11 (b).



(a) Ideal (b) Practical

Fig. 6.11 Voltage transfer curves

The curve is not drawn to the scale.

Key Point : *If drawn to the scale, the curve would be almost vertical due to large values of op-amp gain.*

6.7 Equivalent Circuit of Practical Op-Amp

The circuit which represents op-amp parameters in terms of physical components, for the analysis purpose is called **equivalent circuit** of an op-amp. The equivalent circuit of an op-amp is shown in the Fig. 6.12.

The circuit shows the op-amp parameters like input resistance, output resistance, the open loop voltage gain in terms of circuit components like R_{in}, R_o etc. The op-amp amplifies the difference between the two input voltages.

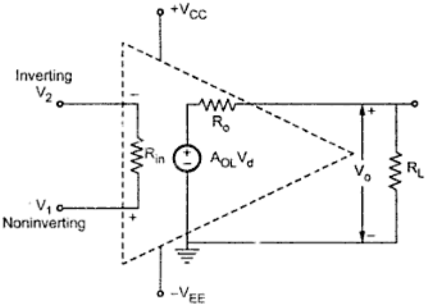


Fig. 6.12 Equivalent circuit of an op-amp

$$\boxed{V_o = A_{OL} V_d = A_{OL} (V_1 - V_2)}$$

where A_{OL} = Large signal open loop voltage gain.

V_d = Difference voltage $V_1 - V_2$.

V_1 = Noninverting input voltage with respect to ground.

V_2 = Inverting input voltage with respect to ground.

R_i = Input resistance of op-amp.

R_o = Output resistance of op-amp.

The output voltage is directly proportional to the difference voltage V_d.

It is to be noted that the op-amp amplifies difference voltage and not the individual input voltages. Thus the output polarity gets decided by the polarity of the difference voltage V_d.

The voltage source $A_{OL} V_d$ is the Thevenin's equivalent voltage source while R_o is the Thevenin's equivalent resistance looking back into the output terminals.

The equivalent circuit plays an important role in analysing various op-amp applications as well as in studying the effects of feedback on the performance of op-amp.

6.7.1 Practical Op-Amp Characteristics

The characteristics of an ideal op-amp can be approximated closely enough, for many practical op-amps. But basically the practical op-amp characteristics are little bit different than the ideal op-amp characteristics.

The various characteristics of a practical op-amp can be described as below.

a) Open loop gain :

It is the voltage gain of the op-amp when no feedback is applied. Practically it is several thousands.

b) Input impedance :

It is finite and typically greater than 1 MΩ. But using FETs for the input stage, it can be increased upto several hundred MΩ.

c) Output impedance :

It is typically few hundred ohms. With the help of negative feedback, it can be reduced to a very small value like 1 or 2 ohms.

d) Bandwidth :

The bandwidth of practical op-amp in open loop configuration is very small. By application of negative feedback, it can be increased to a desired value.

e) Input offset voltage :

Whenever both the input terminals of the op-amp are grounded, ideally, the output voltage should be zero. However, in this condition, the practical op-amp shows a small non zero output voltage. To make this output voltage zero, a small voltage in millivolts is required to be applied to one of the input terminals. Such a voltage makes the output exactly zero. This d.c. voltage, which makes the output voltage zero, when the other terminal is grounded is called **input offset voltage** denoted as V_{ios}. How much voltage, to which terminal and with what polarity, to be applied, is specified by the manufacturer in the datasheet. The input offset voltage depends on the temperature.

This is shown in the Fig. 6.13.

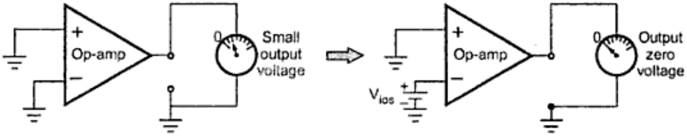


Fig. 6.13 Concept of input offset voltage

f) Input bias current :

For ideal op-amp, no current flows into the input terminals. The practical op-amps do have some input currents which are very small, of the order of 10^{-6} A to 10^{-14} A.

Most of the op-amps use differential amplifier as the input stage. The two transistors of the differential amplifier must be biased correctly. But practically, it is not possible to get exact matching of the two transistors. Thus, the input terminals which are the base terminals of the two transistors, do conduct the small d.c. current. These small base currents of the two transistors are nothing but bias currents denoted as I_{b1} and I_{b2}.

So input bias current can be defined as the current flowing into each of the two input terminals when they are biased to the same voltage level i.e. when the op-amp is balanced.

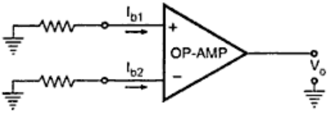


Fig. 6.14 Input bias currents

The two input currents, when op-amp is balanced, are shown in the Fig. 6.14.

The two bias currents are never same hence the manufacturers specify the average input bias current I_b, which is found by adding the magnitudes of I_{b1} and I_{b2} and dividing the sum by 2.

Mathematically it is expressed as,

Input bias current, $$\boxed{I_b = \frac{|I_{b1}| + |I_{b2}|}{2}} \quad \text{... (1)}$$

g) Input offset current :

The difference in magnitudes of I_{b1} and I_{b2} is called as input offset current and is denoted as I_{ios}. Thus,

Input offset current, $\boxed{I_{ios} = | I_{b1} - I_{b2} |}$ ... (2)

The magnitude of this current is very small, of the order of 20 to 60 nA. It is measured under the condition that input voltage to op-amp is zero.

If we supply equal d.c. currents to the two inputs, output voltage of op-amp must be zero. But practically, there exists some voltage at the output. To make it zero, the two input currents are made to differ by small amount. This difference is nothing but the input offset current.

Key Point : *Both input bias as well as input offset currents depend on the temperature.*

h) Output offset voltage :

Ideally when both the inputs of op-amp are at zero potential, output must be zero. But both input offset voltage and bias current contribute to produce output voltage with zero inputs. This voltage existing at the output when inputs are zero is called **output offset voltage** and denoted as V_{oos}.

➠ **Example 6.2 :** *If the base currents for the emitter coupled transistors of a differential amplifier are 18 μA and 22 μA, determine*

i) Input bias current and ii) Input offset current for an op-amp.

Solution : The two input base currents are

$$I_{b1} = 18\,\mu A \quad \text{and} \quad I_{b2} = 22\,\mu A$$

i) The input bias current is

$$I_b = \frac{I_{b1} + I_{b2}}{2} = \frac{18+22}{2} = 20\,\mu A$$

ii) The input offset current is

$$I_{ios} = |I_{b1} - I_{b2}| = |18 - 22| = 4\,\mu A$$

➠ **Example 6.3 :** *For a particular op-amp, the input offset current is 20 nA while input bias current is 60 nA. Calculate the values of two input bias currents.*

Solution : $I_{ios} = 20$ nA, $I_b = 60$ nA

Now $$I_{ios} = I_{b1} - I_{b2} = 20$$

$$I_b = \frac{I_{b1} + I_{b2}}{2} = 60$$

$$\therefore \quad I_{b1} + I_{b2} = 120$$

$$\therefore \quad 2I_{b1} = 140$$

6.10.1 Pin Diagram

The IC 741 is 8 pin IC available in dual in line package (DIP). The pin diagram of IC741 op-amp is shown in the Fig. 6.17.

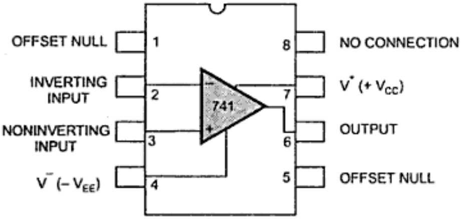


Fig. 6.17 Pin diagram of IC 741 op-amp

The pins 1 and 5 are offset null pins. These are used to nullify offset voltages and provide offset voltage compensation. The pin 2 is inverting input while pin 3 is noninverting input terminal. The output is to be taken from pin 6. The op-amp requires dual supply i.e. positive supply and negative supply. The positive supply is to be given to pin 7 while negative supply is to be given to pin 4. Thus pin 4 is for $-V_{EE}$ supply while pin 7 is for $+V_{CC}$ supply. The pin 8 is the dummy pin and no connection are to be made to this pin externally.

6.10.2 Ideal Vs Practical Characteristics of IC 741 Op-Amp

Let us compare the ideal op-amp characteristics with practical characteristics of IC 741 op-amp.

The Table 6.2 lists the ideal op-amp characteristics and the typical characteristics for 741 IC, a popular general purpose op-amp IC.

Sr. No	Parameter	Symbol	Ideal	Typical for 741 IC
1	Open loop voltage gain	A_{OL}	∞	2×10^5
2	Output impedance	Z_{out}	0	75 Ω
3	Input impedance	Z_{in}	∞	2 MΩ
4	Input offset current	I_{ios}	0	20 nA
5	Input offset voltage	V_{ios}	0	2 mV
6	Bandwidth	B.W	∞	1 MHz
7	CMRR	ρ	∞	90 dB
8	Slew rate	S	∞	0.5 V/ µsec
9	Input bias current	I_b	0	80 nA
10.	Power supply rejection ratio	PSRR	0	30 µV/V

Table 6.2

6.10.3 Features of IC 741

i) No frequency compensation required.

ii) Short circuit protection provided.

iii) Offset voltage null capability.

iv) Large common mode and differential voltage range.

v) No latch up.

6.11 Open Loop Configuration of Op-Amp

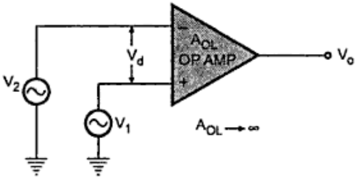


Fig. 6.18 Open loop operation of an op-amp

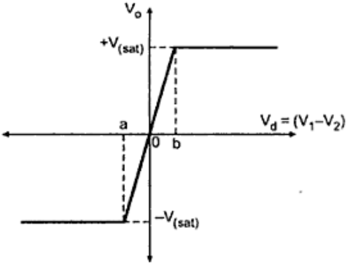


Fig. 6.19 Voltage transfer characteristics

The simplest possible way to use an op-amp is in the open loop mode. The Fig. 6.18 shows an op-amp in the open loop condition.

We know that the d.c. supply voltages applied to the op-amp are V_{CC} and $-V_{EE}$ and the output varies linearily only between V_{CC} and $-V_{EE}$.

Since gain is very large in open loop condition, the output voltage V_o is either at its positive saturation voltage $(+V_{sat})$ or negative saturation voltage $(-V_{sat})$ as $V_1 > V_2$ or $V_2 > V_1$ respectively. This is shown in the Fig. 6.19.

Thus very small noise voltage present at the input also gets amplified due to its high open loop gain and op-amp gets saturated.

It can be seen from the Fig. 6.19, only for small range of input signal (from point a to b), it behaves linearily. This range is very small and practically due to high open loop gain, op-amp either shows $+V_{sat}$ or $-V_{sat}$ level.

This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode.

Hence, the op-amp is generally not used in the open loop configuration.

Such an open loop behaviour of the op-amp finds some rare applications like voltage comparator, zero crossing detector etc.

6.12 Closed Loop Configuration of Op-Amp

The utility of op-amp increases considerably if it is used in a closed loop mode. The closed loop mode is possible using feedback. The feedback allows to feed some part of the output back to the input. In linear applications the op-amp is always used with negative feedback. The feedback helps to control gain which otherwise drives op-amp into saturation.

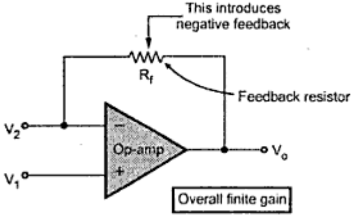


Fig. 6.20 Op-amp with negative feedback

The negative feedback is possible by adding a resistor as shown in the Fig. 6.20, called **feedback resistor**. The feedback is said to be negative as the feedback resistor connects the output to the inverting input terminal.

The gain resulting with feedback is called **closed loop gain** of the op-amp. Due to feedback resistance there is reduction in the gain. The closed loop gain is much less than the open loop gain and is independent of it.

Most of the linear circuits use op-amp in a closed loop mode with negative feedback with R_f. This is because, due to reduced gain, the output is not driven into the saturation and the circuit behaves in a linear manner.

6.12.1 Advantages of Negative Feedback

The advantages of negative feedback are,

i) It reduces the gain and makes it controllable.

ii) It reduces the possibility of distortion.

iii) It increases the bandwidth i.e. frequency range.

iv) It increases the input resistance of the op-amp.

v) It decreases the output resistance of the op-amp.

vi) It reduces the effects of temperature, power supply on the gain of the circuit.

6.13 Realistic Simplifying Assumptions

We can make two assumptions which are realistic and simplify the analysis of op-amp circuits to a great extent. The assumptions are useful and can be used to obtain the output expressions in variety of linear applications.

6.13.1 Zero Input Current

The current drawn by either of the input terminals (inverting and noninverting) is zero.

In practice, the current drawn by the input terminals is very small, of the order of μA or nA. Hence the assumption of zero input current is realistic.

6.13.2 Virtual Ground

This means the differential input voltage V_d between the noninverting and inverting input terminals is essentially zero.

This is obvious because even if output voltage is few volts, due to large open loop gain of op-amp, the difference voltage V_d at the input terminals is almost zero.

e.g. if output voltage is 10 V and the A_{OL} i.e. open loop gain is 10^4 then

$$V_o = V_d A_{OL}$$

$$\therefore \quad V_d = \frac{V_o}{A_{OL}} = \frac{10}{10^4} = 1 \text{ mV}$$

Hence V_d is very small. As $A_{OL} \to \infty$, the difference voltage $V_d \to 0$ and realistically assumed to be zero for analysing the circuits.

$$\therefore \quad V_d = \frac{V_o}{A_{OL}}$$

$$\therefore \quad (V_1 - V_2) = \frac{V_o}{\infty} = 0$$

$$\therefore \quad \boxed{V_1 = V_2} \qquad \text{... (1)}$$

Thus we can say that **under linear range of operation there is virtually short circuit between the two input terminals, in the sense that their voltages are same.** No current flows from the input terminals to the ground. The Fig. 6.21 shows the concept of the virtual ground. The thick line indicates the virtual short circuit between the input terminals.

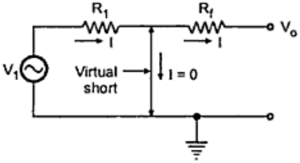


Fig. 6.21 Concept of virtual ground in an op-amp

Now if the noninverting terminal is grounded, by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection between the inverting terminal and the ground. This is the **principle of virtual ground.**

Thus from the equation (1), the **voltage at the one input terminal of an op-amp can be realistically assumed to be equal to the voltage at the other input terminal.**

This concept is very much useful in the analysis of closed loop op-amp circuits.

Let us study now some linear applications of op-amp.

6.14 Op-Amp Applications

The countless simple circuits using one or more operational amplifiers, some external resistors and the capacitors can be constructed. Such op-amp applications are classified as linear and nonlinear type of applications.

In the linear applications, output voltage varies linearily with respect to the input voltage. The negative feedback is the base of linear applications. Some of the linear applications are voltage follower, differential amplifier, instrumentation amplifier, inverting amplifier, noninverting amplifier etc.

In the nonlinear applications, a feedback is provided from the output to the input terminal. The feedback may be provided to the inverting input terminal using nonlinear elements like diodes, transistors etc. The nonlinear input to output characteristics is the feature of nonlinear applications. The typical nonlinear applications are precision rectifiers, comparators, clampers, limiters, schmitt trigger circuit etc.

While deriving the expressions and analysing such circuits, the **realistic assumptions** can be conviniently used. The op-amp input current is zero while the potential difference between inverting and noninverting terminals is zero. Thus if one terminal is grounded, then potential of other terminal can be assumed zero i.e. it is also at ground potential. This is the concept of virtual ground, which plays an important role in analysing the op-amp application circuits.

6.15 Inverting Amplifier

As the name suggests the output of such an amplifier is inverted as compared to the input signal. The inverted output signal means having a phase shift of 180° as compared to the input signal.

So, an amplifier which provides a phase shift of 180° between input and output is called **inverting amplifier.**

The basic circuit diagram of an inverting amplifier using op-amp is shown in the Fig. 6.22 (a).

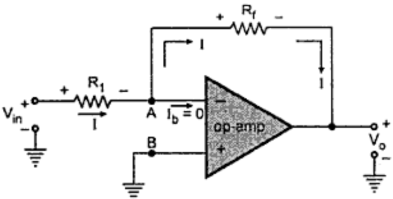


Fig. 6.22 (a) Inverting amplifier

The input and output waveforms are shown in the Fig. 6.22 (b).

Observations :

1. The output is inverted with respect to input, which is indicated by minus sign.
2. The voltage gain is independent of open loop gain of the op-amp, which is assumed to be large.
3. The voltage gain depends on the ratio of the two resistances. Hence selecting R_f and R_1, the required value of gain can be easily obtained.
4. If $R_f > R_1$, the gain is greater than 1.

   If $R_f < R_1$, the gain is less than 1.

   If $R_f = R_1$, the gain is unity.

   Thus the output voltage can be greater than, less than or equal to the input voltage, in magnitude.
5. If the ratio of R_f and R_1 is K which is other than one, the circuit is called **scale changer** while for $R_f / R_1 = 1$ it is called **phase inverter**.
6. The closed loop gain is denoted as A_{VF} or A_{VCL} i.e. gain with feedback.

➠ **Example 6.4 :** *Determine the voltage gain of the op-amp circuit shown in the Fig. 6.23.*

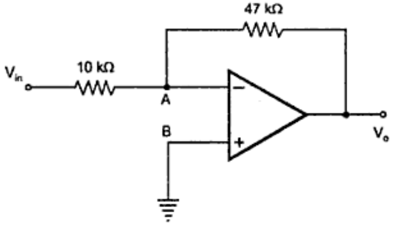


Fig. 6.23

Solution : From the Fig. 6.23, $R_1 = 10\ k\Omega$, $R_f = 47\ k\Omega$

The circuit is inverting amplifier,

$$\therefore \quad \text{Gain} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

$$= -\frac{47\times 10^3}{10\times 10^3} = -4.7$$

The gain is 4.7 and negative sign indicates phase shift i.e. inverting mode.

Example 6.5 : *A sine wave of 0.5 V peak voltage is applied to an inverting amplifier using $R_1 = 10\ k\Omega$ and $R_f = 50\ k\Omega$. It uses the supply voltages of ± 12 V. Determine the output and sketch the waveform.*

If now the amplitude of input sine wave is increased to 5 V, what will be the output ? Is it practically possible ? Sketch the waveform.

Solution : For an inverting amplifier.

$$\text{Gain} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} = \frac{-50}{10} = -5$$

Now $V_m = 0.5$ V for the input hence

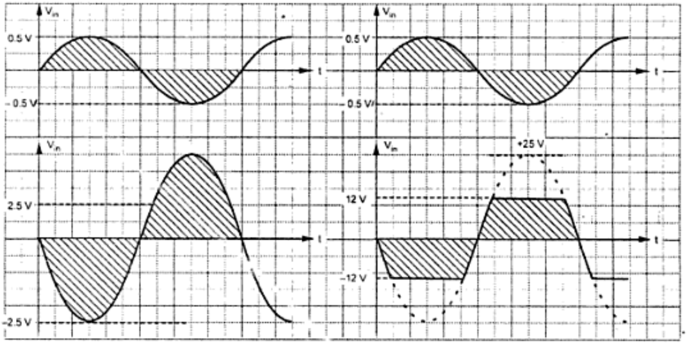
$$(V_o)_m = (V_{in})_m \times \text{Gain} = 0.5 \times 5 = 2.5 \text{ V peak}$$

The input and output waveforms are inverted with respect to each other and are shown in the Fig. 6.24 (a).

Now $V_m = 5$ V for the input hence,

$$(V_o)_m = (V_{in})_m \times \text{Gain} = 5 \times 5 = 25 \text{ V peak}$$

But op-amp output saturates at ± 12 V i.e. at supply voltages used. So portion above ± 12 V and below − 12 V will be clipped off from the output. So 25 V peak output is not practically possible. The input and output waveforms are shown in the Fig. 6.24 (b).



(a) $(V_{in})_m = 0.5$ V (b) $(V_{in})_m = 5$ V

Fig. 6.24

In both cases, there exists a phase shift of 180° between input and output.

6.16 Noninverting Amplifier

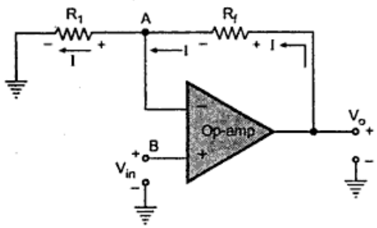


Fig. 6.25 (a) Noninverting amplifier

An amplifier which amplifies the input without producing any phase shift between input and output is called **Noninverting amplifier.** The basic circuit diagram of a noninverting amplifier using op-amp is shown in the Fig. 6.25 (a). The input is applied to the noninverting input terminal of the op-amp.

Derivation of closed loop gain :

The node B is at potential V_{in}, hence the potential of point A is same as B which is V_{in}, from the concept of virtual share.

$$\therefore \quad V_A = V_B = V_{in} \quad \ldots (1)$$

From the output side we can write,

$$I = \frac{V_o - V_A}{R_f}$$

$$\therefore \quad I = \frac{V_o - V_{in}}{R_f} \quad \ldots (2)$$

At the inverting terminal,

$$I = \frac{V_A - 0}{R_1}$$

$$\therefore \quad I = \frac{V_{in}}{R_1} \quad \ldots (3)$$

Entire current passes through R_1 as input current of op-amp is zero.

Equating equations (2) and (3),

$$\therefore \quad \frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\therefore \quad \frac{V_o}{R_f} = \frac{V_{in}}{R_f} + \frac{V_{in}}{R_1}$$

$$\therefore \quad \frac{V_o}{R_f} = V_{in}\left[\frac{(R_1 + R_f)}{R_1 R_f}\right]$$

$$\therefore \quad \frac{V_o}{V_{in}} = \frac{(R_1 + R_f)R_f}{R_1 R_f} = \frac{R_1 + R_f}{R_1}$$

$$\therefore \quad \boxed{A_{VF} = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}} \qquad \ldots (4)$$

The positive sign indicates that there is no phase shift between input and output.

The input and output waveforms are shown in the Fig. 6.25(b).

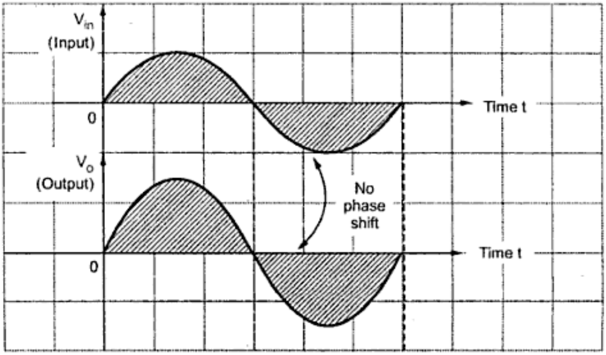


Fig. 6.25 (b) Waveforms of noninverting amplifier

The Table 6.3 provides the comparison of the ideal inverting and noninverting amplifier op-amp circuits.

Ideal inverting amplifier	Ideal noninverting amplifier
1. Voltage gain = $-R_f/R_1$.	1. Voltage gain = $1 + (R_f / R_1)$.
2. The output is inverted with respect to input.	2. No phase shift between input and output.
3. The voltage gain can be adjusted as greater than, equal to or less than one.	3. The voltage gain is always greater than one.
4. The input impedance is R_1 .	4. The input impedance is extremely large.

Table 6.3

Observations

1. The voltage gain is always greater than one.
2. The voltage gain is positive indicating that for a.c. input, the output and input are in phase while for d.c. input, the output polarity is same as that of input.
3. The voltage gain is independent of open loop gain of op-amp, but depends only on the two resistance values.
4. The desired voltage gain can be obtained by selecting proper values of R_f and R_1.

➡ **Example 6.6 :** *An Op-Amp is used in following modes with* $R_1 = 1\,k\Omega$*, and* $R_f = 100\,k\Omega$ *,* $V_i = 10\ mV$ *and* $V_{CC} = \pm 12\ V$*. Find* V_o *is each case.*

i) Inverting mode *ii) Noninverting mode*

Solution : Given values are ,

$R_1 = 1\ k\Omega$, $R_f = 100\ k\Omega$, $V_i = 10$ mV and $V_{CC} = \pm 12$ V

i) Inverting mode :

$$\text{Gain} = \frac{V_o}{V_i} = -\frac{R_f}{R_1} = -\frac{100}{1} = -100$$

$$\therefore \quad V_o = -100\ V_i = -100 \times (10\ \text{mV}) = \mathbf{-1\ V}$$

ii) Noninverting mode :

$$\text{Gain} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1} = 1 + \frac{100}{1} = 101$$

$$\therefore \quad V_o = 101\ V_i = 101\ (10\ \text{mV}) = \mathbf{1.01\ V}$$

If V_i is sinusoidal, the output waveforms for above two cases are as shown, (See Fig. 6.26 on next page).

➡ **Example 6.7 :** *Find the gain and output voltage for a noninverting amplifier using op-amp when input voltage is i) + 0.5 V ii) – 3 V. Assume supply voltage employed is ±12 V,* $R_f = 10\ k\Omega$*,* $R_1 = 1\ k\Omega$*.*

Solution : The gain is,

$$\text{Gain} = 1 + \frac{R_f}{R_1} = 1 + \frac{10}{1} = 11$$

For $V_{in} = 0.5$ V, $V_o = 11 \times 0.5 = \mathbf{5.5\ V}$

For $V_{in} = -3$ V, $V_o = -3 \times 11 = \mathbf{-33\ V}$

But – 33 V is not possible. Output will saturate at – 12 V and remaining portion will be clipped off from the output.

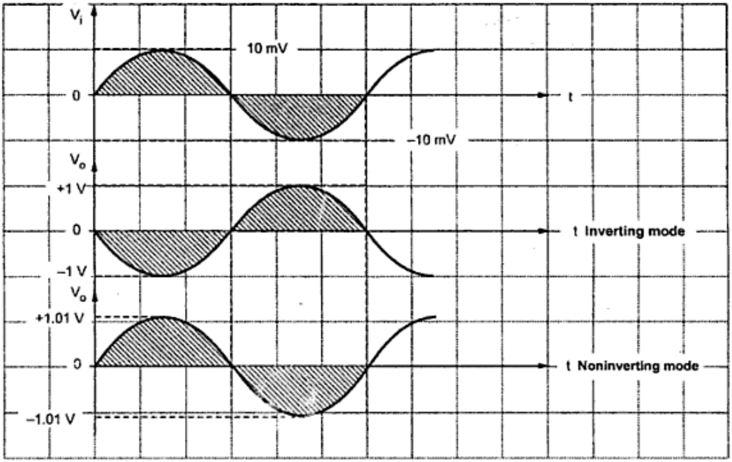


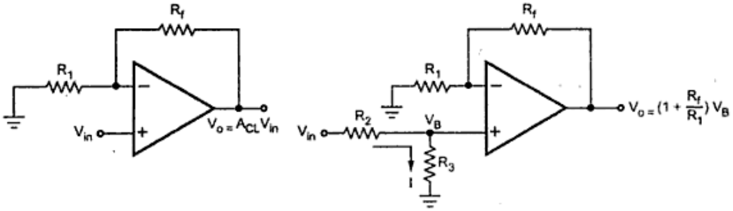
Fig. 6.26

6.17 Important Point about Noninverting Amplifier

Consider a noninverting amplifier shown in the Fig. 6.27 (a). In this case,

$$V_o = \left(1+\frac{R_f}{R_1}\right) V_{in}$$

But consider a noninverting amplifier shown in the Fig. 6.27 (b). In this case V_{in} is not directly applied to the noninverting terminal.


R_f
R_1
V_in
V_o = A_CL V_in
R_f
R_1
R_2
V_B
V_in
I
R_3
V_o = (1 + R_f/R_1) V_B

(a) V_{in} directly applied

(b) V_{in} applied through resistive circuit

Fig. 6.27

Key Point: *Remember that the noninverting amplifier always amplifies voltage at its noninverting terminal i.e.* V_B *by* $\left(1+R_f/R_1\right)$ *times.*

In second case the output voltage V_0 is given by,

$$V_o = \left(1+\frac{R_f}{R_1}\right)V_B \quad \text{and} \quad V_o \neq \left(1+\frac{R_f}{R_1}\right)V_{in}$$

Then analysing circuit at noninverting terminal, V_B can be obtained in terms of V_{in}. In the circuit shown in the Fig. 6.27 (b), $R_2 - R_3$ forms potential divider and as op-amp input current is zero,

$$V_B = \frac{V_{in}}{R_2+R_3} \times R_3$$

$$\boxed{V_o = \left(1+\frac{R_f}{R_1}\right)V_B = \left(1+\frac{R_f}{R_1}\right)\left(\frac{R_3}{R_2+R_3}\right)V_{in}}$$

This fact helps to analyse complex op-amp circuits in which noninverting amplifier is a subpart.

➡ **Example 6.8 :** *Find* V_o *for the circuit shown in the Fig. 6.28.*

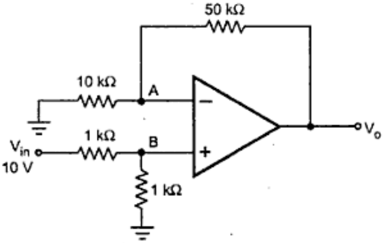


Fig. 6.28

Solution : This is noninverting amplifier but it will amplify V_B by $1+\frac{R_f}{R_1}$ and not $V_{in} = 10\,V$. The op-amp input current is zero hence part of the circuit is as shown in the Fig. 6.28 (a).

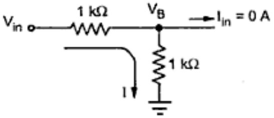


Fig. 6.28 (a)

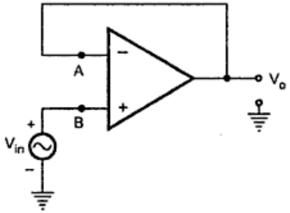


Fig. 6.30 Voltage follower

The node B is at potential V_{in}. Now node A is also at the same potential as B i.e. V_{in}.

$$\therefore \quad V_A = V_B = V_{in} \qquad \ldots (1)$$

Now node A is directly connected to the output. Hence we can write,

$$V_o = V_A \qquad \ldots (2)$$

Equating the equations (1) and (2),

$$\boxed{V_o = V_{in}} \qquad \ldots (3)$$

For this circuit, the voltage gain is unity.

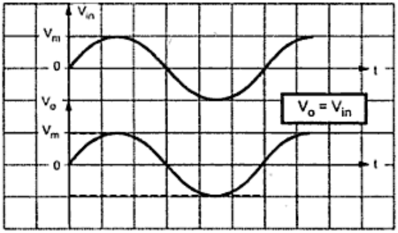


Fig. 6.31

Thus the output voltage V_o is equal to the input voltage V_{in}. If V_{in} increases, V_o also increases. If V_{in} decreases, then V_o also decreases. Thus output follows the input hence the circuit is called voltage follower circuit. It is also called **source follower, unity gain amplifier, buffer amplifier** or **isolation amplifier.** The input and output waveforms are shown in the Fig. 6.31.

6.18.1 Advantages of Voltage Follower

The advantages of such voltage follower circuit are,

1) Very large input resistance, of the order of MΩ.
2) Low output impedance, almost zero. Hence it can be used to connect high impedance source to a low impedance load, as a buffer.
3) It has large bandwidth.

6.19 Summer or Adder Circuit

As the input impedance of an op-amp is extremely large, more than one input signal can be applied to the inverting amplifier. Such circuit gives the addition of the applied signals at the output. Hence it is called **summer** or **adder** circuit. Depending upon the sign of the output, the summer circuits are classified as inverting summer and noninverting summer.

6.19.1 Inverting Summer

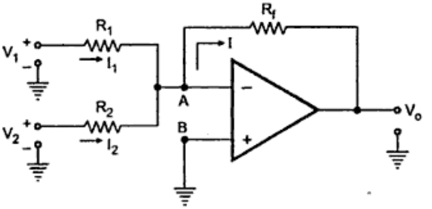


Fig. 6.34 Inverting summer

In this circuit, all the input signals to be added are applied to the inverting input terminal of the op-amp. The circuit with two input signals is shown in the Fig. 6.34.

As point B is grounded, due to virtual ground concept the node A is also at virtual ground potential.

$$\therefore \qquad V_A = V_B = 0 \qquad \dots (1)$$

Now from the input side,

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1} \qquad \dots (2)$$

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2} \qquad \dots (3)$$

Applying at node A and as input op-amp current is zero,

$$I = I_1 + I_2 \qquad \dots (4)$$

From the output side,

$$I = \frac{V_A - V_o}{R_f} = -\frac{V_o}{R_f} \qquad \dots (5)$$

Substituting (5), (2) and (3) in (4),

$$-\frac{V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2}$$

$$\therefore \qquad \boxed{V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2\right]} \qquad \dots (6)$$

If the three resistances are equal, $R_1 = R_2 = R_f$

$$\boxed{V_o = -(V_1 + V_2)}$$

By properly selecting R_f, R_1 and R_2, we can have weighted addition of the input signals like $aV_1 + bV_2$, as indicated by the equation (6).

Infact in such a way, n input voltages can be added.

Thus the magnitude of the output voltage is the sum of the input voltages and hence circuit is called summer or adder circuit. Due to the negative sign of the sum at the output it is called inverting summer. It shows that there is phase inversion.

6.19.2 Noninverting Summing Amplifier

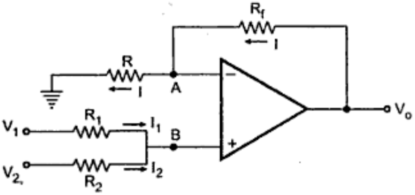


Fig. 6.35 Noninverting summing amplifier

The circuit discussed above is inverting summing amplifier, which can be noticed from the negative sign in the equation (6). But a summer that gives non-inverted sum of the input signals is called **non-inverting summing amplifier.** The circuit is shown in the Fig. 6.35.

Let the voltage of node B is V_B. Now the node A is at the same potential as that of B.

$$\therefore \qquad V_A = V_B \qquad \text{... (7)}$$

From the input side,

$$I_1 = \frac{V_1 - V_B}{R_1} \quad \text{and} \quad I_2 = \frac{V_2 - V_B}{R_2} \qquad \text{...(8)}$$

But as the input current of op-amp is zero,

$$I_1 + I_2 = 0 \qquad \text{...(9)}$$

$$\therefore \quad \frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0 \qquad \text{... substituting (8) in (9)}$$

$$\therefore \quad \frac{V_1}{R_1} + \frac{V_2}{R_2} = V_B\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$$

$$\therefore \quad V_B = \frac{(R_2 V_1 + R_1 V_2)}{(R_1 + R_2)} \qquad \text{...(10)}$$

Now at node A, $I = \frac{V_A}{R} = \frac{V_B}{R}$ as $V_B = V_A$ ...(11)

and $$I = \frac{V_o - V_A}{R_f} = \frac{V_o - V_B}{R_f} \qquad \text{...(12)}$$

Equating the two equations (11) and (12),

$$\therefore \quad \frac{V_B}{R} = \frac{V_o - V_B}{R_f}$$

$$\therefore \quad \frac{V_o}{R_f} = V_B\left[\frac{1}{R}+\frac{1}{R_f}\right]$$

$$\therefore \quad V_o = V_B\,\frac{[R+R_f]}{R} \qquad \text{... (13)}$$

Substituting equations (10) in (13) we get,

$$V_o = \frac{(R_2\,V_1 + R_1\,V_2)[R+R_f\,]}{R\,(R_1+R_2)}$$

i.e. $$\boxed{V_o = \frac{R_2\,(R+R_f)}{R\,(R_1+R_2)}\,V_1 + \frac{R_1\,(R+R_f)}{R\,(R_1+R_2)}\,V_2} \qquad \text{... (14)}$$

The equation (14) shows that the output is **weighted sum** of the inputs.

If $R_1 = R_2 = R = R_f$ we get, $V_o = V_1 + V_2$

As there is no **phase difference between input and output,** it is called noninverting summer amplifier.

6.19.3 Average Circuit

If in the inverting summer circuit, the values of resistance are selected as,

$$R_1 = R_2 = R$$

and $$R_f = \frac{R}{2}$$

Then from the equation ($V_o = V_1 + V_2$) we get,

$$V_o = -\left[\frac{R/2}{R}\,V_1 + \frac{R/2}{R}\,V_2\right] = -\,\frac{(V_1+V_2)}{2} \qquad \text{... (15)}$$

Thus the magnitude of the output voltage is the average of the two input voltages. So circuit acts like an **averager.**

Similarly average of n inputs can be calculated by selecting

$R_1 = R_2 = R_3 = \;...\; = R_n = R$ and $R_f = \frac{R}{n}$.

Example 6.10 : *Determine the output voltage in Fig. 6.36.*

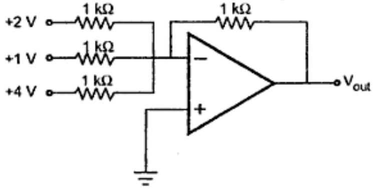


Fig. 6.36

Solution :

$$V_{out} = -(V_{in\,1} + V_{in\,2} + V_{in\,3})\frac{R_f}{R_1}$$

$$= -(2\text{ V} + 1\text{ V} + 4\text{ V})\frac{1\text{ k}\Omega}{1\text{ k}\Omega}$$

$$= -7\text{ V}$$

Example 6.11 : *Design a scaling adder circuit using an op-amp, to give the output $V_o = -(3V_1 + 4V_2 + 5V_3)$.*

Solution : For an inverting summer,

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

Let $R_f = 120\text{ k}\Omega$

$\therefore \frac{R_f}{R_1} = 3$ hence $R_1 = 40\text{ k}\Omega$

$\therefore \frac{R_f}{R_2} = 4$ hence $R_2 = 30\text{ k}\Omega$

$\therefore \frac{R_f}{R_3} = 5$ hence $R_3 = 24\text{ k}\Omega$

Hence the circuit is as shown in the Fig. 6.37.

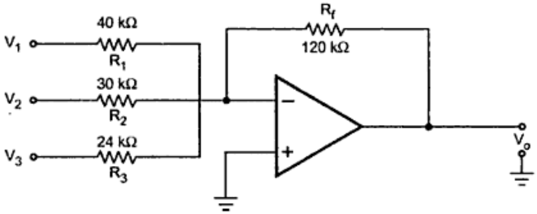

R_f
120 kΩ
40 kΩ
V_1
R_1
30 kΩ
V_2
R_2
24 kΩ
V_3
R_3
−
+
V_o

Fig. 6.37

Example 6.12 : *Determine the output voltage for the circuit shown in the Fig. 6.38, for* $V_1 = 1$ *V and* $V_2 = 3$ *V.*

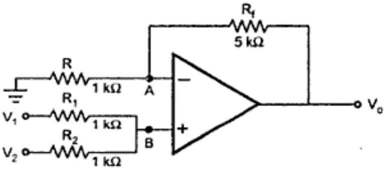

R_f
5 kΩ
R
1 kΩ
A
R_1
V_1
1 kΩ
R_2
B
V_2
1 kΩ
−
+
V_o

Fig. 6.38

Solution : In this circuit $R_1 = R_2 = 1\,k\Omega$.

The voltage at noninverting terminal is given by the equation (4).

$$\therefore \quad V_B = \frac{R_2V_1 + R_1V_2}{R_1 + R_2} = \frac{V_1 + V_2}{2} \qquad \ldots R_1 = R_2 = R'$$

The circuit reduces to a noninverting amplifier with $V_B = V_1 + V_2 / 2$ as shown in the Fig. 6.38(a).

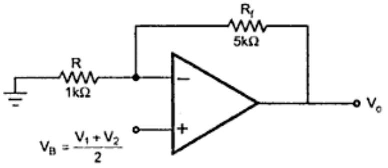

R_f
5kΩ
R
1kΩ
−
+
V_o
$V_B = \frac{V_1 + V_2}{2}$

Fig. 6.38(a)

$$\therefore \quad V_B = \frac{1+3}{2} = 2$$

For a noninverting amplifier, it amplifies voltage at its noninverting input terminal by the gain $1 + \frac{R_f}{R}$.

$$\therefore \quad V_o = V_B\left(1+\frac{R_f}{R}\right) = 2\left(1+\frac{5}{1}\right) = 12 \text{ V}$$

Alternatively equation (8) can be used to find V_o,

$$V_o = \frac{R_2(R+R_f)}{R(R_1+R_2)}V_1 + \frac{R_1(R+R_f)}{R(R_1+R_2)}V_2$$

$$= \left[\frac{1(6)}{1(1+1)}\right]\times 1 + \left[\frac{1\times 6}{1\times(1+1)}\right]\times 3 = 3 + 9 = 12 \text{ V}$$

Example 6.13 : *With the help of a neat circuit diagram, derive the expression for the output voltage of an inverting summing amplifier using op-amp with three input voltages applied to the inverting terminal through resistors of value R and a feedback resistor also of the same value.* **(UPTU - May-2004)**

Solution : The circuit diagram is shown in the Fig. 6.39.

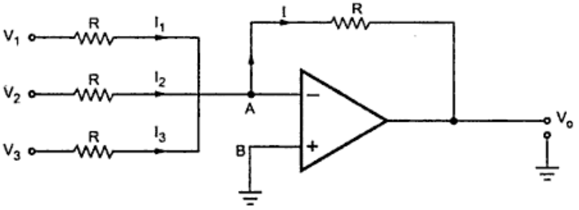


Fig. 6.39

B is grounded hence A is virtually grounded.

$$\therefore \quad V_A = V_B = 0 \text{ V} \quad \ldots (1)$$

Op-amp input current is zero.

$$\therefore \quad I = I_1 + I_2 + I_3 \quad \ldots (2)$$

$$\therefore \quad \frac{V_A - V_o}{R} = \frac{V_1 - V_A}{R} + \frac{V_2 - V_A}{R} + \frac{V_3 - V_A}{R}$$

$$\therefore \quad V_o = -[V_1 + V_2 + V_3] \quad \ldots \text{As } V_A = 0 \text{ V}$$

This is the required expression for the output.

And $$I = \frac{V_{o2} - V_A}{R_f} = \frac{V_{o2} - V_B}{R_f} \qquad \dots (4)$$

Equating the equations (3) and (4),

$$\frac{V_B}{R_1} = \frac{V_{o2} - V_B}{R_f}$$

$$\therefore \quad V_{o2} = \frac{R_1 + R_f}{R_1} V_B$$

$$\therefore \quad V_{o2} = \left[1 + \frac{R_f}{R_1}\right] V_B \qquad \dots (5)$$

Substituting V_B from (2) in (5) we get,

$$V_{o2} = \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2 \qquad \dots (6)$$

Hence using Superposition principle,

$$V_o = V_{o1} + V_{o2}$$

$$\therefore \quad \boxed{V_o = -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2} \qquad \dots (7)$$

Now if the resistances are selected as $R_1 = R_2$,

$$V_o = -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_1 + R_f}\right] V_2$$

$$= -\frac{R_f}{R_1} V_1 + \frac{R_f}{R_1} V_2$$

$$\therefore \quad \boxed{V_o = +\frac{R_f}{R_1} (V_2 - V_1)} \qquad \dots (8)$$

Thus the output voltage is proportional to the difference between the two input voltages. Thus it acts as a subtractor or difference amplifier.

If $R_1 = R_2 = R_f$ is selected,

$$\therefore \quad \boxed{V_o = V_2 - V_1} \qquad \dots (9)$$

But by selecting proper values of R_1, R_2 and R_f, we can have the subtraction of two inputs with appropriate strengths like

$$V_o = aV_2 - b\,V_1$$

➡ **Example 6.14 :** *Draw the circuit diagram of a difference amplifier with a gain of 10 and write the expression for the output voltage.*

Solution : The output of a difference amplifier with

$$R_1 = R_2 \text{ is given by,}$$

$$V_o = \frac{R_f}{R_1}(V_2 - V_1)$$

It is required that $\frac{R_f}{R_1} = 10$

$\therefore$ $R_f = 10\,R_1$

$\therefore$ Choose $R_1 = 1\ \text{k}\Omega$ and $R_f = 10\ \text{k}\Omega$

The circuit diagram is shown in the Fig. 6.42.

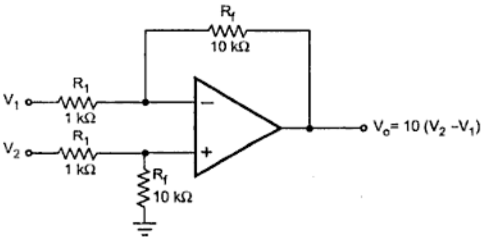


Fig. 6.42

6.21 Integrator

In an integrator circuit, the output voltage is the integration of the input voltage. The integrator circuit can be obtained without using active devices like op-amp, transistors etc. In such a case an integrator is called **passive integrator**. While an integrator using an active devices like op-amp is called **active integrator**. In this section, we will discuss the operation of active op-amp integrator circuit.

Example 6.15 : *A sinusoidal signal with peak value 6 mV and 2 kHz frequency is applied to the input of an ideal op-amp integrator with $R_1 = 100\ k\Omega$ and $C_f = 1\ \mu F$. Find the output voltage.*

Solution : For an ideal integrator

$$V_o = -\frac{1}{R_1 C_f}\int_0^t V_{in}\, dt$$

Now $R_1 = 100\ k\Omega$, $C_f = 1\mu F$, $V_{in} = V_m \sin \omega t$

where $V_m = 6$ mV and $\omega = 2\pi f = 2\pi \times 2\times 10^3 = 4\pi\times 10^3$ rad / s

$$\therefore \quad V_o = -\frac{1}{100\times10^3\times1\times10^{-6}}\int_0^t 6\times10^{-3}\sin\left(4\pi\times10^3 t\right) dt$$

$$= -0.06\left[\frac{-\cos\left(4\pi\times10^3\ t\right)}{4\pi\times10^3}\right]_0^t$$

$$= \mathbf{4.77\times10^{-6}\left[\cos(4000\pi t) - 1\right]\ V}$$

6.22 Differentiator

The circuit which produces the differentiation of the input voltage at its output is called **differentiator.** The differentiator circuit which does not use any active device is called **passive differentiator.** While the differentiator using an active device like op-amp is called an **active differentiator.** Let us discuss first the operation of ideal active op-amp differentiator circuit.

6.22.1 Ideal Active Op-Amp Differentiator

The active differentiator circuit can be obtained by exchanging the positions of R and C in the basic active integrator circuit. The op-amp differentiator circuit is shown in the Fig. 6.50.

The node B is grounded. The node A is also at the ground potential hence $V_A = 0$.

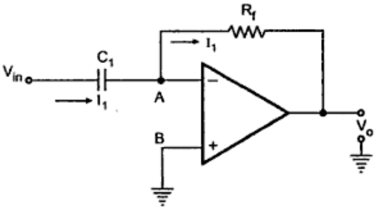


Fig. 6.50 Op-amp differentiator

As input current of op-amp is zero, entire current I_1 flows through the resistance R_f.

From the input side we can write,

$$I_1 = C_1 \frac{d(V_{in} - V_A)}{dt} = C_1 \frac{dV_{in}}{dt} \quad \text{... (1)}$$

From the output side we can write,

$$I = \frac{(V_A - V_o)}{R_f} = -\frac{V_o}{R_f} \quad \text{... (2)}$$

Equating the two equations,

$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_f} \quad \text{... (3)}$$

$$\boxed{V_o = -C_1 R_f \frac{d V_{in}}{dt}} \quad \text{... (4)}$$

The equation shows that the output is $C_1 R_f$ times the differentiation of the input and product $C_1 R_f$ is called **time constant of the differentiator.**

The negative sign indicates that there is a phase shift of 180° between input and output. The main advantage of such an active differentiator is the small time constant required for differentiation.

By Miller's theorem, the effective resistance between input node A and ground becomes $\frac{R_f}{1+A_v} \approx \frac{R_f}{A_v}$ where A_v is the gain of the op-amp which is very large. Hence effective R_f becomes very very small and hence the condition $R_f C_1 << T$ gets satisfied at all the frequencies.

In practice a resistance $R_{comp} = R_f$ is connected to the noninverting terminal to provide the bias compensation. This is shown in the Fig. 6.51.

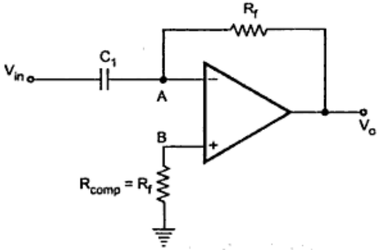


Fig. 6.51 Differentiation with bias compensation

6.22.2 Input and Output Waveforms

Let us study the output waveforms, for various input signals.

For simplicity of understanding, assume that the values of R_f and C_1 are selected to have time constant ($R_f C_1$) as unity.

i) Step input signal

Let the input waveform is of step type with a magnitude of A units. Mathematically it is expressed as,

$$\boxed{V_{in}(t) = A \quad \text{for} \quad t \geq 0} \qquad \ldots (5)$$

Now mathematically, the output of the differentiator must be,

$$\boxed{V_o(t) = -\frac{dV_{in}}{dt} = -\frac{d(A)}{dt} = 0} \qquad \ldots (6)$$

This is because A is constant.

Actually the step input takes a finite time to rise from 0 to A volts.

Due to this finite time, the differentiator output is not zero but appears in the form of a spike at t = 0.

As the circuit acts as an inverting differentiator, the negative going spike or impulse appears at t = 0 and after that output remains zero.

Both input and output waveforms of the differentiator with a step input, are shown in the Fig. 6.52.

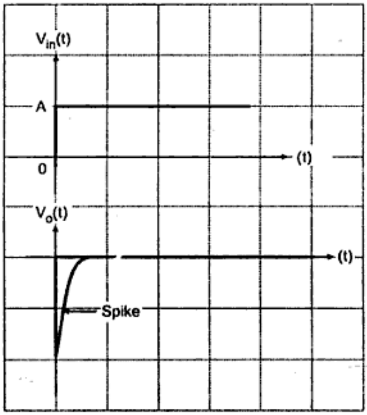


Fig. 6.52 Input and output for step input

ii) Square wave input signal

The square wave is made of steps i.e. step of A volts from t = 0 to t = T/2, while a step of –A volts from t = T/2 to t = T and so on.

Mathematically it can be expressed as,

$$\boxed{\begin{aligned} V_{in}(t) &= A \qquad 0 < t < T/2 \\ &= -A \quad T/2 < t < T \end{aligned}} \qquad \ldots (7)$$

The differentiator behaves similar to its behaviour to step input.

For positive going impulse, the output shows negative going impulse and for negative going input, the output shows positive going impulse.

Hence the total output for the square wave input is in the form of train of impulses or spikes.

The input and output waveforms are shown in the Fig. 6.53.

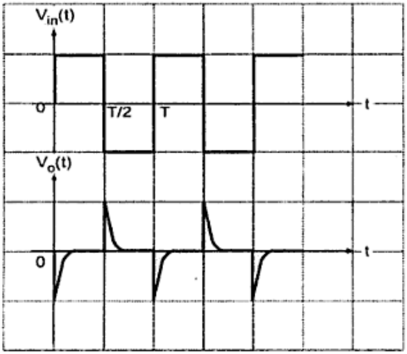


Fig. 6.53 Input and output for square wave input

iii) Sine wave input

Let the input waveform be purely sinusoidal with a frequency of ω rad/sec. Mathematically it can be expressed as,

$$\boxed{V_{in}(t) = V_m \sin \omega t} \qquad \ldots (8)$$

where V_m is the amplitude of the sine wave and T is the period of the waveform.

Let us find out the expression for the output.

6.22.3 Applications of Practical Differentiator

The practical differentiator circuits are most commonly used in :

i) In the wave shaping circuits to detect the high frequency components in the input signal.

ii) As a rate-of-change detector in the FM demodulators.

The differentiator circuit is avoided in the analog computers.

Examples with Solutions

➡ **Example 6.16 :** *The two input terminals of an op-amp are connected to voltage signals of strengths 745 μV and 740 μV respectively. The gain of the op-amp in differential mode is* 5×10^5 *and CMRR is 80 dB. Calculate the output voltage and % error due to common mode.* **(UPTU, May-2003)**

Solution : CMRR = 80 dB, $V_1 = 745\ \mu V$, $V_2 = 740\ \mu V$, $A_d = 5\times10^5$

$$\text{CMRR in dB} = 20 \text{ Log } \frac{A_d}{A_c}$$

$$\therefore \quad 80 = 20 \text{ Log } \frac{5\times10^5}{A_c} \quad \text{i.e. } 10000 = \frac{5\times10^5}{A_c}$$

$$\therefore \quad A_c = 50 \qquad \text{... Common mode gain}$$

$$\therefore \quad \text{Output} = A_dV_d + A_cV_c \qquad \text{where } V_c = \frac{V_1+V_2}{2},\ V_d = V_1 - V_2$$

$$= 5\times10^5\,[745-740]\times10^{-6} + 50\times\left[\frac{745+740}{2}\right]\times10^{-6}$$

$$= \mathbf{2.5371\ V}$$

Ideally output must be $A_dV_d = 2.5$ V

$$\therefore \quad \%\ \text{error} = \frac{2.5371-2.5}{2.5}\times100 = \mathbf{1.484\ \%}$$

➡ **Example 6.17 :** *For a given op-amp, CMRR =* 10^4 *and* $A_d = 10^5$*, find its common mode gain.* **(UPTU, May-2004)**

Solution : CMRR = 10^4, $A_d = 10^5$.

$$\text{CMRR} = \frac{A_d}{A_c} \quad \text{i.e.} \quad A_c = \frac{A_d}{\text{CMRR}}$$

$$\therefore \quad A_c = \frac{10^5}{10^4} = \mathbf{10} \qquad \text{... Common mode gain}$$

Example 6.18 : *Design a noninverting amplifier circuit which is capable of providing a voltage gain of 15. Assume ideal op-amp and resistances used should not exceed 30 kΩ .*

(UPTU, May-2004)

Solution :

$$A_{CL} = 15$$

$$A_{CL} = 1+\frac{R_f}{R_1} \quad \text{i.e.} \quad 15 = 1+\frac{R_f}{R_1}$$

$$\therefore \quad \frac{R_f}{R_1} = 14 \quad \text{i.e.} \quad R_f = 14\,R_1$$

Choose $R_1 = 1\ \text{k}\Omega$ i.e. $R_f = 14\ \text{k}\Omega$

The designed circuit is shown in the Fig. 6.55.

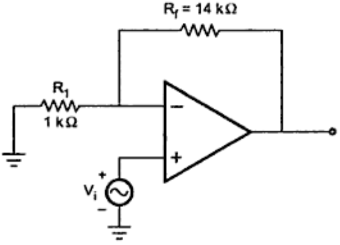


Fig. 6.55

Example 6.19 : *Find the output voltage of the following circuit.*

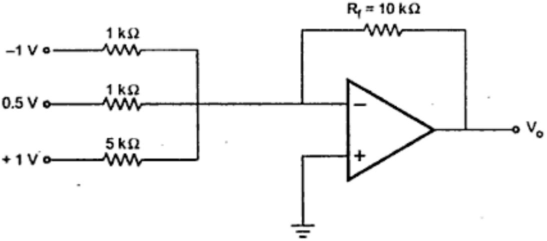


Fig. 6.56

(UPTU, Dec.-2005)

Solution : This is inverting summer

$$V_o = -\left(\frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2+\frac{R_f}{R_3}V_3\right)$$

$$= -\left[\frac{10\times10^3}{1\times10^3}\times(-1)+\frac{10\times10^3}{1\times10^3}\times0.5+\frac{10\times10^3}{5\times10^3}\times1\right]$$

$$= -[-10+5+2] = \mathbf{+\,3\ V}$$

➠ **Example 6.20 :** *Calculate the output voltage of an OP-AMP summing amplifier for the following sets of voltages and resistors.*

Use $R_f = 1M\Omega$ in all cases. **(UPTU, May-2007)**

a) $V_1 = +1$ V, $V_2 = +2$ V, $V_3 = +3$ V

$R_1 = 500$ kΩ, $R_2 = 1$ MΩ, $R_3 = 1$ MΩ

b) $V_1 = -2$ V, $V_2 = +3$ V, $V_3 = +1$ V

$R_1 = 200$ kΩ, $R_2 = 500$ kΩ, $R_3 = 1$ MΩ

Solution : The output of an op-amp summing amplifier is given by,

(a)

$$V_o = \left[\frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2+\frac{R_f}{R_3}V_3\right]$$

$$V_o = -\left[\frac{1\times10^6}{500\times10^3}\times1+\frac{1\times10^6}{1\times10^6}\times2+\frac{1\times10^6}{1\times10^6}\times3\right]$$

$$= -\,[2+2+3] \quad = \mathbf{-\,7\ V}$$

(b)

$$V_o = -\left[\frac{1\times10^6}{200\times10^3}\times(-2)+\frac{1\times10^6}{500\times10^3}\times3+\frac{1\times10^6}{1\times10^6}\times1\right]$$

$$= -\,[-10+6+1] = \mathbf{+3\ V}$$

Review Questions

1. *What is an op-amp? Give its symbol and state its various terminals.*
2. *What is an ideal differential amplifier ? What is differential gain and common mode gain of a differential amplifier ?*
3. *What is CMRR ? Derive its expression.*
4. *Explain the ideal characteristics of an op-amp.*
5. *Write a note on salient features of an ideal op-amp.*
6. *Draw and explain the voltage transfer characteristics of open-loop configuration of op-amp.*

7. *Draw and explain equivalent circuit of practical op-amp.*
8. *What is input offset voltage ?*
9. *Define PSRR. State its importance*
10. *Define slew rate. What is its significance ?*
11. *What is an operational amplifier ? Draw and explain its block diagram.*
12. *Draw and explain the pin diagram of IC741 op-amp.*
13. *Explain the following parameters of an op-amp and state their typical values for IC 741 op-amp :*
    i) Input offset voltage ii) Input offset current
    iii) Input bias current iv) PSRR v) CMRR
    vi) Slew rate vii) Input Impedance viii) Output impedance
    ix) Band width x) Open loop voltage gain
14. *Explain the following parameters of an op-amp and write down the typical values for IC741:*
    i) Input offset voltage ii) Input offset current iii) Input bias current iv) P.S.R.R.
15. *Explain virtual short and virtual ground property of an op-amp.*
16. *Explain the term 'Virtual Ground' in op-amp.*
17. *Draw a circuit diagram for inverting amplifier (closed loop) using op-amp and obtain the expression for its gain. Draw the input and output waveforms, assuming input to be sinusoidal and of low value.*
18. *Derive the expression for the gain of op-amp used as noninverting amplifier.*
19. *Operational Amplifier Inverting and Noninverting closed-loop configurations.*
    i) Draw the neat circuit diagram with standard nomenclature for components used for the above configurations.
    ii) Explain above circuits with reference to feedback, input/output phase, and gain.
    iii) State the expressions for voltage gain for the above circuits.
20. *Compare inverting and noninverting amplifiers.*
21. *What is unity gain buffer ? Draw its circuit diagram.*
22. *Draw and explain the inverting summer circuit using an op-amp.*
23. *Draw and explain the noninverting summer circuit using an op-amp.*
24. *The three voltages V_1, V_2 and V_3 are to be added without a phase shift. Suggest suitable op-amp circuit and derive expression for its output voltage.*
25. *Explain the circuit diagram for obtaining $V_o = V_1 + V_2$.*
26. *Draw the circuit diagram and explain the working of difference amplifier.*
27. *Draw the circuit diagram of an op-amp integrator and derive an expression for an output voltage.*
28. *Draw the circuit diagram of the op-amp differentiator and derive an expression for an output voltage.*

❑❑❑

7

Switching Theory and Logic Design

7.1 Number Systems

Number system is a basis for counting various items. On hearing the word 'number', all of us immediately think of the familiar decimal number system with its 10 digits : 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.

Modern computers communicate and operate with binary numbers which use only the digits 0 and 1. Let us consider decimal number 18. This number is represented in binary as 10010. In the example, if decimal number is considered, we require only two digits to represent the number, whereas if binary number is considered we require five digits. Therefore we can say that, when decimal quantities are represented in the binary form, they take more digits. For large decimal numbers people have to deal with very large binary strings and therefore, they do not like working with binary numbers. This fact gave rise to three new number systems : Octal, Hexadecimal and Binary Coded Decimal (BCD). These number systems represent binary number in a compressed form. Therefore, these number systems are now widely used to compress long strings of binary numbers.

In this chapter, we discuss binary, octal, hexadecimal, and BCD number systems, and we will see how to convert from decimal to binary, octal and hexadecimal, and vice versa. In the later section of this chapter we are going to see binary, hexadecimal, Excess-3 and BCD arithmetic.

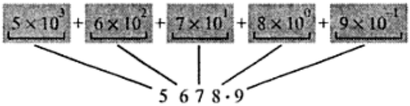
7.1.1 Decimal Number System

Before considering any number system, let us consider familiar decimal number system. In decimal number system we can express any decimal number in units, tens, hundreds, thousands and so on. When we write a decimal number say, 5678.9, we know it can be represented as

$$5000 + 600 + 70 + 8 + 0.9 = 5678.9$$

The decimal number 5678.9 can also be written as 5678.9_{10}, where the 10 subscript indicates the radix or base.

In power of 10, we can write as


$5 \times 10^3 + 6 \times 10^2 + 7 \times 10^1 + 8 \times 10^0 + 9 \times 10^{-1}$
5 6 7 8 · 9

This says that, the position of a digit with reference to the decimal point determines its value/weight. The sum of all the digits multiplied by their weights gives the total number being represented. The leftmost digit, which has the greatest weight is called the **most significant digit** and the rightmost digit, which has the least weight, is called the **least significant digit**. Fig. 7.1 shows decimal digit and its weights expressed as a power of 10.

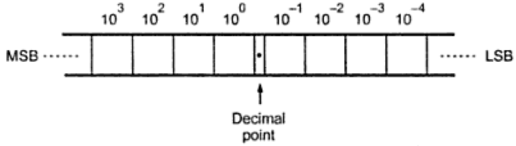

10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
MSB ······
······ LSB
Decimal point

Fig. 7.1 Decimal position values as powers of 10

Example 7.1 : *Represent decimal number 98.72 in power of 10.*

Solution : $N = 9 \times 10^1 + 8 \times 10^0 + 7 \times 10^{-1} + 2 \times 10^{-2}$

The digit 9 has a weight of 10, the digit 8 has a weight of 1, the digit 7 has a weight of 1/10 and the digit 2 has a weight of 1/100.

7.1.2 Binary Number System

We know that decimal system with its ten digits is a base-ten system. Similarly, binary system with its two digits is a base-two system. The two binary digits (bits) are 1 and 0. Like digital system, in binary system each binary digit commonly known as bit, has its own value or weight. However in binary system weight is expressed as a power of 2, as shown in Fig. 7.2.

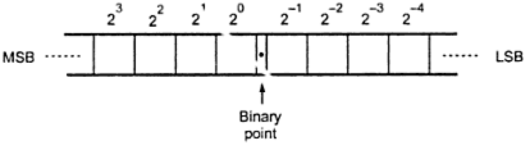

2^3
2^2
2^1
2^0
2^{-1}
2^{-2}
2^{-3}
2^{-4}
MSB ······
······ LSB
Binary point

Fig. 7.2 Binary position values as a power of 2

Example 7.2 : *Represent binary number 1101.101 in power of 2 and find its decimal equivalent.*

Solution : Representing given binary number in power of 2 we have,

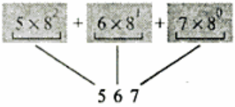
$$\begin{aligned} N &= 1\times 2^3 + 1\times 2^2 + 0\times 2^1 + 1\times 2^0 + 1\times 2^{-1} \\ &\quad + 0\times 2^{-2} + 1\times 2^{-3} \\ &= 8 + 4 + 0 + 1 + 0.5 + 0 + 0.125 \\ &= \mathbf{13.625_{10}} \end{aligned}$$

7.1.3 Octal Number System

We know that the base of the decimal number system is 10 because it uses the digits 0 to 9, and the base of binary number system is 2 because it uses digits 0 and 1. The octal number system uses first eight digits of decimal number system : 0, 1, 2, 3, 4, 5, 6, and 7. As it uses 8 digits, its base is 8.

Example 7.3 : *Represent octal number 567 in power of 8 and find its decimal equivalent.*

Solution : The given octal number 567 can be represented in power of 8 as



$$\begin{aligned} &= 5\times 64 + 6\times 8 + 7\times 1 \\ &= 320 + 48 + 7 \\ &= \mathbf{375_{10}} \end{aligned}$$

7.1.4 Hexadecimal Number System

The hexadecimal number system has a base of 16 having 16 digits : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F. It is another number system that is particularly useful for human communications with a computer. Although it is somewhat more difficult to interpret than the octal number system, it has become the most popular. Since its base is a power of 2 (2^4), it is easy to convert hexadecimal numbers to binary and vice versa.

Table 7.1 shows the relationship between decimal, binary and hexadecimal. Note that each hexadecimal digit represents a group of four binary digits, called nibbles, that are fundamental parts of larger binary words.

Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Table 7.1 Relation between decimal, binary and hexadecimal numbers

➡ **Example 7.4 :** *Represent hexadecimal number 3FD in power of 16 and find its decimal equivalent.*

Solution : The given hexadecimal number $3FD_{16}$ can be represented in power of 16.

$$\underbrace{3\times16^{2}}_{3}+\underbrace{F\times16^{1}}_{F}+\underbrace{D\times16^{0}}_{D}$$

$$= 3\times256 + F(15)\times16 + D(13)\times1$$

$$= 768 + 240 + 13$$

$$= 1021_{10}$$

7.1.5 Counting in Radix (Base) r

In previous sections we have seen number systems with radix (base) r equal to 10, 2, 8 and 16. Each number system has r set of characters. For example, in decimal number system r equals to 10 has 10 characters from 0 to 9, in binary number system r equals to 2 has 2 characters 0 and 1 and so on. In general we can say that, a number represented in radix r, has r characters in its set and r can be any value. This is illustrated in Table. 7.2.

Radix (Base) r	Characters in set
2 (Binary)	0, 1
3	0, 1, 2
4	0, 1, 2, 3
:	
:	
7	0, 1, 2, 3, 4, 5, 6
8 (Octal)	0, 1, 2, 3, 4, 5, 6, 7
:	
:	
10 (Decimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9
:	
:	
16 (Hexadecimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Table 7.2 Radix and character set

➠ **Example 7.5 :** *Find the decimal equivalent of* $(231.23)_4$

Solution :

$$N = 2 \times 4^2 + 3 \times 4^1 + 1 \times 4^0 + 2 \times 4^{-1} + 3 \times 4^{-2}$$

$$= 32 + 12 + 1 + 0.5 + 0.1875$$

$$= 45.6875_{10}$$

➠ **Example 7.6 :** *Count from 0 to 9 in radix 5.*

Solution : The Table 7.2 indicates that radix 5 has 5 characters. A count sequence from 0 decimal to 9 decimal is

00, 01, 02, 03, 04, 10, 11, 12, 13, 14.

7.2 Conversion of Bases

The human beings use decimal number system while computer uses binary number system. Therefore, it is necessary to convert decimal number into its equivalent binary while feeding number into the computer and to convert binary number into its decimal equivalent while displaying result of operation to the human beings. However, dealing with a large quantity of binary numbers of many bits is inconvenient for human beings. Therefore, octal and hexadecimal numbers are used as a shorthand means of expressing large binary numbers. But it is necessary to keep in mind that the digital circuits and systems work strictly in binary; we are using octal and hexadecimal only as a convenience for the operators of the system.

Before going to see conversions between binary, octal and hexadecimal numbers we see the number of digits in several number systems. Table 7.3 shows the decimal, binary, octal and hexadecimal numbers.

Decimal	Binary	Octal	Hexadecimal
0	0 0 0 0	0	0
1	0 0 0 1	1	1
2	0 0 1 0	2	2
3	0 0 1 1	3	3
4	0 1 0 0	4	4
5	0 1 0 1	5	5
6	0 1 1 0	6	6
7	0 1 1 1	7	7
8	1 0 0 0	10	8
9	1 0 0 1	11	9
10	1 0 1 0	12	A
11	1 0 1 1	13	B
12	1 1 0 0	14	C
13	1 1 0 1	15	D
14	1 1 1 0	16	E
15	1 1 1 1	17	F

Table 7.3 Decimal, binary, octal and hexadecimal numbers

7.2.1 Binary to Octal Conversion

We know that base for octal numbers is 8 and the base for binary numbers is 2. The base for octal number is the third power of the base for binary numbers. Therefore, by grouping 3 digits of binary numbers and then converting each group digit to its octal equivalent we can convert binary number to its octal equivalent.

➡ **Example 7.7 :** *Convert* $(1\ 1\ 1\ \ 1\ 0\ 1\ \ 1\ 0\ 0)_2$ *to octal equivalent.*

Solution :

111	101	100
7	5	4

$\therefore$ Octal number = $(754)_8$

7.2.2 Octal to Binary Conversion

Conversion from octal to binary is a reversal of the process explained in the previous section. Each digit of the octal number is individually converted to its binary equivalent to get octal to binary conversion of the number.

➡ **Example 7.8 :** *Convert* $(634)_8$ *to binary.*

Solution :

6	3	4
110	011	100

$\therefore$ Binary number = **110 011 100**

➡ **Example 7.9 :** *Convert* $(725.63)_8$ *to binary.*

Solution :

7	2	5	•	6	3
111	010	101	•	110	011

$\therefore$ Binary number = **111010101 . 110 011**

7.2.3 Binary to Hexadecimal Conversion

We know that base for hexadecimal numbers is 16 and the base for binary numbers is 2. The base for hexadecimal number is the fourth power of the base for binary numbers. Therefore, by grouping 4 digits of binary numbers and then converting each group digit to its hexadecimal equivalent we can convert binary number to its hexadecimal equivalent.

➡ **Example 7.10 :** *Convert* $(1\,1\,0\,1\,1\,0\,0\,0\ \ 1\,0\,0\,1\ \ 1\,0\,1\,1)_2$ *to hexadecimal equivalent.*

Solution :

1 1 0 1	1 0 0 0	1 0 0 1	1 0 1 1
D	8	9	B

$\therefore$ Hexadecimal number = $(\text{D8 9B})_H$

7.2.4 Hexadecimal to Binary Conversion

Conversion from hexadecimal to binary is a reversal of the process explained in the previous section. Each digit of the hexadecimal number is individually converted to its binary equivalent to get hexadecimal to binary conversion of the number.

Example 7.11 : *Convert* $(3FD)_H$ *to binary.*

Solution :

3	F	D
0011	1111	1101

$\therefore$ Binary number = **0011 1111 1101**

Example 7.12 : *Convert* $(5A9.B4)_H$ *to binary.*

Solution :

5	A	9	•	B	4
0101	1010	1001	•	1011	0100

$\therefore$ Binary number = **0101 1010 1001 . 1011 0100**

7.2.5 Octal to Hexadecimal Conversion

The easiest way to convert octal number to hexadecimal number is given below.

1. Convert octal number to its binary equivalent.
2. Convert binary number to its hexadecimal equivalent.

Example 7.13 : *Convert* $(615)_8$ *to its hexadecimal equivalent.*

Solution :

Step 1 : Octal to binary

6	1	5
110	001	101

$\therefore$ Binary number = 110001101

Step 2 : Binary to hexadecimal

0 0 0 1	1 0 0 0	1 1 0 1
1	8	D

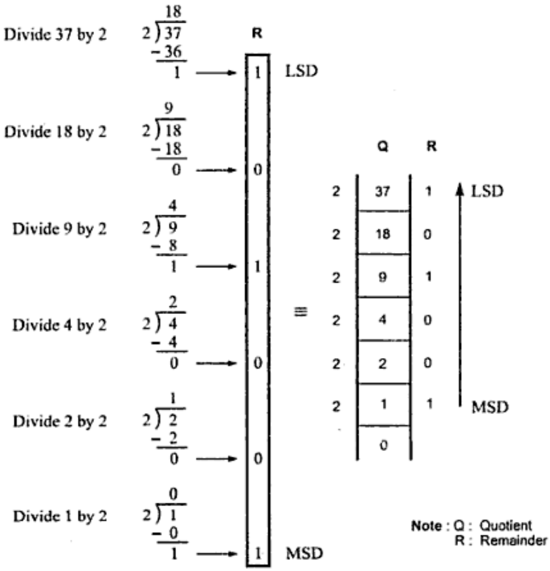
$\therefore$ Hexadecimal number = $\mathbf{18D_H}$

Successive Division for Integer Part Conversion

In this method we repeatedly divide the integer part of the decimal number by r (the new radix) until quotient is zero. The remainder of each division becomes the numeral in the new radix. The remainders are taken in the reverse order to form a new radix number. This means that the first remainder is the least significant digit (LSD) and the last remainder is the most significant digit (MSD) in the new radix number. This procedure is illustrated in following examples.

➠ **Example 7.20 :** *Convert decimal number 37 to its binary equivalent.*

Solution : Here r is 2

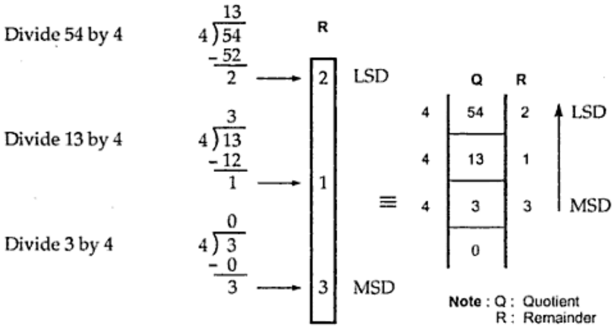

Divide 37 by 2
18
2)37
−36
1
R
1
LSD
Divide 18 by 2
9
2)18
−18
0
0
Divide 9 by 2
4
2)9
−8
1
1
Divide 4 by 2
2
2)4
−4
0
0
Divide 2 by 2
1
2)2
−2
0
0
Divide 1 by 2
0
2)1
−0
1
1
MSD
≡
Q
R
2 37 1
2 18 0
2 9 1
2 4 0
2 2 0
2 1 1
0
LSD
MSD

Note : Q : Quotient
R : Remainder

Binary equivalent = **100101_2**

Example 7.23 : *Convert 54_{10} to radix 4.*

Solution : Here r is 4



Note : Q : Quotient
R : Remainder

The conversion is over when quotient is 0, and we get $(312)_4$ as radix 4 equivalent to decimal number 54.

Successive Multiplication for Fractional Part Conversion

Conversion of fractional decimal numbers to another radix number is accomplished using a successive multiplication method. In this method, the number to be converted is multiplied by the radix of the new number, producing a product that has an integer part and a fractional part. The integer part (carry) of the product becomes a numeral in the new radix number. The fractional part is again multiplied by the radix and this process is repeated until fractional part reaches 0 or until the new radix number is carried out to sufficient digits. The integer part (carry) of each product is read downward to represent the new radix number. This is illustrated in following examples.

Example 7.24 : *Convert 0.8125 decimal number to its binary equivalent.*

Solution :

Fraction		Radix		Result			Recorded carries	
0.8125	×	2	=	1.625	=	0.625	with a carry of 1	MSD
0.625	×	2	=	1.25	=	0.25	with a carry of 1	↓
0.25	×	2	=	0.5	=	0.5	with a carry of 0	
0.5	×	2	=	1.0	=	0.0	with a carry of 1	LSD

Reading carries downward we get,

Binary fraction = 0.1101, which is equivalent to 0.8125 decimal.

7.5 Addition Subtraction

7.5.1 Binary Arithmetic

We can relate addition and subtraction operations of numbers by the following relationship :

(± A) – (+B) = (± A) + (–B) and

(± A) – (–B) = (± A) + (+B)

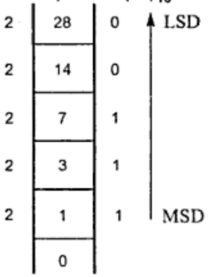
Therefore, we can change subtraction operation to an addition operation by changing the sign of the subtrahend. Hence, the binary addition is the key to binary subtraction, multiplication, and division. So, let us see rules for binary addition.

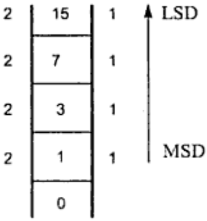
Rules for Binary Addition

A B	Sum	Carry
0 + 0	0	0
0 + 1	1	0
1 + 0	1	0
1 + 1	0	1

7.5.1.1 Binary Arithmetic - Negative Numbers in 1's Complement Form

Case 1 (Both Positive) : Add $(28)_{10}$ and $(15)_{10}$





$\therefore (011100)_2 \rightarrow (28)_{10} \quad (01111)_2 \rightarrow (15)_{10}$

Addition of 28 and 15 :

$$\begin{array}{rccccccccl} & & & 1 & 1 & 1 & & & & \leftarrow \text{Carry} \\ + & 0 & 0 & 1 & 1 & 1 & 0 & 0 & & (28)_{10} \\ & 0 & 0 & 0 & 1 & 1 & 1 & 1 & & (15)_{10} \\ \hline & 0 & 1 & 0 & 1 & 0 & 1 & 1 & & (43)_{10} \end{array}$$

Note : Here, the magnitude of greater number is 5-bit; however, the magnitude of the result is 6-bit. Therefore, the numbers are sign-extended to 7-bits.

Case 2 (Smaller Negative) : Add $(28)_{10}$ and $(-15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

$\therefore$ $(10000)_2 \rightarrow$ 1's complement of 15

Addition of 28 and – 15 :

	+	0	1	1	1	0	0	$(28)_{10}$
Sign extension →		1	1	0	0	0	0	$(-15)_{10}$
Carry →	1	0	0	1	1	0	0	
	└	→	→	→	→	→	1	Add end-around carry
		0	0	1	1	0	1	$(13)_{10}$

Case 3 (Greater Negative) : Add $(-28)_{10}$ and $(15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

$\therefore$ $(100011)_2 \rightarrow (-28)_{10}$

Addition of (– 28) and 15

	+	1	0	0	0	1	1	$(-28)_{10}$	
Sign extension	→	0	0	1	1	1	1	$(15)_{10}$	
		1	1	0	0	1	0	$(-13)_{10}$	Result is in 1's complement form

Verification :	1	1	0	0	1	0		
	0	0	1	1	0	1	→	$(13)_{10}$

Case 4 (Both Negative) : Add $(-28)_{10}$ and $(-15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

$\therefore$ $(10000)_2 \rightarrow$ 1's complement of 15

$(100011)_2 \rightarrow$ 1's complement of 28

Addition of (– 28) and (– 15) :

Sign-extension	→		1	1	0	0	0	1	1	
	+									
Sign-extension	→		1	1	1	0	0	0	0	
Carry		1	1	0	1	0	0	1	1	
									1	Add end-around carry
			1	0	1	0	1	0	0	(– 43) Result is in 1's complement form

Verification :	1	0	1	0	1	0	0		
	0	1	0	1	0	1	1	→	$(43)_{10}$

Note :

- Here, the magnitude of greater number is 5-bit; however, the magnitude of the result is 6-bit. Therefore, the numbers are sign-extended to 7-bits.
- For proper result we suggest to use 1 sign-bit extension to the number having greater magnitude and represent the number having smaller magnitude with extended number of bits.

7.5.1.2 Binary Arithmetic-Negative Numbers in 2's Complement Form

Case 1 (Both Positive) : Add $(28)_{10}$ and $(15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

Addition of 28 and 15

Sign-extension		0	0	1	1	1	0	0	$(28)_{10}$
	+								
Sign-extension		0	0	0	1	1	1	1	$(15)_{10}$
Sign	→	0	1	0	1	0	1	1	$(43)_{10}$

Case 2 (Smaller Negative) : Add $(28)_{10}$ and $(-15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

$\therefore$ $(10001)_2 \rightarrow$ 2's complement of 15

Addition of 28 and – 15

Sign-extension	→	0	0	1	1	1	0	0	$(28)_{10}$
	+								
Sign-extension	→	1	1	1	0	0	0	1	$(-15)_{10}$
Ignore carry	$\boxed{\cancel{1}}$	0	0	0	1	1	0	1	$(13)_{10}$

Case 3 (Greater Negative) : Add $(-28)_{10}$ and $(15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

$\therefore$ $(100100)_2 \rightarrow$ 2's complement of 28

Addition of (– 28) and (15)

Sign-extension	→	1	1	0	0	1	0	0	$(-28)_{10}$	
	+									
Sign-extension	→	0	0	0	1	1	1	1	$(15)_{10}$	
		1	1	1	0	0	1	1	(– 13)	Result is in 2's complement form

Verification :									
		1	1	1	0	0	1	1	
		0	0	0	1	1	0	0	
	+							1	
		0	0	0	1	1	0	1	→ $(13)_{10}$

Case 4 (Both Negative) : Add $(-28)_{10}$ and $(-15)_{10}$

We have $(011100)_2 \rightarrow (28)_{10}$ and

$(01111)_2 \rightarrow (15)_{10}$

$\therefore$ $(100100)_2 \rightarrow$ 2's complement of 28

$(10001)_2 \rightarrow$ 2's complement of 15

Addition of – 28 and – 15

Sign-extension	→	1	1	0	0	1	0	0	(– 28)	
	+									
Sign-extension	→	1	1	1	0	0	0	1	(– 15)	
Ignore carry →	$\boxed{\cancel{1}}$	1	0	1	0	1	0	1	(– 43)	Result is in 2's complement form

The better way to perform octal subtraction is to convert the numbers to binary, perform the subtraction, and convert the result back to octal. However, the complement methods already described for binary can also be used. The 7's and 8's complements for octal numbers are found and used like 1's and 2's complements to perform subtraction.

Subtraction with 7's complement

The 7's complement of an octal number is found by subtracting each digit from 7, as illustrated in Ex. 7.38.

➠ **Example 7.38 :** *Find 7's complement of* 612_8.

Solution :

$$\begin{array}{rccc} & 7 & 7 & 7 \\ - & 6 & 1 & 2 \\ \hline & 1 & 6 & 5_8 \end{array}$$

The steps for octal subtraction using 7's complement method are as given below :

Step 1 : Find 7's complement of subtrahend

Step 2 : Add two octal numbers (first number and 7's complement of the second number)

Step 3 : If carry is produced in the addition, add carry in the least significant bit of the sum; otherwise find 7's complement of the sum as a result with negative sign.

➠ **Example 7.39 :** *Use the 7's complement method of subtraction to compute* $176_8 - 157_8$.

Solution : Step 1 :

$$\begin{array}{rcccl} & 7 & 7 & 7 & \\ - & 1 & 5 & 7 & \\ \hline & 6 & 2 & 0 & \text{7's complement} \end{array}$$

Step 2 :

$$\begin{array}{rccccl} & & 1 & & & \leftarrow \text{carry} \\ & & 1 & 7 & 6 & \\ + & & 6 & 2 & 0 & \\ \hline \text{carry} \rightarrow & 1 & 0 & 1 & 6 & \end{array}$$

Step 3 :

$$\begin{array}{rccc} & 0 & 1 & 6 \\ + & & & 1 \\ \hline & 0 & 1 & 7 \end{array}$$

$\therefore \quad 176_8 - 157_8 \rightarrow 017_8$

Example 7.40 : *Use the 7's complement method of subtraction to compute* $153_8 - 243_8$.

Solution : **Step 1 :**

$$\begin{array}{rrrrl} & 7 & 7 & 7 & \\ - & 2 & 4 & 3 & \\ \hline & 5 & 3 & 4 & \leftarrow \text{7's complement} \\ & 1 & & & \leftarrow \text{carry} \end{array}$$

Step 2 :

$$\begin{array}{rrrrl} & 1 & 5 & 3 & \\ + & 5 & 3 & 4 & \leftarrow \text{7's complement} \\ \hline & 7 & 0 & 7 & \end{array}$$

Step 3 : No carry, hence take 7's complement

$$\begin{array}{rrrrl} & 7 & 7 & 7 & \\ - & 7 & 0 & 7 & \\ \hline & 0 & 7 & 0 & \leftarrow \text{7's complement of sum (– ve sum)} \end{array}$$

$\therefore \quad 153_8 - 243_8 \rightarrow 70_8$

Subtraction With 8's Complement

The 8's complement of an octal number is found by adding a 1 to the least significant bit of the 7's complement of an octal number, as illustrated in the Ex. 1.45.

Example 7.41 : *Find the 8's complement of* 346_8.

Solution :

$$\begin{array}{rrrrl} & 7 & 7 & 7 & \\ - & 3 & 4 & 6 & \\ \hline & 4 & 3 & 1 & \leftarrow \text{7's complement} \\ + & 0 & 0 & 1 & \leftarrow \text{Add 1} \\ \hline & 4 & 3 & 2 & \leftarrow \text{8's complement} \end{array}$$

The steps for octal subtraction using 8's complement method are as given below :

Step 1 : Find 8's complement of subtrahend

Step 2 : Add two octal numbers (first number and 8's complement of the second number).

Step 3 : If carry is produced in the addition it is discarded ; otherwise find 8's complement of the sum as a result with negative sign.

Example 7.44 : *(a)* $3_{16} + 9_{16}$ *b)* $9_{16} + 7_{16}$ *c)* $A_{16} + 8_{16}$.

Solution : a) $3_{16} + 9_{16} = C_{16}$

b) $9_{16} + 7_{16} = (16 - 16)\quad 0_{16}$ carry 1

c) $A_{16} + 8_{16} = (18 - 16)\quad 2_{16}$ carry 1

Note : Sometimes instead of subscript 16, subscript H is used to denote the hexadecimal number.

To obtain the sum of multi-digit hexadecimal numbers, the procedure just described is applied to each column of digits as illustrated in the following example.

Example 7.45 : *Add 3 F 8 $_{16}$ and 5 B 3 $_{16}$*

Solution :

$$\begin{array}{cccl} 1 & & & \leftarrow \text{Carry} \\ 3 & F & 8 & \\ 5 & B & 3 & \\ \hline 8 & (26-16) & B & \end{array} \qquad\qquad \begin{array}{cccl} 1 & & & \leftarrow \text{Carry} \\ 3 & F & 8 & \\ 5 & B & 3 & \\ \hline 9 & A & B_{16} & \end{array}$$

If the decimal sum of several hex digits is 32 or greater, subtract 32 and set carry equal to 2. In general, we can expresss any decimal sum in hexadecimal form by repeatedly subtracting 16 until the result is one of the hex digits through 0 to F. Each time 16 is subtracted the amount of the carry is increased by 1.

7.5.3.2 Subtraction

Hexadecimal subtraction is best accomplished using the complement method. The 15's and 16's complements for hex numbers are found and used like 1's and 2's complements to perform subtraction.

Subtraction with 15's Complement

The 15's complement of a hexadecimal number is found by subtracting each digit from 15, as illustrated in Ex. 7.46.

Example 7.46 : *Find 15's complement of A 9 B_{16}*

Solution :

$$\begin{array}{cccc} & 15 & 15 & 15 \\ - & A & 9 & B \\ \hline & 5 & 6 & 4_{16} \end{array}$$

Solution :

Step 1 :

$$\begin{array}{rccc} & 15 & 15 & 15 \\ - & C & 1 & 4 \\ \hline & 3 & E & B \end{array} \quad \leftarrow \text{15's complement}$$

Step 2 :

$$\begin{array}{rccc} & 1 & 1 & \\ & 6 & 9 & B \\ + & 3 & E & B \\ \hline & A & 8 & 6 \end{array}$$

Step 3 : No carry, hence take 15's complement

$$\begin{array}{rccc} & 15 & 15 & 15 \\ - & A & 8 & 6 \\ \hline & 5 & 7 & 9 \end{array} \quad \leftarrow \text{15's complement of sum}$$

$\therefore \; 69B_{16} - C14_{16} \rightarrow -579_{16}$

Subtraction with 16's complement

The 16's complement of a hexadecimal number is found by adding a 1 to the least significant bit of the 15's complement of a hexadecimal number, as illustrated in the Ex. 7.49.

Example 7.49 : *Find the 16's complement of A 8 C $_{16}$*

Solution :

$$\begin{array}{rccc} & 15 & 15 & 15 \\ - & A & 8 & C \\ \hline & 5 & 7 & 3 \\ + & 0 & 0 & 1 \\ \hline & 5 & 7 & 4 \end{array} \quad \begin{array}{l} \\ \\ \leftarrow \text{15's complement} \\ \leftarrow \text{Add 1} \\ \leftarrow \text{16's complement} \end{array}$$

The steps for hexadecimal subtraction using 16's complement method are as given below :

Step 1 : Find 16's complement of subtrahend

Step 2 :

$$\begin{array}{rccc} & 1 & 1 & \\ & 3 & B & 7 \\ + & 7 & A & C \\ \hline & B & 6 & 3 \end{array}$$

Step 3 : No carry, hence take 16's complement

$$\begin{array}{rcccl} & 15 & 15 & 15 & \\ - & B & 6 & 3 & \\ \hline & 4 & 9 & C & \leftarrow \text{15's complement} \\ + & 0 & 0 & 1 & \leftarrow \text{Add 1} \\ \hline & 4 & 9 & D & \leftarrow \text{16's complement of sum} \end{array}$$

$\therefore 3\,B\,7_{16} - 8\,5\,4_{16} \rightarrow -4\,9\,D_{16}$

7.6 BCD (8-4-2-1)

BCD is an abbreviation for binary-coded-decimal. BCD is a numeric code in which each digit of a decimal number is represented by a separate group of bits. The most common BCD code is 8-4-2-1 BCD, in which each decimal digit is represented by a 4-bit binary number. It is called 8-4-2-1 BCD because the weights associated with 4 bits are 8-4-2-1 from left to right. This means that, bit 3 has weight 8, bit 2 has weight 4, bit 1 has weight 2 and bit 0 has weight 1.

The Table 7.5 shows the 4-bit 8-4-2-1 BCD code used to represent a single decimal digit. The 8-4-2-1 BCD code is so widely used that it is common practice to refer to it simply as BCD.

Decimal	BCD Code			
Digit	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table 7.5 8-4-2-1 BCD code

In multidigit coding, each decimal digit is individually coded with 8-4-2-1 BCD code. For example, 58 in decimal can be encoded in 8-4-2-1 BCD as :

As seen from the above example, in multidigit coding of 8-4-2-1 BCD numbers we require 4-bits per decimal digit. Therefore, total 8-bits are required to encode 58_{10} in 8-4-2-1 BCD. When we represent the same number (58) in binary : 111010_2, we require only 6 digits. This means that, for representing numbers, 8-4-2-1 BCD is less efficient than pure binary number system. The advantage of a BCD code is that it is easy to convert between it and decimal. The principle disadvantage of a BCD, besides its low efficiency, is that arithmetic operations are more complex than they are in pure binary. Let us see the arithmetic operations using 8-4-2-1 BCD.

7.6.1 BCD Addition

The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added.

Sum equals 9 or less with carry 0

Let us consider additions of 3 and 6 in BCD.

$$\begin{array}{rcl} 6 & 0\ 1\ 1\ 0 & \leftarrow \text{BCD for 6} \\ +\ 3 & 0\ 0\ 1\ 1 & \leftarrow \text{BCD for 3} \\ \hline 9 & 1\ 0\ 0\ 1 & \leftarrow \text{BCD for 9} \end{array}$$

The addition is carried out as in normal binary addition and the sum is 1 0 0 1, which is BCD code for 9.

Sum greater than 9 with carry 0

Let us consider addition of 6 and 8 in BCD

$$\begin{array}{rcl} 6 & 0\ 1\ 1\ 0 & \leftarrow \text{BCD for 6} \\ +\ 8 & 1\ 0\ 0\ 0 & \leftarrow \text{BCD for 8} \\ \hline 1\,4 & 1\ 1\ 1\ 0 & \leftarrow \text{Invalid BCD number (1110)} > 9 \end{array}$$

The sum 1 1 1 0 is an invalid BCD number. This has occurred because the sum of the two digits exceeds 9. Whenever this occurs the sum has to be corrected by the addition of six (0110) in the invalid BCD number, as shown below

$$\begin{array}{rcl} 6 & 0\ 1\ 1\ 0 & \leftarrow \text{BCD for 6} \\ +\ 8 & 1\ 0\ 0\ 0 & \leftarrow \text{BCD for 8} \\ \hline 1\ \ 4 & 1\ 1\ 1\ 0 & \leftarrow \text{Invalid BCD number} \\ + & 0\ 1\ 1\ 0 & \leftarrow \text{Add 6 for correction} \\ \hline \underbrace{0\ 0\ 0\ 1}_{1} & \underbrace{0\ 1\ 0\ 0}_{4} & \leftarrow \text{BCD for 14} \end{array}$$

After addition of 6 carry is produced into the second decimal position.

Sum equals 9 or less with carry 1

Let us consider addition of 8 and 9 in BCD

$$\begin{array}{rrl}
8 & 1\ 0\ 0\ 0 & \leftarrow \text{BCD for 8} \\
+\ 9 & 1\ 0\ 0\ 1 & \leftarrow \text{BCD for 9} \\
\hline
17 & 0\ 0\ 0\ 1\ 0\ 0\ 0\ 1 & \leftarrow \text{Incorrect BCD result}
\end{array}$$

In this, case, result (0001 0001) is valid BCD number, but it is incorrect. To get the correct BCD result correction factor of 6 has to be added to the least significant digit sum, as shown.

$$\begin{array}{rrl}
8 & 1\ 0\ 0\ 0 & \leftarrow \text{BCD for 8} \\
+\ 9 & 1\ 0\ 0\ 1 & \leftarrow \text{BCD for 9} \\
\hline
17 & 0\ 0\ 0\ 1\ 0\ 0\ 0\ 1 & \leftarrow \text{Incorrect BCD result} \\
 & +\ 0\ 0\ 0\ 0\ 0\ 1\ 1\ 0 & \leftarrow \text{Add 6 for correction} \\
\hline
 & 0\quad 0\ 0\ 1\ 0\ 1\ 1\ 1 & \leftarrow \text{BCD for 17}
\end{array}$$

Going through these three cases of BCD addition we can summarize the BCD addition procedure as follows :

1. Add two BCD numbers using ordinary binary addition.
2. If four-bit sum is equal to or less than 9, no correction is needed. The sum is in proper BCD form.
3. If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.
4. To correct the invalid sum, add 0110_2 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

Example 7.52 : *Perform each of the following decimal additions in 8-4-2-1 BCD*

a) $\begin{array}{r} 24 \\ +\ 18 \\ \hline \end{array}$ *b)* $\begin{array}{r} 48 \\ +\ 58 \\ \hline \end{array}$ *c)* $\begin{array}{r} 175 \\ +\ 326 \\ \hline \end{array}$ *d)* $\begin{array}{r} 589 \\ +\ 199 \\ \hline \end{array}$

Solution :

```
a)    24   0 0 1 0        0 1 0 0
    + 18   0 0 0 1        1 0 0 0
    ----   -------        -------
      42   0 0 1 1        1 1 0 0     Invalid BCD number 1 1 0 0 > 9
                     +    0 1 1 0     Add 6 for correction
           ----------------------
           0 0 1 1      1 0 0 1 0
         +       1 <---'              Propagate carry to next higher digit
         -----------    ---------
         0   1 0 0        0 0 1 0
b)    48   0 1 0 0        1 0 0 0
    + 58 + 0 1 0 1        1 0 0 0
    ----   ------------------------
     106   1 0 0 1      1 0 0 0 0
                 1 <---'  0 1 1 0     Propagate carry and
             ------------------------ Add 6 for correction
             1 0 1 0        0 1 1 0   1010 > 9 so add 6 for correction
             0 1 1 0
             ------------------------
0 0 0 1      0 0 0 0        0 1 1 0     Corrected sum
c)  175      0 0 0 1    0 1 1 1    0 1 0 1
  + 326    + 0 0 1 1    0 0 1 0    0 1 1 0
  -----    ---------------------------------
    501      0 1 0 0    1 0 0 1    1 0 1 1   1 0 1 1 > 9 so add 6
         +                         0 1 1 0
         -----------------------------------
             0 1 0 0    1 0 0 1  1 0 0 0 1
                              1 <'
      --------------------------------------
             0 1 0 0    1 0 1 0    0 0 0 1   1 0 1 0 > 9 so add 6
                      + 0 1 1 0
         ----------------------------------------
             0 1 0 0  1 0 0 0 0    0 0 0 1
                      1        Propagate carry to next higher digit
         ----------------------------------------
             0 1 0 1    0 0 0 0    0 0 0 1   Corrected sum
```

	1 1 1 1	0 0 1 0	
+	0 1 1 0		Add 6
	1 0 1 0 1	0 0 1 0	
└──→ +		1	End around carry
	0 1 0 1	0 0 1 1	BCD for 53

b) 89	1 0 0 0	1 0 0 1	
− 54	0 1 0 0	0 1 0 1	(45) 9's complement of 54 BCD
35	1 1 0 0	1 1 1 0	
		+ 0 1 1 0	1110 > 9 so add 6
	1 1 0 0	1 0 1 0 0	
	+ 1 ←┘		Propagate carry
	1 1 0 1	0 1 0 0	
	0 1 1 0		Add 6
	1 0 0 1 1	0 1 0 0	
└──→ +		1	End around carry
	0 0 1 1	0 1 0 1	BCD for 35

Subtraction using 10's Complement

The 10's complement of a decimal number is equal to the **9's complement plus 1**. The 10's complement can be used to perform subtraction by adding the minuend to the 10's complement of the subtrahend and dropping the carry. This is illustrated in following examples.

From the above examples we can summarize steps for 10's complement BCD subtraction as follows :

- Find the 10's complement of a negative number
- Add two numbers using BCD addition
- If carry is not generated find the 10's complement of the result.

7.7.2 Other Codes

There are various other weighted 4-bit BCD codes, each developed to have certain properties useful for special applications. Table 7.8 shows these codes, identified by the weights assigned to their bit positions. The $74\bar{2}\bar{1}$ code is somewhat different than the other codes. When 1 occurs in either of the two right most positions means that the weight of that position is subtracted, rather than added, to determine the decimal value.

Decimal	3 3 2 1	4 2 2 1	5 2 1 1	5 3 1 1	5 4 2 1	6 3 1 1	7 4 2 1	$7 4 \bar{2} \bar{1}$
0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 1 1 1
2	0 0 1 0	0 0 1 0	0 0 1 1	0 0 1 1	0 0 1 0	0 0 1 1	0 0 1 0	0 1 1 0
3	0 0 1 1	0 0 1 1	0 1 0 1	0 1 0 0	0 0 1 1	0 1 0 0	0 0 1 1	0 1 0 1
4	0 1 0 1	1 0 0 0	0 1 1 1	0 1 0 1	0 1 0 0	0 1 0 1	0 1 0 0	0 1 0 0
5	1 0 1 0	0 1 1 1	1 0 0 0	1 0 0 0	1 0 0 0	0 1 1 1	0 1 0 1	1 0 1 0
6	1 1 0 0	1 1 0 0	1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 0	0 1 1 0	1 0 0 1
7	1 1 0 1	1 1 0 1	1 0 1 1	1 0 1 1	1 0 1 0	1 0 0 1	1 0 0 0	1 0 0 0
8	1 1 1 0	1 1 1 0	1 1 0 1	1 1 0 0	1 0 1 1	1 0 1 1	1 0 0 1	1 1 1 1
9	1 1 1 1	1 1 1 1	1 1 1 1	1 1 0 1	1 1 0 0	1 1 0 0	1 0 1 0	1 1 1 0

Table 7.8 Weighted 4-bit BCD codes

7.8 Excess-3 Code

Excess-3 code is a modified form of a BCD number. The Excess-3 code can be derived from the natural BCD code by adding 3 to each coded number. For example, decimal 12 can be represented in BCD as 0001 0010. Now adding 3 to each digit we get Excess-3 code as 0100 0101 (12 in decimal).

Table 7.9 shows excess-3 codes to represent single decimal digit

Decimal digit	Excess-3 Code			
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0

Solution :

a)	5		1 0 0 0	Excess-3 for 5
	+ 4	+	0 1 1 1	Excess-3 for 4
	9		1 1 1 1	No carry
		−	0 0 1 1	Subtract 3
			1 1 0 0	Excess-3 for 9

b)	16		0 1 0 0	1 0 0 1	Excess-3 for 16
	+ 29	+	0 1 0 1	1 1 0 0	Excess-3 for 29
	45		1 0 0 1	1 0 1 0 1	
			1 ←┘		Propagate carry
			1 0 1 0	0 1 0 1	
				+ 0 0 1 1	Add 3 to correct 0 1 0 1
			1 0 1 0	1 0 0 0	
		−	0 0 1 1		Subtract 3 to correct 1 0 1 0
			0 1 1 1	1 0 0 0	Excess-3 for 45

c)	103		0 1 0 0	0 0 1 1	0 1 1 0	Excess-3 for 103
	+ 287	+	0 1 0 1	1 0 1 1	1 0 1 0	Excess-3 for 287
	390		1 0 0 1	1 1 1 0	1 0 0 0 0	
				+ 1 ←┘		Propagate carry
			1 0 0 1	1 1 1 1	0 0 0 0	
				+	0 0 1 1	Add 3 to correct 0 0 0 0
			1 0 0 1	1 1 1 1	0 0 1 1	
			0 0 1 1	0 0 1 1		Subtract 3 to correct 1001 and 1111
			0 1 1 0	1 1 0 0	0 0 1 1	Excess-3 for 390

Example 7.58 : *Perform the subtraction* $645_{10} - 319_{10}$ *in excess-3 using the 9's complement method.*

Solution :

Excess-3 for 645 : 1 0 0 1 0 1 1 1 1 0 0 0

Excess-3 for 319 : 0 1 1 0 0 1 0 0 1 1 0 0

9's complement for 319 : 1 0 0 1 1 0 1 1 0 0 1 1

645		1 0 0 1	0 1 1 1	1 0 0 0	
− 319	+	1 0 0 1	1 0 1 1	0 0 1 1	
326		1 0 0 1 0 1	0 0 1 0	1 0 1 1	Propagate carry and
		1 ←		+ 1	add end around carry
		0 0 1 1	0 0 1 0	1 1 0 0	
	+	0 0 1 1	0 0 1 1		Add 3 to correct 0011 and 0010
		0 1 1 0	0 1 0 1	1 1 0 0	
	−			0 0 1 1	Subtract 3 to correct 1001
		0 1 1 0	0 1 0 1	1 0 0 1	Excess-3 for 326

7.8.3 Excess-3 Subtraction using 9's Complement

To perform Excess-3 subtraction using 9's complement we have to -

- Take 9's complement of subtrahend.
- Add excess-3 of minuend and excess-3 of complemented subtrahend.
- If carry = 1 : Result is positive. Add end around carry. If any digit is not valid BCD, subtract 6 from that digit.
- If carry = 0 : Result is negative. Ignore carry. Take 1's complement to get true result. If any digit is not valid BCD, subtract 6 from that digit.

Example 7.59 : *Perform the subtraction* $(645)_{10} - (319)_{10}$ *in excess-3 using the 9's complement method.*

7.9 Gray Code

Decimal Code	Gray code
0	0 0 0 0
1	0 0 0 1
2	0 0 1 1
3	0 0 1 0
4	0 1 1 0
5	0 1 1 1
6	0 1 0 1
7	0 1 0 0
8	1 1 0 0
9	1 1 0 1
10	1 1 1 1
11	1 1 1 0
12	1 0 1 0
13	1 0 1 1
14	1 0 0 1
15	1 0 0 0

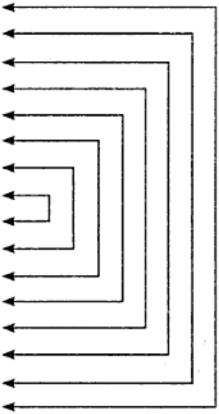


Table 7.10 Gray code

Gray code is a special case of **unit-distance code**. In unit-distance code, bit patterns for two consecutive numbers differ in only one bit position. These codes are also called **cyclic codes.** The Table 7.10 shows the bit patterns assigned for gray code from decimal 0 to decimal 15.

As shown in the Table 7.10 for gray code any two adjacent code groups differ only in one bit position. The gray code is also called **reflected code**. Notice that the two least significant bits for 4_{10} through 7_{10} are the mirror images of those for 0_0 through 3_{10}. Similarly, the three least significant bits for 8_{10} through 15_{10} are the mirror images of those for 0_{10} through 7_{10}. In general, the n least significant bits for 2^n through $2^{n+1} - 1$ are the mirror images of those for 0 through $2^n - 1$. This observation gives us a method for counting in gray code.

Another property of gray code is that the gray-coded number corresponding to the decimal number $2^n - 1$, for any n, differs from gray coded 0 (0000) in one bit position only. For example, for n = 2, 3 and 4, we see that

$$2^2 - 1 = 3_{10} = 0\ 0\ 1\ 0 \text{ in gray}$$

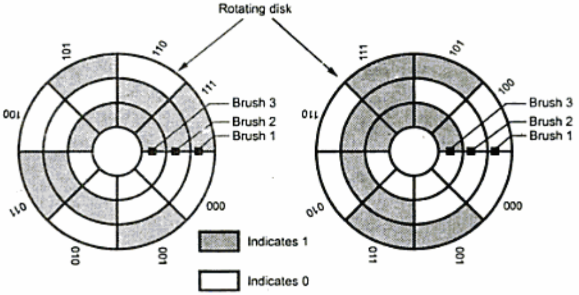
$$2^3 - 1 = 7_{10} = 0\ 1\ 0\ 0 \text{ in gray and}$$

$$2^4 - 1 = 15_{10} = 1\ 0\ 0\ 0 \text{ in gray}$$

Each differ from 0000 in one bit position only. This property places the gray code for the largest n-bit binary number at unit distance from 0.

7.9.1 Advantage of Gray Code

Let us consider an application where 3-bit binary code is provided to indicate position of the rotating disk. As shown in the Fig. 7.5, brushes are used to indicate black and white portions on the disk. When the brushes are on the black portion, they output a 1. When on the white portion, they output a 0.



(a) Binary code (b) Gray code

Fig. 7.5 Position indication using binary and gray codes

Now consider what happens when the brushes are on the 111 sector and almost ready to enter the 000 sector. If one brush is slightly ahead of the other, say the 3^{rd} brush, then the position is indicated by a 011 instead of a 111 or 000. This results, a 180° error in the disk position. Since it is physically impossible to have all the brushes precisely aligned, some error will always be present at the edges of the sectors.

If we use gray code to represent disk position then error due to improper brush alignment can be reduced. This is because the gray code assures that only one bit will change each time the decimal number is incremented. So in 3-bit code, error may occur due to one bit position. Other two bits positions of two adjacent sectors are always same and hence there is no possibility of error. Therefore in 3-bit code probability of error is reduced upto 66%. In case of 4-bit code it is reduced upto 75%.

7.9.2 Gray-to-Binary Conversion

The gray to binary code conversion can be achieved using following steps.

1. The most significant bit of the binary number is the same as the most significant bit of the gray code number. So write it down.
2. To obtain the next binary digit, perform an exclusive-OR-operation between the bit just written down and the next gray code bit. Write down the result.

3. Repeat step 2 until all gray code bits have been exclusive-ORed with binary digits. The sequence of bits that have been written down is the binary equivalent of the gray-code number.

Example 7.61 : *Convert gray code 101011 into its binary equivalent.*

Solution :

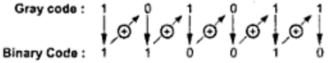


Fig. 7.6

7.9.3 Binary to Gray Conversion

Let us represent binary number as

$B_1\ B_2\ B_3\ B_4\ \dots\ B_n$ and its equivalent gray code as

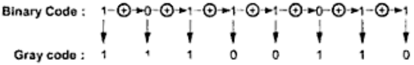
$G_1\ G_2\ G_3\ G_4\ \dots\ G_n$.

With this representation gray code bits are obtained from the binary bits as follows :

$$
\begin{aligned}
G_1 &= B_1 \\
G_2 &= B_1 \oplus B_2 \\
G_3 &= B_2 \oplus B_3 \\
G_4 &= B_3 \oplus B_4 \\
&\ \vdots \\
G_n &= B_{n-1} \oplus B_n
\end{aligned}
$$

Example 7.62 : *Convert 10111011 in binary into its equivalent gray code.*

Solution :



7.10 Five Bit Codes

Table 7.11 shows some 5-bit BCD codes having special characteristics. These special characteristics of the code are useful for error detection. As shown in the Table 7.10, 63210 and two-out-of-five codes have two 1s in every code group. The 63210 code is a weighted

LSBs	MSBs							
	000 (0)	001 (1)	010 (2)	011 (3)	100 (4)	101 (5)	110 (6)	111 (7)
0000 (0)	NUL	DLE	SP	0	@	P	`	p
0001 (1)	SOH	DC_1	!	1	A	Q	a	q
0010 (2)	STX	DC_2	"	2	B	R	b	r
0011 (3)	ETX	DC_3	#	3	C	S	c	s
0100 (4)	EOT	DC_4	$	4	D	T	d	t
0101 (5)	ENQ	NAK	%	5	E	U	e	u
0110 (6)	ACK	SYN	&	6	F	V	f	v
0111 (7)	BEL	ETB	'	7	G	W	g	w
1000 (8)	BS	CAN	(	8	H	X	h	x
1001 (9)	HT	EM	)	9	I	Y	i	y
1010 (A)	LF	SUB	*	:	J	Z	j	z
1011 (B)	VI	ESC	+	;	K	[	k	{
1100 (C)	FF	FS	,	<	L	\	l	|
1101 (D)	CR	GS	-	=	M	J	m	}
1110 (E)	SO	RS	.	>	N	↑	n	~
1111 (F)	SI	US	/	?	O	←	o	DEL

Table 7.12 American standard code for information interchange

Definition of control abbreviations :

ACK	Acknowledge	FS	Form separator
BEL	Bell	GS	Group separator
BS	Backspace	HT	Horizontal tab
CAN	Cancel	LF	Line feed
CR	Carriage return	NAK	Negative acknowledge
DC_1-DC_4	Direct control	NUL	Null
DEL	Delete idle	RS	Record separator
DLE	Data link escape	SI	Shift in
EM	End of Medium	SO	Shift out
ENQ	Enquiry	SOH	Start of heading
EOT	End of transmission	STX	Start text
ESC	Escape	SUB	Substitute
ETB	End of transmission block	SYN	Synchronous idle
ETX	End text	US	Unit separator
FF	Form feed	VT	Vertical tab

Note : The hexadecimal digit representing each bit pattern is shown in parentheses.

1	1			6	6			:	11	8	6
2	2			7	7			<	12	8	4
3	3			8	8			=	8	6	
4	4			9	9			>	0	8	6
								?	0	8	7
								@	8	4	
A	12	1		E	12	5		I	12	9	
B	12	2		F	12	6		J	11	1	
C	12	3		G	12	7		K	11	2	
D	12	4		H	12	8		L	11	3	
M	11	4		Q	11	8		V	0	5	
N	11	5		R	11	9		W	0	6	
O	11	6		S	0	2		X	0	7	
P	11	7		T	0	3		Y	0	8	
				U	0	4		Z	0	9	
[	12	8	2	a	12	0	1	e	12	0	5
\	0	8	2	b	12	0	2	f	12	0	6
]	11	8	2	c	12	0	3	g	12	0	7
^	11	8	7	d	12	0	4	h	12	0	8
–	0	8	5								
`	8	1									
i	12	0	9	m	12	11	4	q	12	11	8
j	12	11	1	n	12	11	5	r	12	11	9
k	12	11	2	o	12	11	6	s	11	0	2
l	12	11	3	p	12	11	7	t	11	0	3
u	11	0	4	{	12	0					
v	11	0	5	|	12	11					
w	11	0	6	}	11	0					
x	11	0	7	~	11	0	1				
y	11	0	8	DEL	12	9	7				
z	11	0	9								

Table 7.14

7.12.1 Fundamental Postulates of Boolean Algebra

The postulates of a mathematical system form the basic assumption from which it is possible to deduce the theorems, laws and properties of the system. Boolean algebra is formulated by a defined set of elements, together with two binary operators, + and · , provided that the following postulates are satisfied.

- **Closure (a) :** Closure with respect to the operator +

  When two binary elements are operated by operator + the result is a unique binary element.

- **Closure (b) :** Closure with respect to the operator · (dot).

  When two binary elements are operated by operator · (dot), the result is a unique binary element.

- An identity element with respect to +, designated by 0 :

  $A + 0 = 0 + A = A$

- An identity element with respect to · , designated by 1 : $A \cdot 1 = 1 \cdot A = A$
- Commutative with respect to + : $A + B = B + A$
- Commutative with respect to · : $A \cdot B = B \cdot A$
- Distributive property of · over + :

  $$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$$

- Distributive property of + over · :

  $$A + (B \cdot C) = (A + B) \cdot (A + C)$$

- For every binary element, there exists complement element. For example, if A is an element, we have $\overline{A}$ is a complement of A. i.e. if $A = 0$, $\overline{A} = 1$ and if $A = 1$, $\overline{A} = 0$.
- There exists at least two elements, say A and B in the set of binary elements such that $A \neq B$.

From the above discussion we can summarize the postulates of Boolean algebra as shown in Table. 7.15.

No.	Postulate	Comment
1.	Result of each operation is either 0 or 1	$1, 0 \in B$
2.	a) $0 + 0 = 0 \quad 0 + 1 = 1 + 0 = 1$ b) $1 \cdot 1 = 1 \quad 1 \cdot 0 = 0 \cdot 1 = 0$	Identify elements 0 for + and 1 for ·
3	a) $(A + B) = (B + A)$ b) $(A \cdot B) = (B \cdot A)$	Commutative law
4.	a) $A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ b) $A + (B \cdot C) = (A + B) \cdot (A + C)$	Distributed law
5	a) $A + \bar{A} = 1$ since $0 + \bar{0} = 0 + 1 = 1$ and $1 + \bar{1} = 1 + 0 = 1$ b) $A \cdot \bar{A} = 0$ since $0 \cdot \bar{0} = 0 \cdot 1 = 0$ and $1 . \bar{1} = 1 \cdot 0 = 0$	Complement

Table 7.15 Fundamental postulates of Boolean algebra

7.12.2 Laws of Boolean Algebra

Three of the basic laws of Boolean algebra are the same as in ordinary algebra : the commutative laws, associative laws, and the distributive law.

Commutative Laws

LAW 1 : A + B = B + A : This states that the order in which the variables are ORed makes no difference in the output. The truth tables are identical. Therefore, A OR B is same as B OR A.

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

≡

B	A	B + A
0	0	0
0	1	1
1	0	1
1	1	1

Table 7.16 Truth table for commutative law for OR gates

LAW 2 : AB = BA : The commutative law of multiplication states that the order in which the variables are ANDed makes no difference in the output. The truth tables are identical. Therefore, A AND B is same as B AND A.

A	B	A B
0	0	0
0	1	0
1	0	0
1	1	1

≡

B	A	B A
0	0	0
0	1	0
1	0	0
1	1	1

Table 7.17 Truth table for commutative law for AND gates

It is important to note that the commutative laws can be extended to any number of variables. For example, since A + B = B + A, it follows that A + B + C = B+A+C, and since A + C = C + A, it is true that B + A + C = B + C + A. Similarly,
ABCD = BACD = BADC = ABDC, and so on.

Associative Laws

LAW 1 : A + (B + C) = (A + B) + C : This law states that in the ORing of several variables, the result is the same regardless of the grouping of the variables. For three variables, A OR B ORed with C is the same as A ORed with B OR C.

A	B	C	A + B	(A + B) + C
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

≡

A	B	C	B + C	A + (B + C)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Table 7.18 Truth table for associative law for OR gates

LAW 2 : (AB) C = A (BC) : The associative law of multiplication states that it makes no difference in what order the variables are grouped when ANDing several variables. For three variables, A AND B ANDed with C is the same as A ANDed with B and C.

A	B	C	AB	(AB) C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0

≡

A	B	C	BC	A (BC)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0

1	1	0	1	0
1	1	1	1	1

1	1	0	0	0
1	1	1	1	1

Table 7.19 Truth table for associative law for AND gates

Distributive Law

LAW : A (B + C) = AB + AC : The distributive law states that ORing several variables and ANDing the result with a single variable is equivalent to ANDing the result with a single variable with each of the several variables and then ORing the products.

A	B	C	(B + C)	A(B + C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

≡

A	B	C	AB	AC	AB + AC
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

Table 7.20 Truth table for distributive law

It is important to note that the distributive property is often used in reverse; i.e., given AB + AC, we replace it by its equivalent, A (B + C). As in ordinary algebra, this process is called **factoring.** We factored A out of the expression AB + AC.

7.12.3 Basic Theorems and Properties

7.12.3.1 Duality

The principle of duality theorem says that, starting with a Boolean relation, you can derive another Boolean relation by

1. Changing each OR sign to an AND sign
2. Changing each AND sign to an OR sign and
3. Complementing any 0 or 1 appearing in the expression

For example : Dual of relation $A + \overline{A} = 1$ is $A \cdot \overline{A} = 0$

Duality is a very important property of Boolean algebra.

7.12.3.2 Basic Theorems

We can define the following theorems using fundamental postulates of Boolean algebra.

Theorem 1(a) $A + A = A$

$$\begin{array}{ccccc} 0 & + & 0 & = & 0 \\ & & & & \\ 1 & + & 1 & = & 1 \end{array} \Rightarrow \quad A + A = A$$

Proof :

$$\begin{aligned} A + A &= (A + A) \cdot 1 && \text{by Postulate : 2(b)} \\ &= (A + A) \cdot (A + \overline{A}) && \text{5(a)} \\ &= A + A\overline{A} && \text{4(b)} \\ &= A + 0 && \text{5(b)} \\ &= A && \text{2(a)} \end{aligned}$$

Theorem 1(b)

$A \cdot A = \quad A$

$$\begin{array}{ccccc} 0 & \cdot & 0 & = & 0 \\ & & & & \\ 1 & \cdot & 1 & = & 1 \end{array} \Rightarrow \quad A \cdot A = A$$

Proof :

$$\begin{aligned} A \cdot A &= A \cdot A + 0 && \text{by postulate : 2(a)} \\ &= AA + A\overline{A} && \text{5(b)} \\ &= A\,(A + \overline{A}) && \text{4(a)} \\ &= A \cdot 1 && \text{5(a)} \\ &= A && \text{2(b)} \end{aligned}$$

Theorem 2(a) :

$A + 1 = \quad 1$

$$\begin{array}{ccccc} 1 & + & 0 & = & 1 \\ & & & & \\ 1 & + & 1 & = & 1 \end{array} \Rightarrow \quad 1 + A = 1 \text{ or } A + 1 = 1$$

Proof :

$$\begin{aligned} A + 1 &= 1 \cdot (A + 1) && \text{by postulate : 2(b)} \\ &= (A + \overline{A})\,(A + 1) && \text{5(a)} \\ &= A + \overline{A} \cdot 1 && \text{4(b)} \\ &= A + \overline{A} && \text{2(b)} \\ &= 1 && \text{5(a)} \end{aligned}$$

Theorem 2(b) :

$$A \cdot 0 = 0$$

$$\begin{array}{l} 0 \cdot \boxed{0} = 0 \\ 0 \cdot \boxed{1} = 0 \end{array} \Rightarrow \quad 0 \cdot A = 0 \text{ or } A \cdot 0 = 0$$

Proof :

$A \cdot 0 =$ 0 by duality of Theorem 2(a)

Theorem 3 :

$$\overline{\overline{A}} = A$$

$$\begin{array}{ccc} \boxed{\overline{\overline{0}}} & = & \boxed{0} \\ \boxed{\overline{\overline{1}}} & = & \boxed{1} \end{array} \quad \overline{\overline{A}} = A$$

Proof : Complement of $\overline{A}$ is A and also $\overline{\overline{A}}$

Theorem 4(a) :

$$A + AB = A$$

Proof :

$$\begin{aligned} A + AB &= A \cdot 1 + AB && \text{by postulate : 2(b)} \\ &= A\,(1 + B) && \text{4(b)} \\ &= A \cdot 1 && \text{2(a)} \\ &= A && \text{2(b)} \end{aligned}$$

Theorem 4(b) :

$$A\,(A + B) = A$$

Proof :

$$\begin{aligned} A\,(A + B) &= A \cdot A + AB && \text{by postulate : 4(a)} \\ &= A + AB && \text{by Theorem : 1(b)} \\ &= A && \text{: 4(a)} \end{aligned}$$

Theorem 5(a) :

$$\begin{aligned} A + \overline{A}B &= A + B \\ &= A + AB + \overline{A}B && \text{by Theorem : 4(a)} \\ &= A + B \cdot (A + \overline{A}) && \text{by Postulate : 4(a)} \\ &= A + B \cdot 1 && \text{: 5(a)} \\ &= A + B && \text{: 2(b)} \end{aligned}$$

Theorem 5(b) :

$$\begin{aligned} A \cdot (\overline{A} + B) &= AB \\ &= (A + AB) \cdot (\overline{A} + B) && \text{by Theorem : 4(a)} \\ &= A\overline{A} + AB + ABB && \text{by Postulate : 4(a)} \\ &= AB + ABB && \text{: 5(b)} \\ &= AB + AB && \text{: 2(b)} \\ &= AB && \text{by Theorem : 1(a)} \end{aligned}$$

The Table 7.21 lists the five basic theorems of Boolean algebra four of its postulates. The postulates and theorems are listed in pairs and designated by part (a) and part (b). One part may be obtained from the other by using principle of duality.

Postulates	**(a)**	**(b)**
Postulate 2	$A + 0 = A$	$A \cdot 1 = A$
Postulate 5	$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$
Postulate 3 (Commutative)	$A + B = B + A$	$AB = BA$
Postulate 4 (Distributive)	$A\,(B + C) = AB + AC$	$A + BC = (A + B)\,(A + C)$
Theorems	**(a)**	**(b)**
Theorem 1 (Idempotency)	$A + A = A$	$A \cdot A = A$

7.12.3.4 Consensus Theorem

In simplification of Boolean expression, an expression of the form $AB+\overline{A}C+BC$ the term BC is redundant and can be eliminated to form the equivalent expression $AB+\overline{A}C$. The theorem used for this simplification is known as consensus theorem and it is stated as

$$AB+\overline{A}C+BC = AB+\overline{A}C$$

The key to recognize the consensus terms is to first find a pair of terms, one of which contains a variable and the other contains its complement. Now we have to find the third term which should contain the remaining variables from pair of terms eliminating selected variable and its complement.

Proof :

$$\begin{aligned} AB+\overline{A}C+BC &= AB+\overline{A}C+(A+\overline{A})BC \\ &= AB+\overline{A}C+AB+\overline{A}C \\ &= AB+\overline{A}C \end{aligned}$$

Example 7.63 : *Solve the given expression using consensus theorem.*

$$\overline{A}\,\overline{B}+AC+B\overline{C}+\overline{B}C+AB$$

Solution :

$$\overline{A}\,\overline{B}+AC+B\overline{C}+\overline{B}C+AB = \overline{A}\,\overline{B}+AC+B\overline{C}+AB$$

$$\overline{A}\,\overline{B}+AC+B\overline{C}+AB = \overline{A}\,\overline{B}+AC+B\overline{C}$$

$$\therefore \quad \overline{A}\,\overline{B}+AC+B\overline{C}+\overline{B}C+AB = \overline{A}\,\overline{B}+AC+B\overline{C}$$

Note : The brackets indicate how the consensus terms are identified.

7.12.3.5 Dual of Consensus Theorem

The dual form of Consensus theorem is stated as

$$(A+B)(\overline{A}+C)(B+C) = (A+B)(\overline{A}+C)$$

Proof :

$$\begin{aligned} (A\overline{A}+AC+\overline{A}B+BC)(B+C) &= A\overline{A}+AC+\overline{A}B+BC \\ (AC+\overline{A}B+BC)(B+C) &= AC+\overline{A}B+BC \\ ABC+\overline{A}BB+BCC+ACC+\overline{A}BC+BCC &= AC+\overline{A}B+BC \\ (A+\overline{A})BC+\overline{A}B+BC+AC &= AC+\overline{A}B+BC \\ \overline{A}B+BC+AC &= AC+\overline{A}B+BC \end{aligned}$$

... Proved

Example 7.64 : *Solved the following Boolean expression using dual of consensus theorem* $(A+B)(\overline{A}+C)(B+C)(\overline{A}+D)(B+D)$.

Solution : $(A+B)(\overline{A}+C)(B+C)(\overline{A}+D)(B+D)$

$= (A+B)(\overline{A}+C)(\overline{A}+D)(B+D)$

$= (A+B)(\overline{A}+C)(\overline{A}+D)$

7.13 Logic Gates

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function. The types of gates available are the NOT, AND, OR, NAND, NOR, exclusive-OR, and the exclusive-NOR. Let us see the standard logic gates : NOT, AND and OR.

7.13.1 NOT Gate (Inverter)

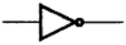


Fig. 7.8 Inverter symbol

The inverter (NOT gate) performs a basic logic function called "inversion" or "complementation". The inverter changes one logic level to its opposite level. In terms of bits, it changes a logic 1 to a logic 0 and a logic 0 to a logic 1. The Fig. 7.8 shows the symbol for the inverter.

The bubble [o] appearing on the output is the negation (inversion) indicator.

Inverter Operation :

When a HIGH level is applied to an inverter input, a LOW level will appear on its output. When a LOW level is applied to its input, a HIGH level will appear on its output. This operation is summarized in the Truth Table 7.24, which indicates the output for each possible input in terms of levels and bits.

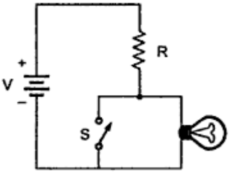
Inverter Truth Table :

Input	Output	Input	Output
LOW	HIGH	0	1
HIGH	LOW	1	0

Table 7.24

Switching Lamp Analogy

The Fig. 7.9 shows the switching lamp analogy for NOT gate. When the switch S is open, the lamp is ON and when the switch S is close, lamp is OFF.

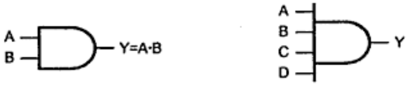


Input	Output
Switch open (Low)	Lamp ON (High)
Switch close (High)	Lamp OFF (Low)

Fig. 7.9 Switching circuit analogy of NOT function

7.13.2 AND Gate

The AND gate performs logical multiplication, more commonly known as the AND function. The AND gate may have two or more inputs and a single output, as indicated by the standard logic symbols shown in the Fig. 7.10.



(a) Two inputs to AND gate

(b) Four inputs to AND gate

Fig. 7.10

AND Operation

Gates with two and four inputs are shown in Fig. 7.10; however, an AND gate can have any number of inputs greater than one. The operation of the AND gate is such that the output is HIGH only when all of the inputs are HIGH. When any of the inputs are LOW, the output is LOW. Hence, the AND gate determines when certain conditions are simultaneously true, as indicated by HIGH levels on all of its inputs, and to produce a HIGH on its output indicating this conditions. The Fig. 7.11 illustrates a two-input AND gate with all four possibilities of input combinations, and the resulting output for each.

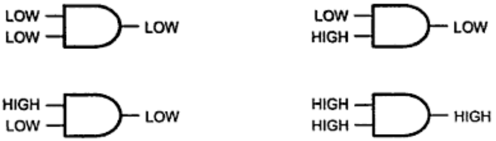


Fig. 7.11 Four possible inputs for two input AND gate and resulting outputs

AND Truth Table

The truth table for a two-input AND gate is shown in Table 7.25. This table can be expanded for any number of inputs. For any AND gate, regardless of the number of inputs, the output is high only when all inputs are HIGH.

Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Table 7.25 Truth table for 2 input AND gate

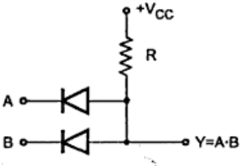


Fig. 7.12 2-input AND gate

Fig. 7.12 shows one way to build a 2-input AND gate. The inputs are labelled A and B, while the output is Y. Let us assume a supply voltage V_{CC} of +5 V. Also we will assume the input voltages are either 0 V (Low) or +5 V (High). With 2 inputs, there are four possible input cases and we will now observe the output for all four input cases.

CASE 1 : A is low and B is low: When both input voltages are low, the cathode of each diode is grounded. Therefore, the positive supply forward-biases both diodes in parallel. Because of this, the output voltage is ideally zero (practically 0.7 V for Si). This means Y is low.

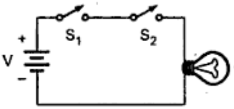
CASE 2 : A is low and B is high : When A is low, the upper diode is forward-biased (ON), and it pulls the output down to a low voltage, i.e. Y = 0. With the B input high, the lower diode goes into reverse bias (OFF).

CASE 3 : A is high and B is low : Because of the symmetry of the circuit, the circuit operation is similar to case 2. But in this case, upper diode is reverse biased (OFF), lower diode is forward biased (ON), and Y is low.

CASE 4 : A is high and B is high : When both inputs are at +5 V, both diodes are reverse biased and there is no current through diodes and resistor R. This pulls up the output Y to the supply voltage. Therefore, Y is high.

Switching Lamp Analogy

The Fig. 7.13 shows the switching lamp analogy for AND gate. It is very clear that the lamp will be ON only when both the switches S_1 and S_2 are closed simultaneously; i.e. only when S_1 AND S_2 are ON simultaneously. When any of two switches is OFF, the lamp is OFF.

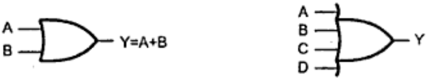


Input		Output
S_1	S_2	
Open (Low)	Open (Low)	Lamp OFF (Low)
Open (Low)	Close (High)	Lamp OFF (Low)
Close (High)	Open (Low)	Lamp OFF (Low)
Close (High)	Close (High)	Lamp ON (High)

Fig. 7.13 Switching circuit analogy of AND function

7.13.3 OR Gate

The OR gate performs logical addition, more commonly known as the OR function. An OR gate has two or more inputs and one output, as indicated by the standard logic symbol in Fig. 7.14, where OR gates with two and four inputs are illustrated. An OR gate produces a HIGH on the output when any of the inputs is HIGH. The output is LOW only when all of the inputs are LOW. Hence, the purpose of an OR gate is to determine when one or more of its inputs are HIGH and to produce a HIGH on its output to indicate this condition.



(a) Two inputs to OR gate (b) Four inputs to OR gate

Fig. 7.14 Four inputs to OR gate

OR Operation

The Fig. 7.15 illustrates the logic operation for a two-input OR gate for all four possible input combinations :

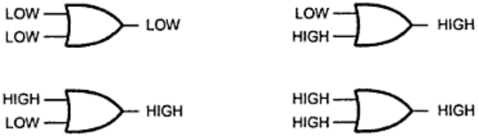
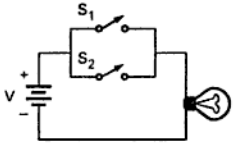


Fig. 7.15 Four possible inputs for two input OR gate and resulting outputs

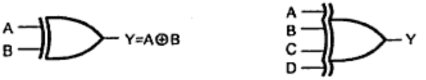


Input		Output
S_1	S_2	
Open (Low)	Open (Low)	Lamp OFF (Low)
Open (Low)	Close (High)	Lamp ON (High)
Close (High)	Open (Low)	Lamp ON (High)
Close (High)	Close (High)	Lamp ON (High)

Fig. 7.17 Switching circuit analogy of OR function

7.13.4 The Exclusive-OR Gate

The EX-OR gate is an abbreviation for Exclusive-OR gate. An EX-OR gate has two or more inputs and one output, as indicated by the standard logic symbol in Fig. 7.18 where EX-OR gates with two and four inputs are shown.



(a) Two input EX-OR

(b) Four input EX-OR

Fig. 7.18

It recognizes only the words that have an odd number of ones. This means that for odd number of ones, output of EX-OR gate is high. The Fig. 7.19 illustrates the logic operation for a two-input EX-OR gate for all four possible input combinations.

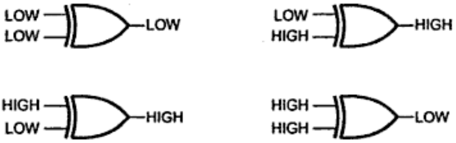


Fig. 7.19 Four possible inputs for two input EX-OR gate and resulting outputs

The Truth Table 7.27 describes the logical operations of the two-input EX-OR gate.

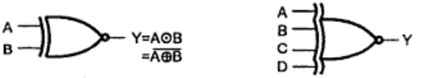
Inputs		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

Table 7.27 Truth table for 2-input EX-OR gate

The truth table can be expanded for any number of inputs, however, regardless of the number of inputs, the output is high only when odd number of inputs are HIGH.

7.13.5 The Exclusive-NOR Gate

The term EX-NOR is a contraction of NOT-X-OR, NOT exclusive OR gate. It is logically equivalent to an EX-OR gate followed by an inverter. An EX-NOR gate has two or more inputs and one output, as indicated by the standard logic symbol in Fig. 7.20 where EX-NOR gates with two and four inputs are shown.



(a) Two input EX-NOR (b) Four input EX-NOR

Fig. 7.20

It recognizes only the words that have an even number of ones and inputs having all zeroes. This means that for even number of ones at the input, or inputs having all zeroes, the output of EX-NOR gate is high. The Fig. 7.21 illustrates the logic operation for a two input EX-NOR gate for all four possible input combinations.

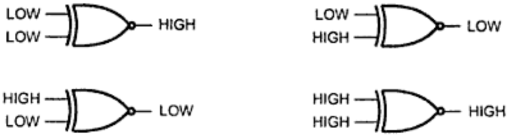


Fig. 7.21 Four possible inputs for two input EX-NOR gate and resulting outputs

The truth table 7.28 describes the logical operations of the two input EX-NOR gate.

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Table 7.28 Truth table for 2-input EX-NOR

The truth table can be expanded for any number of input; however, regardless of the number of inputs, the output is high when even number of inputs are high or when all input are zeroes.

7.13.6 Properties of Exclusive - OR Gate

Property 1 : $A \oplus A = 0$: Output is logic zero when inputs are same.

Property 2 : $A \oplus \overline{A} = 1$: Output is logic 1 when inputs are different.

Property 3 : $A \oplus 1 = \overline{A}$: EX-OR as Inverter.

When one input of EX-OR gate is connected to logic one we get the **complement** of the other input at the output of EX-OR gate.

$$0 \oplus 0 = 0$$

$$0 \oplus 1 = 1$$

$$\boxed{1} \oplus \boxed{0} = \boxed{1}$$

$$\boxed{1} \oplus \boxed{1} = \boxed{0}$$

Input tied to logic 1.

Other input

Output is complement form of other input.

Property 4 : $A \oplus 0 = A$ EX-OR as Non-Inverter

When one input of EX-OR gate is connected to logic 0 we get the **uncomplement** of the other input at the output of EX-OR gate.

Input is Grounded

$0 \oplus 0 = 0$

$0 \oplus 1 = 1$

Output is complement form of other input.

$1 \oplus 0 = 1$

$1 \oplus 1 = 0$

Property 5 : EX-OR as Modulo 2 Adder

The exclusive-OR gate can be used as a modulo 2 adder because its truth table is same as the truth table of modulo 2 adder.

$0 + 0 = 0$ $0 \oplus 0 = 0$

$0 + 1 = 1$ $0 \oplus 1 = 1$

$1 + 0 = 1$ $1 \oplus 0 = 1$

$1 + 1 = 0$ $1 \oplus 1 = 0$

Property 6 : (AB) ⊕ (AC) = A (B ⊕ C)

A	B	C	AB ⊕ AC	A (B ⊕ C)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Property 7 :

If $A \oplus B = C$, then

$A \oplus C = B$

$B \oplus C = A$ and

$A \oplus B \oplus C = 0$

A	B	A ⊕ B = C	A ⊕ C = B	B ⊕ C = A	A ⊕ B ⊕ C = 0
0	0	0	0	0	0
0	1	1	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0

The truth table 7.29 summarizes the logical operation of the two input NAND gate.

Inputs		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 7.29 Truth table for 2-input NAND gate

7.14.2 NOR Gate

The term NOR is a contraction of NOT-OR and implies an OR function with an inverted output. A standard logic symbol for a two-input NOR gate and its equivalent OR gate followed by an inverter is shown in the Fig. 7.24.

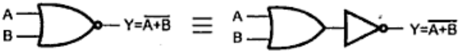


Fig. 7.24 NOR gate symbol and equivalent circuit

Similar to NAND gate, the NOR gate is a universal gate, i.e. NOR gate can be used to construct an AND gate, an OR gate, an inverter, or any combination of these functions.

The logic operation of the NOR gate is that a LOW output occurs when any of its inputs is HIGH. Only when all of its inputs are LOW, the output is HIGH.

The Fig. 7.25 illustrates the logical operation of a two-input NOR gate for all four possible input combinations.

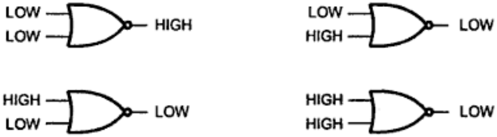


Fig. 7.25 Four possible inputs for two input NOR gate and resulting outputs

A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

≡

A	B	$\overline{AB}$	$\overline{\overline{AB}}$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 7.31 Truth Table

OR Function :

OR function is generated using only NAND gates as follows : We know that Boolean expression for OR gate is

$$Y = A + B$$

$$= \overline{\overline{A}} + \overline{\overline{B}}$$ Rule 9 : $[\overline{\overline{A}} = A]$

$$= \overline{\overline{A} \cdot \overline{B}}$$ DeMorgan's Theorem 1

The above equation is implemented using only NAND gates as shown in the Fig. 7.28.

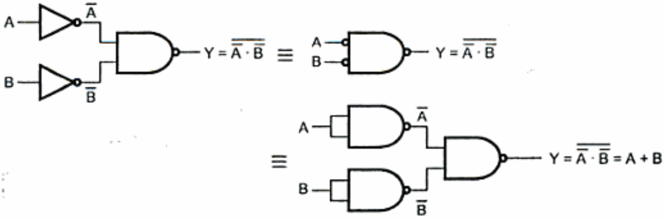

A
$\overline{A}$
B
$\overline{B}$
$Y = \overline{\overline{A} \cdot \overline{B}}$
≡
A
B
$Y = \overline{\overline{A} \cdot \overline{B}}$
A
$\overline{A}$
≡
B
$\overline{B}$
$Y = \overline{\overline{A} \cdot \overline{B}} = A + B$

Fig. 7.28 OR function using only NAND gates

Note : Bubble at the input of NAND gate indicates inverted input.

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

≡

A	B	$\overline{A} \cdot \overline{B}$	$\overline{\overline{A} \cdot \overline{B}}$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Table 7.32 Truth table

NOR Function :

NOR function is generated using only NAND gates as follows : We know that Boolean expression for NOR gate is

$$Y = \overline{A+B}$$

$$= \bar{A} \,.\, \bar{B} \qquad \text{DeMorgan's Theorem 2}$$

$$= \overline{\overline{\bar{A} \cdot \bar{B}}} \qquad \text{Rule 9 : } [\bar{\bar{A}} = A]$$

The above equation is implemented using only NAND gates, as shown in the Fig. 7.29.

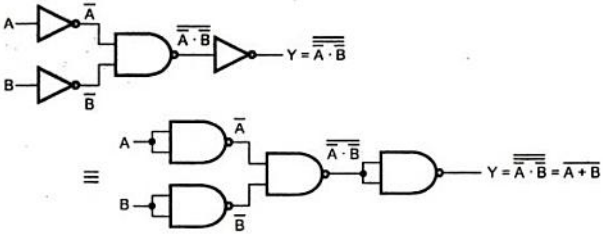

A
$\bar{A}$
B
$\bar{B}$
$\overline{\bar{A} \cdot \bar{B}}$
$Y = \overline{\overline{\bar{A} \cdot \bar{B}}}$
≡
A
$\bar{A}$
B
$\bar{B}$
$\overline{\bar{A} \cdot \bar{B}}$
$Y = \overline{\overline{\bar{A} \cdot \bar{B}}} = \overline{A+B}$

Fig. 7.29 NOR function using only NAND gates

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

≡

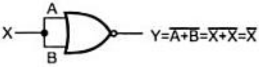
A	B	$\bar{A} \cdot \bar{B}$	$\overline{\bar{A} \cdot \bar{B}}$	$\overline{\overline{\bar{A} \cdot \bar{B}}}$
0	0	1	0	1
0	1	0	1	0
1	0	0	1	0
1	1	0	1	0

Table 7.33 Truth table

7.14.4 Implementation of NOT, AND, OR and NAND Functions using NOR Gate

NOT Function :

An inverter can be made from a NOR gate by connecting all of the inputs together and creating, in effect, a single common input, as shown in Fig. 7.30.



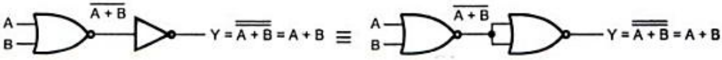
A
X
B
Y=$\overline{A+B}=\overline{X+X}=\overline{X}$

	A	B	$\overline{A+B}$	
X = 0	0	0	1	Y = 1
	0	1	0	
	1	0	0	
X = 1	1	1	0	Y = 0

Fig. 7.30 NOT function using NOR gate

OR Function :

An OR function can be generated using only NOR gates. It can be generated by simply inverting output of NOR gate; i.e. $\overline{\overline{A+B}}$ = A + B. Fig. 7.31 shows the two input OR gate using NOR gates.



A
B
$\overline{A+B}$
Y = $\overline{\overline{A+B}}$ = A + B
≡
A
B
$\overline{A+B}$
Y = $\overline{\overline{A+B}}$ = A + B

Fig. 7.31 OR function using NOR gates

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

≡

A	B	$\overline{A+B}$	$\overline{\overline{A+B}}$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Table 7.34 Truth table

AND Function :

AND function is generated using only NOR gates as follows : We know that Boolean expression for AND gate is

$$Y = A \cdot B$$

$$= \overline{\overline{A}} \cdot \overline{\overline{B}} \qquad \text{Rule 9 : } [\overline{\overline{A}} = A]$$

$$= \overline{\overline{A} + \overline{B}} \qquad \text{DeMorgan's Theorem 2}$$

A	B	$\overline{A\cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

=

A	B	$\bar{A}+\bar{B}$	$\overline{\bar{A}+\bar{B}}$	$\overline{\overline{\bar{A}+\bar{B}}}$
0	0	1	0	1
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0

Table 7.36 Truth table

➠ **Example 7.65 :** *Implement EX-OR gate using only NAND Gates.*

Solution : The Boolean expression for EX-OR gate is : $Y = A\bar{B}+\bar{A}B$

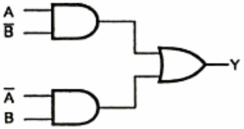

A
$\bar{B}$
$\bar{A}$
B
Y

Fig. 7.34 (a)

We can implement AND-OR logic by using NAND-NAND logic as shown in Fig. 7.34 (b).

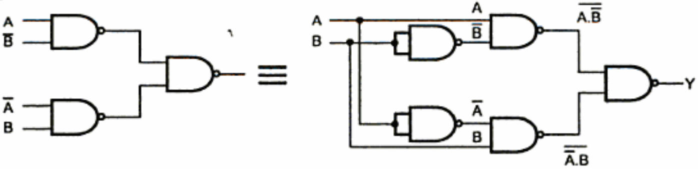

A
$\bar{B}$
$\bar{A}$
B
≡
A
B
A
$\bar{B}$
$\overline{A.\bar{B}}$
$\bar{A}$
B
$\overline{\bar{A}.B}$
Y

Fig. 7.34 (b)

➠ **Example 7.66 :** *Implement EX-NOR gate using only NOR gates.*

Solution : The Boolean expression for EX-NOR gate is :

$$Y = AB+\bar{A}\,\bar{B} = \overline{A\bar{B}+\bar{A}B}$$

$$= \overline{A\bar{B}}\cdot\overline{\bar{A}B} = (\bar{A}+B)\cdot(A+\bar{B})$$

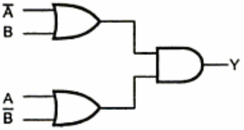

$\bar{A}$
B
A
$\bar{B}$
Y

Fig. 7.35(a)

We can implement OR-AND logic by using NOR-NOR logic, as shown in Fig. 7.35(b).

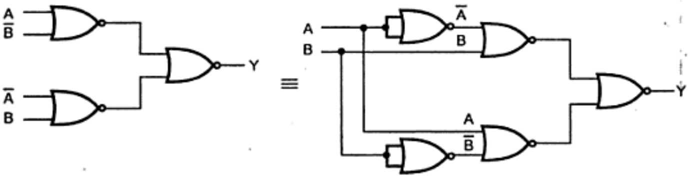

A
$\overline{B}$
$\overline{A}$
B
Y
≡
A
B
$\overline{A}$
B
A
$\overline{B}$
Y

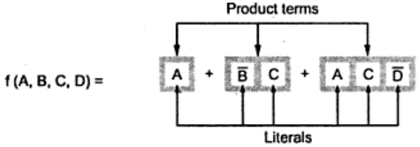
Fig. 7.35 (b)

7.15 Switching Functions / Boolean Functions

Boolean expressions are constructed by connecting the Boolean constants and variables with the Boolean operations. These Boolean expressions are also known as **Boolean formulas**. We use Boolean expressions to describe **Boolean functions**. For example, if the Boolean expression (A + $\overline{B}$) C is used to describe the function f, then Boolean function is written as

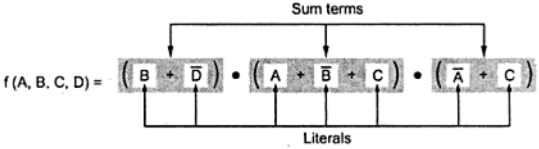
$$f(A, B, C) = (A + \overline{B})\,C \text{ or } f = (A + \overline{B})\,C$$

Based on the structure of Boolean expression, it can be categorized in different formulas. One such categorization are the normal formulas. Let us consider the four-variable Boolean function.


Product terms
f (A, B, C, D) =
A
+
$\overline{B}$
C
+
A
C
$\overline{D}$
Literals

... (1)

In this Boolean function the variables are appeared either in a complemented or an uncomplemented form. Each occurrence of a variable in either a complemented or an uncomplemented form is called a **literal**. Thus, the above Boolean function (1) consists of six literals. They appear in the product terms. A **product term** is defined as either a literal or a product (also called conjunction) of literals. Function 1 contains three product terms, namely, A, $\overline{B}$ C and A C $\overline{D}$. Let us consider another four variable Boolean function


Sum terms
f (A, B, C, D) =
(B + $\overline{D}$)
•
(A + $\overline{B}$ + C)
•
($\overline{A}$ + C)
Literals

... (2)

The above Boolean function consists of seven literals. Here, they appear in the sum terms. A **sum term** is defined as either a literal or a sum (also called disjunction) of literals. Function 2 contains three sum terms, namely, $(B + \overline{D})$, $(A + \overline{B} + C)$ and $(\overline{A} + C)$. These literals and terms are arranged in one of the two forms :

- Sum of product form (SOP) and
- Product of sum form (POS).

7.15.1 Sum of Product Form

The words sum and product are derived from the symbolic representations of the OR and AND functions by + and · (addition and multiplication), respectively. But we realize that these are not arithmetic operators in the usual sense. A product term is any group of literals that are ANDed together. For example, ABC, XY and so on. A sum term is any group of literals that are ORed together such as A + B + C, X + Y and so on. A sum of products (SOP) is a group of product terms ORed together. Some examples of this form are :

Sum

1. $f(A, B, C) = A\,B\,C + A\,\overline{B}\,\overline{C}$

Product terms

Sum

2. $f(P, Q, R, S) = \overline{P}\,Q + Q\,R + R\,S$

Product terms

Each of these sum of products expressions consist of two or more product terms (AND) that are ORed together. Each product term consists of one or more literals appearing in either complemented or uncomplemented form. For example, in the sum of products expression $ABC + A\overline{B}\overline{C}$, the first product term contains literals A, B and C in their uncomplemented form. The second product term contains B and C in their complemented (inverted) form. The sum of product form is also known as **disjunctive normal form** or **disjunctive normal formula.**

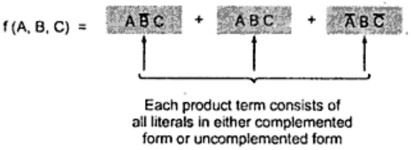

f (A, B, C) = $A\bar{B}C + ABC + \bar{A}B\bar{C}$
Each product term consists of
all literals in either complemented
form or uncomplemented form

Fig. 7.36 Standard SOP form

7.16.2 Standard POS Form or Maxterm Canonical Form

If each term in POS form contains all the literals then the POS form is known as **standard or canonical POS form**. Each individual term in the standard POS form is called **maxterm**. Therefore, canonical POS form is also known as **maxterm canonical form**. In other words, we can say that a product of sums is a standard or canonical product of sums if every sum term involves every literal or its complement. One standard product of sums expression is as shown in Fig. 7.37.

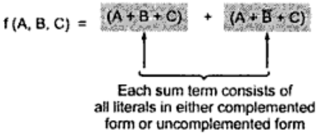

f (A, B, C) = $(A + B + C) + (A + \bar{B} + C)$
Each sum term consists of
all literals in either complemented
form or uncomplemented form

Fig. 7.37 Standard POS form

7.16.3 Converting Expressions in Standard SOP or POS Forms

Sum of products form can be converted to standard sum of products by ANDing the terms in the expression with terms formed by ORing the literal and its complement which are not present in that term. For example for a three literal expression with literals A, B and C, if there is a term AB, where C is missing, then we form term $(C + \bar{C})$ and AND it with AB. Therefore, we get $AB(C + \bar{C}) = ABC + AB\bar{C}$.

Steps to convert SOP to standard SOP form

Step 1 : Find the missing literal in each product term if any.

Step 2 : AND each product term having missing literal/s with term/s form by ORing the literal and its complement.

Step 3 : Expand the terms by applying distributive law and reorder the literals in the product terms.

Step 4 : Reduce the expression by omitting repeated product terms if any. Because $A + A = A$.

Step 2 : OR sum term with (missing literal • its complement).

Original sum terms

$$f(A, B, C) = (A+B) + (C\cdot\overline{C}) \quad (B+C) + (A\cdot\overline{A}) \quad (A+C) + (B\cdot\overline{B})$$

Missing literals and their complements

Step 3 : Expand the terms and reorder literals.

Expand :

$$\begin{aligned} \text{Since } A+BC &= (A+B)(A+C) \text{ we have,} \\ f(A, B, C) &= (A+B+C)(A+B+\overline{C})(B+C+A)(B+C+\overline{A}) \\ &\quad (A+C+B)(A+C+\overline{B}) \end{aligned}$$

Reorder :

$$\begin{aligned} f(A, B, C) &= (A+B+C)(A+B+\overline{C})(A+B+C)(\overline{A}+B+C) \\ &\quad (A+B+C)(A+\overline{B}+C) \end{aligned}$$

Step 4 : Omit repeated sum terms

Repeated sum terms

$$f(A, B, C) = (A+B+C)(A+B+\overline{C})(A+B+C)(\overline{A}+B+C)(A+B+C)(A+\overline{B}+C)$$

$$\therefore f(A, B, C) = (A+B+C)(A+B+\overline{C})(\overline{A}+B+C)(A+\overline{B}+C)$$

➡ **Example 7.70 :** *Convert the given expression in standard POS form.*

$$Y = A\cdot(A+B+C)$$

Solution : Step 1 : Find the missing literal/s in each sum term.

$$f(A, B, C) = A\cdot(A+B+C)$$

Literals B and C are missing.

Step 2 : OR sum term with (missing literal • its complement).

$$f(A, B, C) = \left(A+B\cdot\overline{B}+C\cdot\overline{C}\right)(A+B+C)$$

As shown in Table 7.37 each minterm is represented by m_i and each maxterm is represented by M_i, where the subscript i is the decimal number equivalent of the natural binary number. With these shorthand notations logical function can be represented as follows :

1. $$f(A, B, C) = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$$

$$= m_0 + m_1 + m_3 + m_6 = \sum m(0, 1, 3, 6)$$

2. $$f(A, B, C) = (A + B + \overline{C})\,(A + \overline{B} + \overline{C})\,(\overline{A} + \overline{B} + C)$$

$$= M_1 + M_3 + M_6 = \pi\, M\,(1, 3, 6)$$

where Σ denotes **sum of product** while π denotes **product of sum.**

We know that logical expression can be represented in the truth table form. It is possible to write logical expression in standard SOP or POS form corresponding to a given truth table. The logical expression corresponding to a given truth table can be written in a standard sum of products form by writing one product term for each input combination that produces an output of 1. These product terms are ORed together to create the standard sum of products. The product terms are expressed by writing complement of a variable when it appears as an input 0, and the variable itself when it appears as an input 1. Consider, for example, the following truth table :

A	B	C	Y	
0	0	0	0	
0	0	1	0	
0	1	0	1	← $\overline{A}B\overline{C}$
0	1	1	1	← $\overline{A}BC$
1	0	0	0	
1	0	1	0	
1	1	0	1	← $AB\overline{C}$
1	1	1	0	

Table 7.38

The product corresponding to input combination 010 is $\overline{A}B\overline{C}$, the product corresponding to input combination 011 is $\overline{A}BC$, and product corresponding to input combination 110 is $AB\overline{C}$. Thus the standard sum of products form is

$$f(A, B, C) = \overline{A}B\overline{C} + \overline{A}BC + AB\overline{C} = m_2 + m_3 + m_6$$

The logic expression corresponding to a truth table can also be written in a standard product of sums form by writing one sum term for each output 0. The sum terms are expressed by writing complement of a variable when it appears as an input 1, and the variable itself when it appears as an input 0. Consider, for example, the following truth table :

A	B	C	Y	
0	0	0	1	
0	0	1	1	
0	1	0	0	$\leftarrow A + \overline{B} + C$
0	1	1	1	
1	0	0	1	
1	0	1	0	$\leftarrow \overline{A} + B + \overline{C}$
1	1	0	1	
1	1	1	1	

Table 7.39

The sum corresponding to input combinations 010 is $A + \overline{B} + C$, and the sum corresponding to input 101 is $\overline{A} + B + \overline{C}$. Thus, the standard product of sums form is

$$\begin{aligned} f(A, B, C) &= (A + \overline{B} + C)(\overline{A} + B + \overline{C}) \\ &= M_2 + M_5 \end{aligned}$$

7.16.5 Complements of Canonical Formulae

Let us write the standard SOP and POS from the previous truth table :

SOP form : $f(A, B, C) = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,\overline{B}\,\overline{C} + A\,B\,\overline{C} + A\,B\,C$

POS form : $f(A, B, C) = (A + \overline{B} + C)(\overline{A} + B + \overline{C})$

Now by simplifying equation in the POS form we have,

$$\begin{aligned} f(A, B, C) &= A\,\overline{A} + A\,B + A\,\overline{C} + \overline{A}\,\overline{B} + B\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,C + B\,C + C\,\overline{C} \\ &= A\,B + A\,\overline{C} + \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,C + B\,C \end{aligned}$$

Converting to standard sum of products we have,

$$\begin{aligned} f(A, B, C) &= A\,B\,(C + \overline{C}) + A\,\overline{C}\,(B + \overline{B}) + \overline{A}\,\overline{B}\,(C + \overline{C}) + \overline{B}\,\overline{C}\,(A + \overline{A}) \\ &\quad + \overline{A}\,C\,(B + \overline{B}) + B\,C\,(A + \overline{A}) \\ &= A\,B\,C + A\,B\,\overline{C} + A\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} \\ &\quad + \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,C + \overline{A}\,\overline{B}\,C + A\,B\,C + \overline{A}\,B\,C \\ &= A\,B\,C + A\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,C \end{aligned}$$

Rearranging terms we have,

$$= \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,\overline{B}\,\overline{C} + A\,B\,\overline{C} + A\,B\,C$$

Therefore, we can say that POS and SOP derived from the same truth table are logically equivalent. In terms of minterms and maxterms we can then write

$$f(A, B, C) = m_0 + m_1 + m_3 + m_4 + m_6 + m_7 = M_2 + M_5$$

$$\therefore \quad f(A, B, C) = \sum m(0, 1, 3, 4, 6, 7)$$

$$= \pi M(2, 5)$$

From the above expressions we can easily notice that there is a complementary type of relationship between a function expressed in terms of maxterms. Using this complementary relationship we can find logical function in terms of maxterms if function in minterms is known or vice-versa. For example, for a four variables if

$$f(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 10, 12, 14)$$

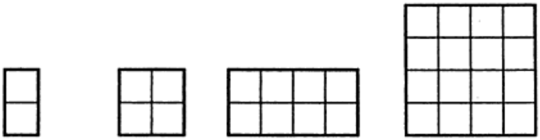
$$\text{then} \quad f(A, B, C, D) = \pi M(1, 3, 5, 7, 9, 11, 13, 15)$$

7.17 Minimization using K-map

We have seen that for simplification of Boolean expressions by Boolean algebra we need better understanding of Boolean laws, rules and theorems. During the process of simplification we have to predict each successive step. For these reasons, we can never be absolutely certain that an expression simplified by Boolean algebra alone is the simplest possible expression. On the other hand, the map method gives us a systematic approach for simplifying a Boolean expression. The map method, first proposed by Veitch and modified by Karnaugh, hence it is known as the **Veitch diagram** or the **Karnaugh map.**

7.17.1 One-Variable, Two-Variable, Three-Variable and Four-Variable Maps

The basis of this method is a graphical chart known as Karnaugh map (K-map). It contains boxes called cells. Each of the cell represents one of the 2^n possible products that can be formed from n variables. Thus, a 2-variable map contains $2^2 = 4$ cells, a 3-variable map contains $2^3 = 8$ cells, and so forth. Fig. 7.38 shows outlines of 1, 2, 3 and 4 variable maps.



1-Variable map (2 cells) 2-Variable map (4 cells) 3-Variable map (8 cells) 4-Variable map (16 cells)

Fig. 7.38 Outlines of 1, 2, 3 and 4 variable Karnaugh maps

Product terms are assigned to the cells of a Karnaugh map by labelling each row and each column of the map with a variable, with its complement, or with a combination of variables and complements. The product term corresponding to a given cell is then the product of all variable in the row and column where the cell is located. Fig. 7.39 shows the way to label the rows and columns of a 1, 2, 3 and 4-variable maps and the product terms corresponding to each cell.

$\bar{A}$	$\bar{A}$ 0
A	A 1

1-Variable map
(a)

	$\bar{B}$	B
$\bar{A}$	$\bar{A}\bar{B}$ 0	$\bar{A}B$ 1
A	$A\bar{B}$ 2	AB 3

2-Variable map
(b)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	$\bar{A}\bar{B}\bar{C}$ 0	$\bar{A}\bar{B}C$ 1	$\bar{A}BC$ 3	$\bar{A}B\bar{C}$ 2
A	$A\bar{B}\bar{C}$ 4	$A\bar{B}C$ 5	ABC 7	$AB\bar{C}$ 6

3-Variable map
(c)

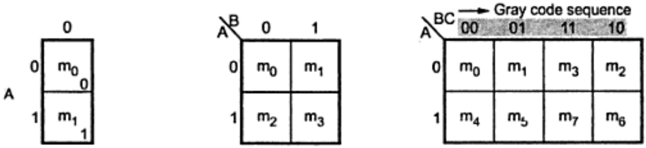
	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	$\bar{A}\bar{B}\bar{C}\bar{D}$ 0	$\bar{A}\bar{B}\bar{C}D$ 1	$\bar{A}\bar{B}CD$ 3	$\bar{A}\bar{B}C\bar{D}$ 2
$\bar{A}B$	$\bar{A}B\bar{C}\bar{D}$ 4	$\bar{A}B\bar{C}D$ 5	$\bar{A}BCD$ 7	$\bar{A}BC\bar{D}$ 6
AB	$AB\bar{C}\bar{D}$ 12	$AB\bar{C}D$ 13	$ABCD$ 15	$ABC\bar{D}$ 14
$A\bar{B}$	$A\bar{B}\bar{C}\bar{D}$ 8	$A\bar{B}\bar{C}D$ 9	$A\bar{B}CD$ 11	$A\bar{B}C\bar{D}$ 10

4-Variable map
(d)

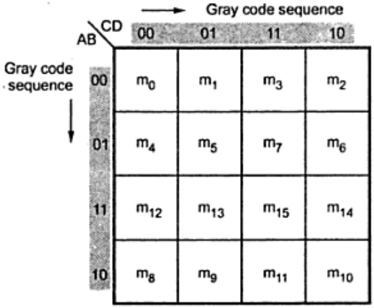
Fig. 7.39 1, 2, 3 and 4 variable maps with product terms

It is important to note that when we move from one cell to the next along any row or from one cell to the next along any column, one and only one variable in the product term changes (to a complemented or to an uncomplemented form). For example, in Fig. 7.39 (b) the only change that occurs in moving along the bottom row from $A\bar{B}$ to AB is the change from $\bar{B}$ to B. Similarly, the only change that occurs in moving down the right column from $\bar{A}$ B to AB is the change from $\bar{A}$ to A. Irrespective of number of variables the labels along each row and column must conform to the single-change rule. We know that the Gray code has same properties (only one variable change when we proceed to next number or previous number) hence gray code is used to label the rows and columns of K-map as shown in Fig. 7.40.

The Fig. 7.40 shows label of the rows and columns of a 1, 2, 3 and 4-variable maps using gray code and the product terms corresponding to each cell. Here, instead of writing actual product terms, corresponding shorthand minterm notations are written in the cell, and row and columns are marked with Gray code instead of variables.


0
A
0
1
m_0
0
m_1
1
B
A
0
1
m_0
m_1
m_2
m_3
Gray code sequence
BC
A
00
01
11
10
m_0
m_1
m_3
m_2
m_4
m_5
m_7
m_6

(a) 1- Variable map **(b) 2-Variable map** **(c) 3-Variable map**


Gray code sequence
CD
AB
00
01
11
10
Gray code sequence
m_0
m_1
m_3
m_2
m_4
m_5
m_7
m_6
m_{12}
m_{13}
m_{15}
m_{14}
m_8
m_9
m_{11}
m_{10}

(d) 4-Variable map

Fig. 7.40 Another way to represent 1, 2, 3 and 4-variable maps

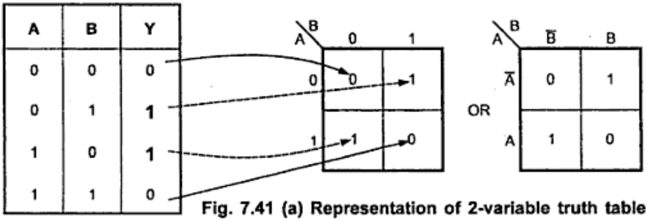
7.17.2 Plotting a Karnaugh Map

We know that logic function can be represented in various forms such as truth table, SOP Boolean expression and POS boolean expression. In this section we will see the procedures to plot the given logic function in any form on the Karnaugh map.

7.17.2.1 Representation of Truth Table on Karnaugh Map

Cell : The smallest unit of a Karnaugh map, corresponding to one line of a truth table. The input variables are the cell's co-ordinates and the output variable is the cell's contents.

Fig. 7.41 shows K-maps plotted from truth tables with 2, 3 and 4 variables. Looking at the Fig. 7.41 we can easily notice that the terms which are having output 1, have the corresponding cells marked with 1s. The other cells are marked with zeros.

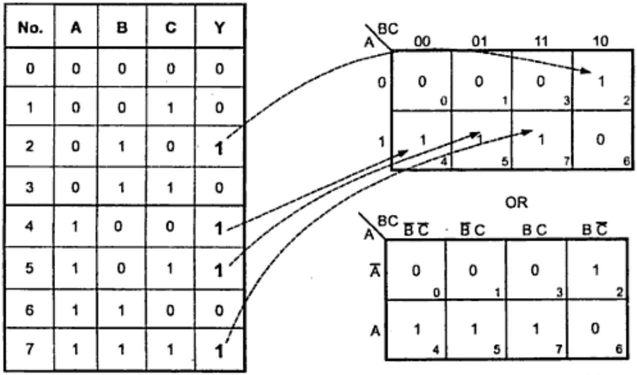


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A B 0 1
0 0 1
1 1 0
OR
A B $\bar{B}$ B
$\bar{A}$ 0 1
A 1 0

Fig. 7.41 (a) Representation of 2-variable truth table on K-map

Note : The student can varify the data in each cell by checking the data in the column Y for particular row number and the data in the same cell number in the K-map.



No.	A	B	C	Y
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1

A BC 00 01 11 10
0 0 0 0 1
0 1 3 2
1 1 1 1 0
4 5 7 6
OR
A BC $\bar{B}\bar{C}$ $\bar{B}C$ BC $B\bar{C}$
$\bar{A}$ 0 0 0 1
0 1 3 2
A 1 1 1 0
4 5 7 6

Fig. 7.41 (b) Representation of 3-variable truth table on K-map

Example 7.74 : *Plot Boolean expression.*

$$Y = (A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)(A+B+\overline{C}+\overline{D})(\overline{A}+\overline{B}+C+\overline{D})(\overline{A}+\overline{B}+\overline{C}+D).$$

Solution : The expression has 4 variables and hence it can be plotted using 4-variable map as shown below

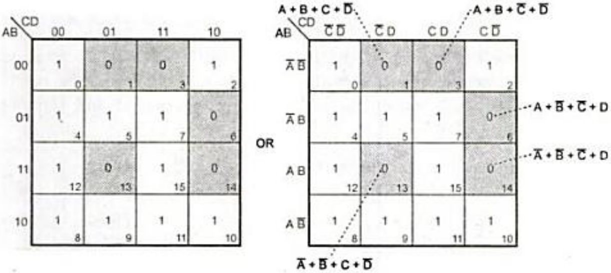

AB CD
00 01 11 10
1 0 0 1
1 1 1 0
1 0 1 0
1 1 1 1
OR
A + B + C + $\overline{D}$
A + B + $\overline{C}$ + $\overline{D}$
$\overline{C}\overline{D}$ $\overline{C}$D CD C$\overline{D}$
$\overline{A}\overline{B}$ $\overline{A}$B AB A$\overline{B}$
A + $\overline{B}$ + $\overline{C}$ + D
$\overline{A}$ + $\overline{B}$ + $\overline{C}$ + D
$\overline{A}$ + $\overline{B}$ + C + $\overline{D}$

Fig. 7.45

$(A + B + C + \overline{D}) = M_1$, $(A + \overline{B} + \overline{C} + D) = M_6$, $(A + B + \overline{C} + \overline{D}) = M_3$,

$(\overline{A} + \overline{B} + C + \overline{D}) = M_{13}$, $(\overline{A} + \overline{B} + \overline{C} + D) = M_{14}$

7.17.3 Grouping Cells for Simplification

In the last section we have seen representation of Boolean function on the Karnaugh map. We have also seen that minterms are marked by 1s and maxterms are marked by 0s. Once the Boolean function is plotted on the Karnaugh map we have to use grouping technique to simplify the Boolean function. The grouping is nothing but combining terms in adjacent cells. Two cells are said to be adjacent if they conform the single change rule, i.e., there is only one variable difference between co-ordinates of two cells. For example, the cells for minterms ABC and $\overline{A}$BC are adjacent. The simplification is achieved by grouping adjacent 1s or 0s in groups of 2^i, where $i = 1, 2, \ldots, n$ and n is the number of variables. When adjacent 1s are grouped then we get result in the sum of products form; otherwise we get result in the product of sums form. Let us see the various grouping rules.

7.17.3.1 Grouping Two Adjacent Ones (Pair)

Fig. 7.46 (a) shows the Karnaugh map for a particular three variable truth table. This K-map contains a pair of 1s that are horizontally adjacent to each other; the first represents $\overline{A}\,\overline{B}C$ and the second represents $\overline{A}BC$. Note that in these two terms only the B variable appears in both normal and complemented form ($\overline{A}$ and C remain unchanged). Thus these two terms can be combined to give a resultant that eliminates the B variable since it appears in both uncomplemented and complemented form. This is easily proved as follows :

$$\begin{aligned} Y &= \overline{A}\,\overline{B}C+\overline{A}BC \\ &= \overline{A}C(\overline{B}+B) && \text{Rule 6 : } [A+\overline{A}=1] \\ &= \overline{A}C \end{aligned}$$

This same principle holds true for any pair of vertically or horizontally adjacent 1s. Fig. 7.46 (b) shows an example of two vertically adjacent 1s. These two can be combined to eliminate A variable since it appears in both its uncomplemented and complemented forms. This gives result

$$Y = \overline{A}BC + ABC = BC$$

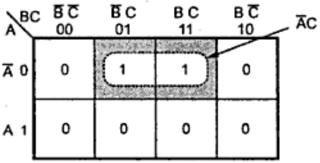

BC
A
$\overline{B}\,\overline{C}$ 00
$\overline{B}C$ 01
BC 11
$B\overline{C}$ 10
$\overline{A}C$
$\overline{A}$ 0
A 1
0 1 1 0
0 0 0 0

Fig. 7.46(a)

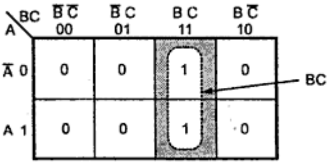

BC
A
$\overline{B}\,\overline{C}$ 00
$\overline{B}C$ 01
BC 11
$B\overline{C}$ 10
BC
$\overline{A}$ 0
A 1
0 0 1 0
0 0 1 0

Fig. 7.46(b)

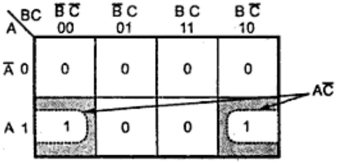
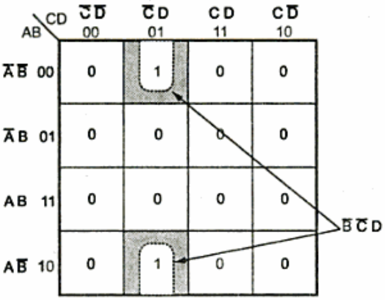

BC
A
$\overline{B}\,\overline{C}$ 00
$\overline{B}C$ 01
BC 11
$B\overline{C}$ 10
$A\overline{C}$
$\overline{A}$ 0
A 1
0 0 0 0
1 0 0 1

Fig. 7.46 (c)

In a Karnaugh map the leftmost column and rightmost column are considered to be adjacent. Thus, the two 1s in these columns with a common row can be combined to eliminate one variable. This is illustrated in Fig. 7.46 (c).

Here variable B has appeared in both its complemented and uncomplemented forms and hence eliminated as follows :

$$\begin{aligned} Y &= A\overline{B}\,\overline{C}+AB\overline{C} \\ &= A\overline{C}(\overline{B}+B) && \text{Rule 6 : } [\overline{A}+A=1] \\ &= A\overline{C} \end{aligned}$$

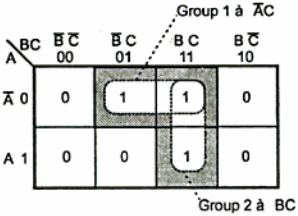


$AB \backslash CD$	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	0	1	0	0
$\bar{A}B$ 01	0	0	0	0
AB 11	0	0	0	0
$A\bar{B}$ 10	0	1	0	0

Fig. 7.46 (d)

Let us see another example shown in Fig. 7.46 (d). Here two 1s from top row and bottom row of some column are combined to eliminate variable A, since in a K map the top row and bottom row are considered to be adjacent.

$$
\begin{aligned}
Y &= \bar{A}\,\bar{B}\,\bar{C}\,D + A\,\bar{B}\,\bar{C}\,D \\
&= \bar{B}\,\bar{C}\,D\,(\bar{A} + A) \\
&= \bar{B}\,\bar{C}\,D
\end{aligned}
$$



$A \backslash BC$	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	1	0
A 1	0	0	1	0

Fig. 7.46 (e)

Fig. 7.46 (e) shows a Karnaugh map that has two overlapping pairs of 1s. This shows that we can share one term between two pairs.

$$
\begin{aligned}
Y &= \bar{A}\,\bar{B}\,C + \bar{A}\,B\,C + A\,B\,C \\
&= \bar{A}\,\bar{B}\,C + \bar{A}\,B\,C + \bar{A}\,B\,C + A\,B\,C && \text{Rule 5 : [A + A = A]} \\
&= \bar{A}\,C\,(\bar{B} + B) + B\,C\,(\bar{A} + A) \\
&= \bar{A}\,C + B\,C
\end{aligned}
$$

Fig. 7.46 (f) shows a K-map where three group of pairs can be formed. But only two pairs are enough to include all 1s present in the K-map. In such cases third pair is not required.

8

Electronic Instruments

8.1 Introduction

The measurement of a given quantity is the result of comparison between the quantity to be measured and a definite standard. The instruments which are used for such measurements are called **measuring instruments**. The three basic quantities in the electronic measurement are current, voltage and power. The measurement of these quantities is important as it is used for obtaining measurement of some other quantity or used to test the performance of some electronic circuits or components etc. The various types of instruments which are used to measure current, voltage and power are classified as analog instruments, electronic instruments and the digital instruments. The digital instruments are increasing in number now-a-days.

The necessary requirements for any measuring instruments are :

i) With the introduction of the instrument in the circuit, the circuit conditions should not be altered. Thus the quantity to be measured should not get affected due to the instrument used.

ii) The power consumed by the instruments for their operation should be as small as possible.

The instrument which measures the current flowing in the circuit is called **ammeter** while the instrument which measures the voltage across any two points of a circuit is called **voltmeter.** The instruments which are used to measure the power are called **power meters** or **wattmeters.**

8.2 Digital Voltmeters

The digital voltmeters generally referred as DVM, convert the analog signals into digital and display the voltages to be measured as discrete numericals instead of pointer deflection, on the digital displays. Such voltmeters can be used to measure a.c. and d.c. voltages and also to measure the quantities like pressure, temperature, stress etc. using proper transducer and signal conditioning circuit. The transducer converts the quantity into the proportional voltage signal and signal conditioning circuit brings the signal into the proper limits which can be easily measured by the digital voltmeter. The output voltage is displayed on the digital display on the front panel. Such a digital output reduces the human reading and interpolation errors and parallax errors.

The DVMs have various features and the advantages, over the conventional analog voltmeters having pointer deflection on the continuous scale.

8.3 Advantages of Digital Voltmeters

The DVMs have number of advantages over conventional analog voltmeters, which are,

1. Due to the digital display, the human reading errors, interpolation errors and parallax errors are reduced.
2. They have input range from +1.000 V to +1000 V with the automatic range selection and the overload indication.
3. The accuracy is high upto ± 0.005 % of the reading.
4. The resolution is better as 1 μV reading can be measured on 1 V range.
5. The input impedance is as high as 10 MΩ.
6. The reading speed is very high due to digital display.
7. They can be programmed and well suited for computerised control.
8. The output in digital form can be directly recorded and it is suitable for further processing also.
9. With the development of IC chips, the cost of DVMs, size and power requirements of DVMs are drastically reduced.
10. Due to small size, are portable.
11. The internal calibration does not depend on the measuring circuit.
12. The BCD output can be printed or used for digital processing.
13. The inclusion of additional circuitry make them suitable for the measurement of quantities like current, impedance, capacitance, temperature, pressure etc.

8.4 Performance Parameters of Digital Voltmeters

The various performance parameters of DVMs are,

1. Number of measurement ranges : The basic range of any DVM is either 1 V or 10 V. With the help of attenuator at the input, the range can be extended from few microvolts to kilovolts.

2. Number of digits in readout : The number of digits of DVMs vary from 3 to 6. More the number of digits, more is the resolution.

3. Accuracy : The accuracy depends on resolution and resolution on number of digits. Hence more number of digits means more accuracy. The accuracy is as high upto ± 0.005% of the reading.

4. Speed of the reading : In the digital voltmeters, it is necessary to convert analog signal into digital signal. The various techniques are used to achieve this conversion. The circuits which are used to achieve such conversion are called **digitizing circuits** and the process is called **digitizing.** The time required for this conversion is called **digitizing period.** The maximum speed of reading and the digitizing period are interrelated. The instrument user must wait, till a stable reading is obtained as it is impossible to follow the visual readout at high reading speeds.

5. Normal mode noise rejection : This is usually obtained through the input filtering or by use of the integration techniques. The noise present at the input, if passed to the analog to digital converting circuit then it can produce the error, especially when meter is used for low voltage measurement. Hence noise is required to be filtered.

6. Common mode noise rejection : This is usually obtained by guarding. A **guard** is a sheet metal box sourrounding the circuitry. A terminal at the front panel makes this 'box' available to the circuit under measurement.

7. Digital output of several types : The digital readout of the instrument may be 4 line BCD, single line serial output etc. Thus the type of digital output also determines the variety of the digital voltmeter.

8. Input impedance : The input impedance of DVM must be as high as possible which reduces the loading effects. Typically it is of the order of 10 MΩ.

8.5 Basic Block Diagram of DVM

Any digital instrument requires analog to digital converter at its input. Hence first block in a general DVM is ADC as shown in the Fig. 8.1.

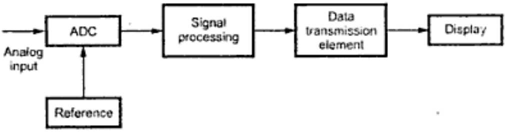


Fig. 8.1 Basic block diagram of DVM

Every ADC requires a reference. The reference is generated internally and reference generator circuitry depends on the type of ADC technique used. The output of ADC is decoded and signal is processed in the decoding stage. Such a decoding is necessary to drive the seven segment display. The data from decoder is then transmitted to the display. The data transmission element may be latches, counters etc. as per the requirement. A digital display shows the necessary digital result of the measurement.

8.6 Classification of Digital Voltmeters

The digital voltmeters are classified mainly based on the technique used for the analog to digital conversion. Depending on this, the digital voltmeters are mainly classified as,

i) Non-integrating type and ii) Integrating type

The non-integrating type digital voltmeters are further classified as,

a) Potentiometric type : These are subclassified as,

1) Servo potentiometric type
2) Successive approximation type
3) Null balance type

b) Ramp type : These are subclassified as,

1) Linear type
2) Staircase type

The integrating type digital voltmeters are classified as :

a) Voltage to frequency converter type
b) Potentiometric type
c) Dual slope integrating type

8.7 Digital Multimeters

The digital multimeter is an instrument which is capable of measuring a.c. voltages, d.c. voltages, a.c. and d.c. currents and resistances over several ranges. The basic circuit of a digital multimeter is always a d.c. voltmeter as shown in the Fig. 8.2.

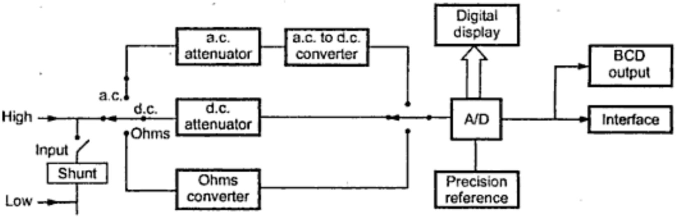

Digital display
a.c. attenuator
a.c. to d.c. converter
BCD output
a.c.
d.c.
High
d.c. attenuator
A/D
Interface
Ohms
Input
Shunt
Ohms converter
Precision reference
Low

Fig. 8.2 Basic scheme of digital multimeter

The current is converted to voltage by passing it through low shunt resistance. The a.c. quantities are converted to d.c. by employing various rectifier and filtering circuits. While for the resistance measurements the meter consists of a precision low current source that is applied across the unknown resistance while gives d.c. voltage. All the quantities are digitized using analog to digital converter and displayed in the digital form on the display. The analog multimeters require no power supply and they suffer less from electric noise and isolation problems but still the digital multimeters have following **advantages** over analog multimeters :

i) The accuracy is very high.

ii) The input impedance is very high hence there is no loading effect.

iii) An unambigious reading at greater viewing distances is obtained.

iv) The output available is electrical which can be used for interfacing with external equipment.

v) Due to improvement in the integrated technology, the prices are going down.

vi) These are available in very small size.

The requirement of power supply, electric noise and isolation problems are the two limitations.

The basic building blocks of digital multimeter are several A/D converters, counting circuitry and an attenuation circuit. Generally dual slope integration type ADC is preferred in the multimeters. The single attenuator circuit is used for both a.c. and d.c. measurements in many commercial multimeters. The block diagram of a digital multimeter is shown in the Fig. 8.3.

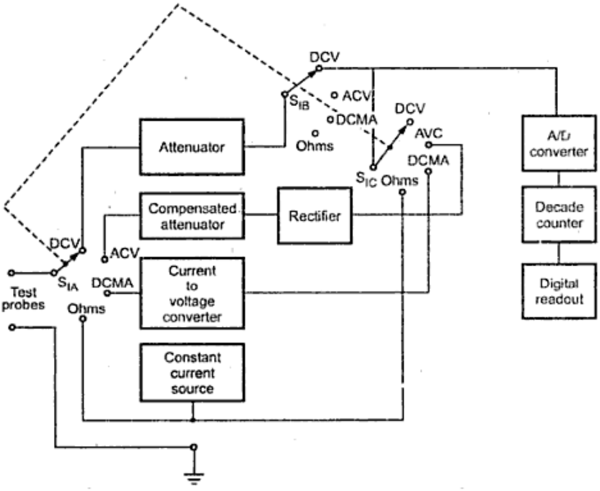

DCV
S_IB
ACV
DCMA
Ohms
DCV
AVC
DCMA
S_IC Ohms
Attenuator
Compensated attenuator
Rectifier
DCV
ACV
S_IA
DCMA
Test probes
Ohms
Current to voltage converter
Constant current source
A/D converter
Decade counter
Digital readout

Fig. 8.3 Block diagram of a digital multimeter

iii) D.C. current

There are five ranges from ± 200 μA to ± 2000 mA.

The resolution is ± 0.01 μA on the lowest range.

The accuracy is ± 0.3 % of reading + two digits.

iv) A.C. current

There are five ranges from 200 μA to 2000 mA.

The accuracy is frequency dependent but the best accuracy of ± 1% + ten digits between 45 Hz and 2 kHz on all the ranges.

v) Resistance

Six ranges are available from 200 Ω to 20 MΩ.

The accuracy is ± 0.1 % of reading + two digits + 0.02 Ω on the lowest range.

vi) Input impedance

The input impedance is about 10 MΩ on all the ranges.

vii) Normal mode noise rejection

It is greater than 60 dB at 50 Hz while the common mode noise rejection is greater than 90 dB at 50 Hz and greater than 120 dB at d.c.

viii) Overload protection

The overload protection of 1000 V d.c. and 750 r.m.s. a.c. is provided.

ix) Diode test

The voltage drop across the diode can be measured for which 1 mA ± 10% of constant current source is used.

x) Conductance

It can display conductance in siemens.

xi) Relative reference

When 'REL' button is pressed, the displayed reading is stored as a reference and then subtracted from the subsequent readings to indicate only amount of deviation from the reference.

xii) Frequency

The frequency range is 200 Hz to 200 kHz autoselection.

8.9 Introduction to C.R.O.

In studying the various electronic, electrical networks and systems, signals which are functions of time, are often encountered. Such signals may be periodic or non periodic in nature. The device which allows, the amplitude of such signals, to be displayed primarily as a function of time, is called **cathode ray oscilloscope**, commonly known as C.R.O. The C.R.O. gives the visual representation of the time varying signals. The oscilloscope has become an universal instrument and is probably most versatile tool for the development of electronic circuits and systems. It is an integral part of electronic laboratories.

The oscilloscope is, infact, a voltmeter. Instead of the mechanical deflection of a metallic pointer as used in the normal voltmeters, the oscilloscope uses the movement of an electron beam against a fluorescent screen, which produces the movement of a visible spot. The movement of such spot on the screen is proportional to the varying magnitude of the signal, which is under measurement.

The electron beam can be deflected in two directions : the horizontal or x-direction and the vertical or y-direction. Thus an electron beam producing a spot can be used to produce two dimensional displays. Thus C.R.O. can be regarded as a fast x-y plotter. The x-axis and y-axis can be used to study the variation of one voltage as a function of another. Typically the x-axis of the oscilloscope represents the time while the y-axis represents variation of the input voltage signal. Thus if the input voltage signal applied to the y-axis of C.R.O. is sinusoidally varying and if x-axis represents the time axis, then the spot moves sinusoidally, and the familiar sinusoidal waveform can be seen on the screen of the oscilloscope. The oscilloscope is so fast device that it can display the periodic signals whose time period is as small as microseconds and even nanoseconds. The C.R.O. basically operates on voltages, but it is possible to convert current, pressure, strain, acceleration and other physical quantities into the voltage using transducers and obtain their visual representations on the C.R.O.

8.10 Cathode Ray Tube (CRT)

The cathode ray tube (CRT) is the heart of the C.R.O. The CRT generates the electron beam, accelerates the beam, deflects the beam and also has a screen where beam becomes visible as a spot. The main parts of the CRT are :

i) Electron gun ii) Deflection system iii) Fluorescent screen

iv) Glass tube or envelope v) Base

A schematic diagram of CRT, showing its structure and main components is shown in the Fig. 8.5.

8.10.4 Glass Tube

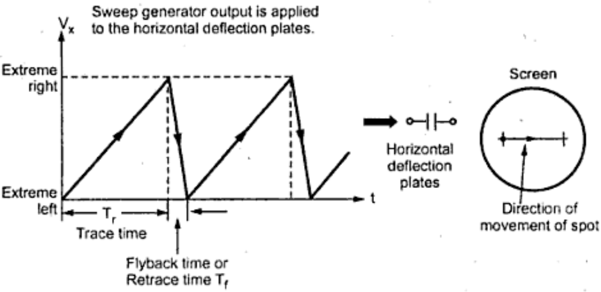
All the components of a CRT are enclosed in an evacuated glass tube called **envelope**. This allows the emitted electrons to move about freely from one end of the tube to the other end.

8.10.5 Base

The base is provided to the CRT through which the connections are made to the various parts.

8.11 Basic Principle of Signal Display

In many applications, it is required to display the voltage as a function of time. By applying such a voltage to the Y input, the vertical deflection of the electron beam will be proportional to the magnitude of this voltage. It is then necessary to convert the horizontal deflection into a time axis. A special unit inside the oscilloscope, called the **sweep generator** or **time base generator**, provides a periodic voltage waveform that varies linearly with time, as shown in the Fig. 8.8. Since this waveform resembles the teeth of hacksaw, it is also called **sawtooth waveform.**



V_x
Sweep generator output is applied to the horizontal deflection plates.
Extreme right
Extreme left
T_r
Trace time
Flyback time or Retrace time T_f
t
Horizontal deflection plates
Screen
Direction of movement of spot

Fig. 8.8 Sawtooth waveform generated by time base generator

Assume that no voltage is applied to vertical deflecting plates, but only this sawtooth voltage V_x is applied to the horizontal deflecting plates. During the **trace time** T_r , the voltage V_x is linearly increasing with time, and hence the electron beam will move linearly in the horizontal direction. At the end of trace period T_r , the beam reaches extreme right hand position in the horizontal direction. At this, instant, the voltage suddenly drops to zero in a short interval of time, known as **flyback period**. Hence the beam suddenly jumps back to the original positions at the extreme left hand side. Then again it starts moving to the right during the next cycle of sawtooth waveform. The fly back of the beam is blanked out by a suitable voltage and is not visible on the screen.

Thus for a selected trace time T_r , the spot moves horizontally across the face of the screen along the x-axis from left to right, with a constant speed, restarts again from the left, and repeats such traces. Depending on the speed of the bright spot and the persistence of vision, the trace produced by the spot will look like a horizontal straight line. Thus the horizontal axis is now converted into a time axis.

When a periodically varying voltage say sinusoidal voltage is applied to the y terminal of the scope and internally generated sawtooth voltage is applied to the horizontal deflection plates, then sawtooth voltage keeps on shifting the spot horizontally while the applied voltage shifts the spot vertically proportional to its magnitude. Hence finally due to the effect of both the voltage, a familiar sinusoidal waveform can be observed on the screen.

When the sweep and signal frequencies are equal, a single cycle appears on the screen. When the sweep is lower than the signal, several cycles appear on the screen. In such case, the number of cycles depends on the ratio of the two frequencies. When the sweep is higher than the signal, less than one cycle appears on the screen.

The display of spot on the screen appears stationary only when the two frequencies i.e. sweep and signal are same or are integral multiples of each other. For any other frequencies the trace on the screen keeps on drifting horizontally. Thus for the trace to appear stationary, the sawtooth voltage is synchronized with signal applied to the vertical input. For the vertical input signal, the triggering pulses are derived for the synchronization.

There are two important requirements of a sweep generator :

1. The sweep must be linear in nature, for all screen horizontal deflection.
2. To move the spot in one direction only, the sweep voltage must drop to zero suddenly, after reaching its maximum value. Otherwise the return sweep will trace the signal backwards.

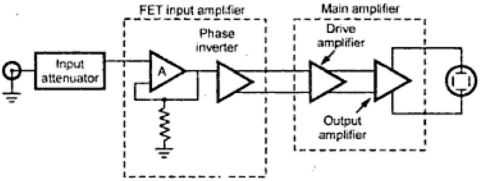

FET input amplifier
Phase inverter
Main amplifier
Drive amplifier
Input attenuator
A
Output amplifier

Fig. 8.10 Vertical amplifier

The phase inverter provides two antiphase output signals which are required to operate the push pull output amplifier.

The push pull operation has advantages like better hum voltage cancellation, even harmonic suppression especially large 2nd harmonic, greater power output per tube and reduced number of defocusing and nonlinear effects.

8.12.3 Delay Line

The delay line is used to delay the signal for some time in the vertical sections. When the delay line is not used, the part of the signal gets lost. Thus the input signal is not applied directly to the vertical plates but is delayed by some time using a **delay line circuit** as shown in the Fig. 8.11.

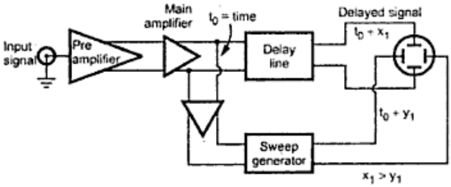
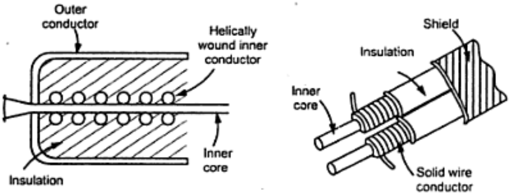

Main amplifier
t0 = time
Delayed signal
t0 + x1
Input signal
Pre amplifier
Delay line
t0 + y1
Sweep generator
x1 > y1

Fig. 8.11 Delay line circuit

Key Point : *As the signal is delayed, the sweep generator output gets enough time to reach to the horizontal plates before signal reaches the vertical plates.*

If the trigger pulse is picked off at a time $t = t_0$ after the signal has passed through the main amplifier then signal is delayed by x_1 nanoseconds while sweep takes y_1 nanoseconds to reach. The design of delay line is such that the delay time x_1 is higher than the time y_1. Generally x_1 is 200 nanoseconds while the y_1 is 80 nanoseconds, thus the sweep starts well in time and no part of the signal is lost.



(a) Helical distributed delay line

(b) Construction details

Fig. 8.14 Distributed delay line

The inductance can be increased by winding the helical inner conductor on ferromagnetic core. This increases the characteristics impedance Z_0 and delay time. Typical parameters for helical, distributed parameter delay line are $Z_0 = 1000\ \Omega$ and $t_d = 180$ nsec/m. The co-axial delay line is advantageous as :

i) It does not require careful adjustment as lumped parameter.

ii) It requires less space.

8.12.4 Trigger Circuit

It is necessary that horizontal deflection starts at the same point of the input vertical signal, each time it sweeps. Hence to synchronize horizontal deflection with vertical deflection a synchronizing or triggering circuit is used. It converts the incoming signal into the triggering pulses, which are used for the synchronization.

8.12.5 Time Base Generator

The time base generator is used to generate the sawtooth voltage, required to deflect the beam in the horizontal section. This voltage deflects the spot at a constant time dependent rate. Thus the x-axis on the screen can be represented as time, which helps to display and analyse the time varying signals.

8.12.6 Horizontal Amplifier

The sawtooth voltage produced by the time base generator may not be of sufficient strength. Hence before giving it to the horizontal deflection plates, it is amplified using the horizontal amplifier.

8.12.7 Power Supply

The power supply block provides the voltages required by CRT to generate and accelerate an electron beam and voltages required by other circuits of the oscilloscope like horizontal amplifier, vertical amplifier etc.

2. Invert : This control inverts the input signal ; that is, it multiplies it by –1. Then positive input voltages become negative and cause downward deflections. The effect of invert is shown in the Fig. 8.17.

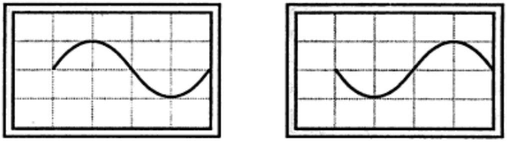

(a) Original signal (b) With invert ON

Fig. 8.17 The effect of invert

3. Position : With the help of this control, the pattern obtained on the screen can be shifted, as a whole, vertically upwards or downwards. This is achieved by adding a d.c. offset voltage to the input signal.

4. X 10 : This control makes the gain of the vertical amplifier 10 times as great as normal, it changes the scale factor by factor of 10. Thus if the X 10 switch is turned 'ON' and the scope is set on 0.05 V/cm, if the actual scale factor is 0.005 V/cm or 5 mV/cm.

5. Vertical Coupling : This switch controls the coupling to the vertical amplifier. The usual choices are A.C., D.C., or ground. The meaning of these various positions are as follows :

i. A.C. : The vertical amplifier is a.c. coupled to the input. Thus the d.c. component of the input is blocked, and only the a.c. components of the input signal deflect the beam vertically. This allows to observe small a.c. signals or large d.c. background.

ii. D.C. : The vertical amplifier has d.c. coupling throughout, so that the deflection corresponds to both the a.c. and the d.c. components of the input.

iii. GROUND : The input to the amplifier is grounded. There will be no vertical deflection. If no voltage is applied to horizontal plates, the spot will be at the position corresponding to ground. It is useful for measuring voltage with respect to ground.

6. Vertical Mode Control : The control serves for the vertical section of the scope as a whole.

Assume that two input signals are simultaneously applied to the two vertical inputs of the scope. Then this switch determines what is displayed on the screen. Thus usual choices are :

1 only, 2 only, 1 + 2 ; 1 – 2, Alternate, and Chop. The meaning of each of these is described briefly below :

i) 1 only : Only the signal at input 1 is displayed.

ii) 2 only : Only the signal at input 2 is displayed.

To measure the amplitude use the following steps :

1. Note down the selection in volts/division from the front panel, selected for measurement.
2. Adjust shift control to adjust signal on screen so that it becomes easy to count number of divisions corresponding to peak to peak value of the signal.
3. Note down peak to peak value in terms of the number of divisions on screen.
4. Use the following relation to obtain peak to peak value in volts.

$$\boxed{V_{P\text{-}P} = (\text{Number of divisions or units noted}) \times \left(\frac{\text{Volts}}{\text{Divisions}}\right)}$$

5. The amplitude can then be calculated as,

$$\boxed{V_m = \text{Amplitude} = \frac{V_{P\text{-}P}}{2}}$$

While the r.m.s. value of sinusoidal signal can be obtained as,

$$\boxed{V_{RMS} = \frac{V_m}{\sqrt{2}} = \frac{V_{P\text{-}P}}{2\sqrt{2}} \quad \text{only for sinusoidal signals}}$$

Key Point : *The volts/div is nothing but **deflection sensitivity** of* C.R.O.

8.14.2 Current Measurement

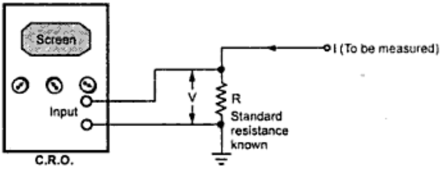
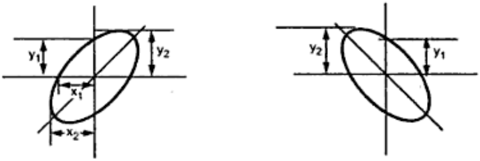


Fig. 8.20

The CRO is basically voltage indicating device. Hence to measure the current, the current is passed through a known standard resistance. The voltage across resistance is displayed on CRO and is measured. This measured voltage divided by the known resistance gives the value of the unknown current. The arrangement is shown in the Fig. 8.20.

Then,

$$\boxed{I = \frac{V_{\text{measured}} \text{ on C.R.O.}}{R}}$$



(a) (b)

Fig. 8.22

If the pattern obtained is as shown in the Fig. 8.22 (b) then the phase angle ϕ is given by,

$$\boxed{\phi = 180° - \sin^{-1}\frac{y_1}{y_2}}$$

8.15.2 Measurement of Frequency

To measure the unknown frequency, the signal with unknown frequency is applied to vertical deflection plates called f_V. Then signal applied to horizontal deflection plates is obtained from a variable frequency oscillator of known frequency f_H.

Thus, f_H = Frequency of signal applied to horizontal plates which is known.

f_V = Frequency of signal applied to vertical plates which is unknown.

Using the shift control, stationary Lissajous figure is obtained on screen such that to the figure vertical and horizontal axes are tangential to one or more points. The patterns depends on the ratio of two frequencies f_H and f_V as shown in the Fig. 8.23.

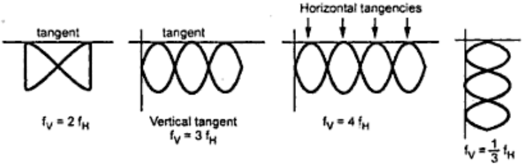


Fig. 8.23

The ratio of two frequencies can be obtained as,

$$\boxed{\frac{f_V}{f_H} = \frac{\text{Number of horizontal tangencies}}{\text{Number of vertical tangencies}}}$$

Contents

- **Semiconductor Diodes and Applications**
  p-n junction, Depletion layer, v-i characteristics, ideal and practical, diode resistance, capacitance diode ratings (average current, repetitive peak current, peak-inverse voltage) p-n junction is as rectifiers (half wave and full wave) filter (Shunt capacitor filter), calculation of ripple factor and load regulation clipping circuits, clamping circuits, voltage multipliers.

  Breakdown Diodes
  Breakdown mechanism (Zener and avalanche), Breakdown characteristics, Zener resistance, Zener diode ratings, Zener diode application as shunt regulator.

- **Bipolar Junction Transistor (BJT)**
  Basic construction, Transistor action, CB, CE and CC configurations, Input/output characteristics, Biasing of transistors, fixed bias, Emitter bias, Potential divider bias, Comparison of biasing circuits. Graphical analysis of CE amplifier, Concept of voltage gain, Current gain, H-parameter model (low frequency), Computation of Ai, Av, Ri, Ro of single transistor CE amplifier configurations.

- **Field Effect Transistor (FET)**
  JFET : Basic construction, Principle of working, Concept of pinch-off, Maximum drain saturation current, Input and transfer characteristics, Characteristics equation, CG, CS and CD configurations, Fixed, Self-biasing of JFET amplifier.
  MOSFET : Depletion and enhancement type MOSFET - construction, operation and characteristics.

- **Operational Amplifier (Op-Amp)**
  Concept of ideal operational amplifier, ideal and practical Op-Amp parameters, inverting, non-inverting and unity gain configurations, Applications of Op-Amp as adders, Difference amplifiers, Integrators and Differentiator.

- **Switching Theory and Logic Design (STLD)**
  Number systems, Conversion of bases, (decimal, binary, octal and hexadecimal numbers) addition and subtraction, Fractional numbers, BCD numbers, Boolean algebra, Logic Gates, Concept of universal gates canonical forms, Minimization using K-map (Don't care conditions also)

- **Electronic Instruments**
  Working principle of digital voltmeter, Digital multimeter (Block diagram approach) CRO (its working with block diagram) measurement of voltage, current, phase and frequency using CRO.

Premier12

First Edition : 2008

Price INR 325/-
ISBN 978-81-8431-503-5
9788184315035

TECHNICAL PUBLICATIONS PUNE

Technical Publications Pune
1, Amit Residency, 412 Shaniwar Peth, Pune - 411030, M.S., India.
Telefax : +91 (020) 24495496/97, Email : technical@vtubooks.com
Visit us at : www.vtubooks.com